

KWIK CIRCUIT FAQ

Designing a Kickback filter for a Precision SAR ADC with Easy Drive

by Jim Catt and Tim Green

FAQ: How to design a kickback filter for an Easy Drive Precision SAR ADC

Introduction

This KWIK (Know-how With Integrated Knowledge) Circuit application note offers a step-by-step guide to address a specific design challenge. For a given set of application circuit requirements, it illustrates how these are addressed using generic formulae and makes them easily scalable to other similar application specifications.

The analog inputs of Successive Approximation Register (SAR) analog-to-digital converters (ADC) present a switched capacitive load to the signal source. During the acquisition phase, the sampling switch connects the sampling capacitor, C_{SH} , to the ADC input pin to track (acquire) the input signal (see Figure 1). The switch remains in this state until the conversion phase, when the switch opens, and the voltage stored on the sampling capacitor (cap) is digitized. After each conversion phase, the sampling switch closes and C_{SH} reconnects to the ADC input.

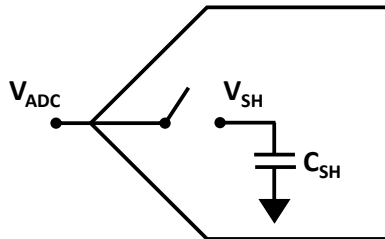


Figure 1. SAR ADC input circuit

When the sampling switch closes at the beginning of the acquisition period, there is always some difference between the C_{SH} voltage (V_{SH}) and the input signal (V_{ADC}), resulting in charge flow into or out of the ADC input. This leads to a transient voltage glitch at C_{SH} and at the input to the ADC. If this glitch is not settled before the next conversion phase, the

SAR ADC will sample and digitize a distorted version of the input signal. The front-end amplifier is therefore tasked with correcting the C_{SH} voltage glitch to within a target error (V_{error}), to prevent settling error artifacts from increasing harmonic distortion and degrading system accuracy.

An RC filter is often placed between the amplifier and the ADC, to function as a charge reservoir that can rapidly deliver/absorb charge to/from C_{SH} , relieving some of the drive requirement on the amplifier. It is important to note that the kickback filter bandwidth often needs to be higher than the Nyquist band, and therefore **it should NOT be used as an anti-aliasing filter**.

This KWIK note uses a simple precision amplifier and SAR ADC circuit to focus on the procedure for selecting RC filter and amplifier components to achieve the SAR ADC setting requirements. The design example features the AD4630-24 Easy Drive SAR ADC, which is designed to pre-charge C_{SH} to the previously sampled voltage, thereby minimizing the charge per sample demanded from the amplifier. The ADA4896-2 operational amplifiers are configured as unity gain buffers to maximize their speed and minimize their output impedance. Additional signal chain use cases will be covered in other KWIK notes.

Design Specifications

For an input signal range of $\pm V_{REF}$, the key system specification goals are listed in Table 1. The circuit schematic is shown in Figure 2.

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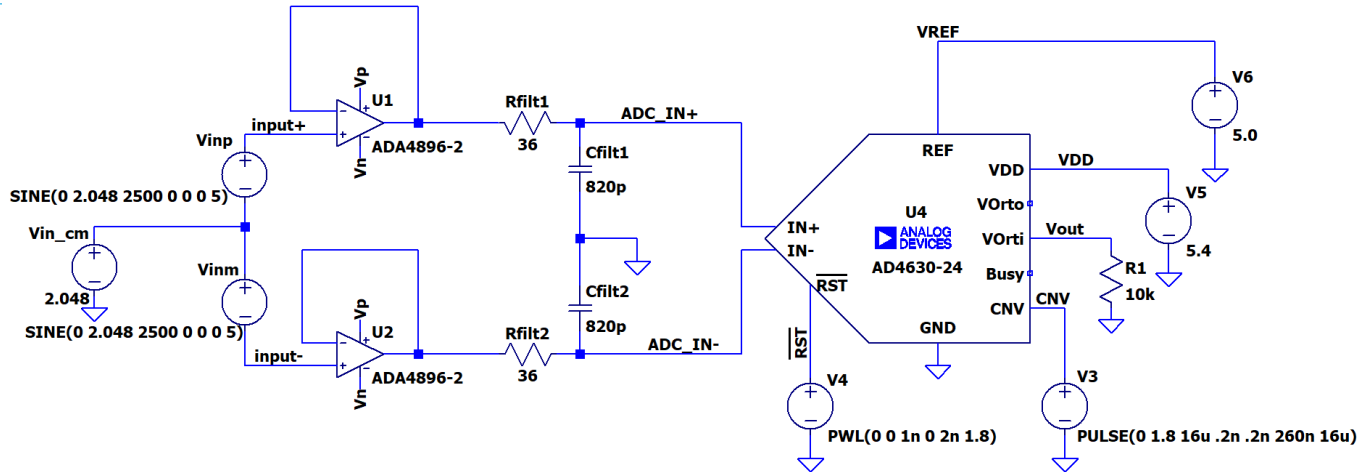


Figure 2. SAR ADC Driver Circuit

Table 1. Design Goal Key Specifications

Differential Input signal V F _{MAX}	F _{SAMPLE} (SPS)	ADC conversion period (ns) (max)	ADC acquisition period (ns) (min)	Op Amp Supplies +Vs/-Vs	ADC Resolution (bits)	V _{REF} (V)	Settling error (V _{error}) (≤ 244 nV)	Settling time (ns)
±4.906V 2.5 kHz	2M	300	244	+5V/-5V	24	4.096	≤ ½ LSB (≤ 244 nV)	≤ 244

Design Description

The circuit presented here contains a pair of unity-gain amplifiers and R-C filter that drives the ADC’s differential inputs over a ±V_{REF} signal range. The goal is to design the R-C kickback filter so that the ADC input voltage settles to less than ½ LSB error at the end of the acquisition period.

The circuit in Figure 2 is composed of the ADA4896-2, an R-C kickback filter at each buffer output, and the AD4630-24 dual channel, 24-bit, 2 MSPS SAR ADC, with EasyDrive inputs. Note that the AD4630-24 input is differential, so the sampled voltage is: IN+ - (IN-).

Design Tips

Verify that the driver amplifier will not be slew rate limited. This can be checked by using the following inequality:

$$F_{MAX} < \frac{\text{Slew rate in V/S}}{2\pi \cdot V_P} \quad (1)$$

Data sheet slew rate specifications are usually given as V/μs, so be sure to normalize the value to volts/second. The value for V_P should be set to one-half the value of either V_{OH} or V_{OL}, whichever has the largest absolute value. The calculated ratio must be higher than F_{MAX}, the highest frequency component of the input signal.

Design Procedure

Assumptions

1. This design procedure assumes that the ADC input circuit pre-charges the sampling capacitor to the previous sample voltage prior to starting a new acquisition cycle. This minimizes the amount of charge that needs to be transferred to the sample cap during the acquisition phase and reduces the drive requirements on the amplifier.
2. The ADC input is not multiplexed. If the ADC input is multiplexed, then it is possible that the voltage step size between samples can be as large as V_{REF}.

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- The input is an AC signal which is continuously sampled.
- The Z_{OUT} characteristic of the amplifier is known or can be simulated. This procedure uses Z_{OUT} of the amplifier to assess the stability of the chosen solution.

Procedure

1. Verify that the amplifier is not slew rate limited.

In this example, $V_P = 2.048V$, and $F_{MAX} = 2.5$ kHz. The ADA4896-2 data sheet indicates that the maximum slew rate is 120 V/us for $G=1$. Using inequality (1):

$$\frac{\text{Slew rate in } \frac{V}{S}}{2\pi \cdot V_P} = \frac{120e6}{2\pi \cdot 2.048} = 9.33 \text{ MHz} > 2.5 \text{ kHz}$$

Therefore, the ADA4896-2 will NOT be slew rate limited for this application.

2. Calculate the maximum voltage droop (V_{Droop}) that can occur when the ADC sampling switch closes.

When the ADC sampling switch closes, there will be a momentary voltage glitch (V_{GLITCH}) in the ADC voltage as the charge from the filter cap and the charge from the sampling cap gets redistributed. V_{GLITCH} is related to V_{STEP} , which is the voltage change in the signal over the conversion period, t_{CONV} . V_{STEP} is a function of the signal frequency and amplitude. From Table 1, f_{MAX} is 2.5kHz. Using $v(t) = V_{PEAK} \cdot \sin(2\pi f_{MAX} t)$, find dv/dt :

$$\begin{aligned} \frac{dv}{dt}(V_{PEAK} \cdot \sin(2\pi f_{MAX} t)) &= \\ &= 2\pi f_{MAX} \cdot V_{PEAK} \cdot \cos(2\pi f_{MAX} t) \cong \frac{\Delta V}{\Delta t} \end{aligned}$$

Since the maximum value of $\cos(*)$ is 1, the maximum value of the derivative is:

$$\frac{\Delta V}{\Delta t} = 2\pi f_{MAX} \cdot V_{PEAK}$$

$$\Delta V = 2\pi \cdot f_{MAX} \cdot V_{PEAK} \cdot \Delta t$$

$\Delta t = t_{CONV}$ of the ADC and $V_{PEAK} = 2.048V$, hence,

$$\Delta V = 2\pi f_{MAX} \cdot V_{PEAK} \cdot t_{CONV}$$

The AD4630-24 acquisition period can begin before the conversion period is complete. Therefore, the worst-case acquisition period (244 ns) is subtracted from the sample cycle duration (500 ns) to obtain the relevant conversion period.

$$t_{CONV} = t_{CYC} - t_{ACQ} = 500 \text{ ns} - 244 \text{ ns} = 256 \text{ ns}$$

The worst-case voltage step size is then computed using the equation for ΔV :

$$\begin{aligned} V_{STEP} = \Delta V &= 2\pi f_{MAX} \cdot V_{PEAK} \cdot t_{CONV} = \\ &= 2\pi \cdot 2500 \cdot 2.048 \cdot 256 \cdot 10^{-9} = 0.00823 \text{ V} \end{aligned}$$

This represents the maximum voltage step size for a 2.5 kHz AC signal based on the worst case acquisition period. However, the voltage glitch on the ADC input is attenuated by the combination of the sampling cap and filter cap, and is approximated by:

$$V_{GLITCH} = V_{STEP} \cdot \left(\frac{C_{SH}}{C_{FILT} + C_{SH}} \right) \quad (2)$$

$$\therefore V_{GLITCH} = 0.00823 \cdot \left(\frac{C_{SH}}{C_{FILT} + C_{SH}} \right)$$

From the AD4630-24 data sheet, we find that $C_{SH} = 58$ pF. A good first estimate of C_{FILT} is $\geq 10 \cdot C_{SH}$, or a value > 580 pF. Equation (2) says that as C_{FILT} increases, the voltage glitch decreases, which should result in a decrease in settling time. Using $C_{FILT} = 820$ pF, the voltage is glitch is:

$$V_{GLITCH} = 0.00823 \cdot \left(\frac{58 \text{ pF}}{820 \text{ pF} + 58 \text{ pF}} \right) = 544 \mu\text{V}$$

This is the glitch for one of the ADC input pins. The AD4630-24 is a differential input SAR, so the differential glitch will be double the glitch on a single input pin, or approximately 1.088 mV. Note that this approximation does not consider the on-resistance of the sampling switch, and so represents a worst-case glitch.

3. Calculate the time constant required for the ADC input voltage to settle to within the desired target error metric.

Traditionally, a target error metric of $\frac{1}{2}$ LSB has been used for settling time, to minimize distortion. However, for high resolution, high linearity ADCs like the AD4630-24, the designer may choose a metric that reflects the INL of the device. For the AD4630-24, the typical INL is 0.1 ppm (1.677 LSBs), and the maximum is 0.9 ppm (15.1 LSBs). Note that the smaller the error metric, the lower the total harmonic distortion (THD) due to settling errors. Most drivers used with the AD4630-24 will be the dominant THD source, so relaxing the settling error specification used in equation (4) below is acceptable. In this note, we will use $\frac{1}{2}$ LSB.

The ADC input will settle exponentially. The time constant, τ , is given by:

$$\tau = \frac{t_{ACQ}}{N} \quad (3)$$

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t_{ACQ} = the acquisition time of the ADC.

N = number of time constants required to settle.

For the AD4630-24, sampling at 2 MSPS, the minimum acquisition time is 244 ns (see data sheet).

For the AD4630-24, 1/2 LSB is:

$$\frac{1}{2} \cdot \frac{2 \cdot V_{REF}}{2^K} = \frac{4.096}{2^{24}} = 244.1 \text{ nV} = \frac{1}{2} \text{ LSB}$$

The number of time constants, N , can be expressed as:

$$N = \ln\left(\frac{V_{GLITCH}}{\frac{1}{2} \text{ LSB}}\right) = \ln\left(\frac{0.544 \text{ mV}}{244.1 \text{ nV}}\right) = 7.709 \quad (4)$$

Substitute (4) into (3):

$$\tau = \frac{t_{ACQ}}{\ln\left(\frac{V_{GLITCH}}{\frac{1}{2} \text{ LSB}}\right)} \quad (5)$$

$$\tau = \frac{244 \text{ ns}}{7.709} = 3.166 \cdot 10^{-8} \text{ ns.}$$

Together, τ and N give a predicted settling time of 244 ns.

4. Calculate the kickback filter bandwidth using τ .

Note that the time constant can also be used to express the R-C bandwidth:

$$f_{RC-BW} = \frac{1}{2\pi \cdot \tau} = \frac{1}{2\pi RC} \quad (6)$$

Therefore, using the expected voltage glitch, target settling error and ADC resolution, the R-C kickback filter time constant and bandwidth can be calculated.

From equation (6), the filter bandwidth is:

$$f_{RC-BW} = \frac{1}{2\pi \cdot 3.166 \cdot 10^{-8}} = 5.026 \text{ MHz} \quad (7)$$

Equation (5) tells us that $\tau = R \cdot C = 31.66 \text{ ns}$.

Choosing R or C enables the computation of the companion component. Note that the bandwidth in (7) is much greater than the Nyquist bandwidth ($F_s/2 = 1 \text{ MHz}$) and will not provide any anti-aliasing protection. An anti-aliasing filter is still required in the signal chain, typically in front of the driver or incorporated into the driver.

5. Select R-C filter component values.

Knowing the closed loop Z_{OUT} characteristic of an amplifier is important for determining the Z_{LOAD} of the

filter that can be driven by the amplifier while maintaining stability. Figure 3 is a plot of the closed loop Z_{OUT} of the ADA4896-2 (see data sheet), shown by the red trace with a +20 dB/decade slope. This is plotted along with impedance plots for two different values of capacitive loads. If a purely capacitive load with a -20 dB/decade slope intersects Z_{OUT} at a frequency where the latter has a slope of +20 dB/decade (inductive), the two reactances cancel, satisfying the conditions for an oscillator, thus causing oscillation during settling in response to a step change in the voltage. Even if the reactances do not perfectly cancel, the signal settling period will be extended and more ringing will occur as the reactances get closer to perfect cancellation. Reference [3], part 4, provides additional insight into driving capacitive loads.

Note that the Z_{OUT} plot in Figure 3 has an inductive characteristic up to approximately 160 MHz. At 160 MHz, the plot peaks at about 64 ohms, and eventually approaches a steady state value of approximately 33 ohms. A purely capacitive load of approximately 16 pF (green trace) will have an impedance of 63 ohms at 160 MHz and is plotted on the graph. The slope of Z_{OUT} at 160 MHz is nearly flat so the likelihood of oscillation occurring with this cap load is almost zero, with a short settling time for a step change in the signal. As larger cap loads are applied, the settling time will lengthen, and it will exhibit an increasing amount of damped oscillation. For example, a line representing 9.4 nF (blue trace) intersects Z_{OUT} at approximately 10 MHz (where $Z_{OUT} \approx 2 \text{ ohms}$). This cap load will cause sustained oscillation in the range of 10 MHz.

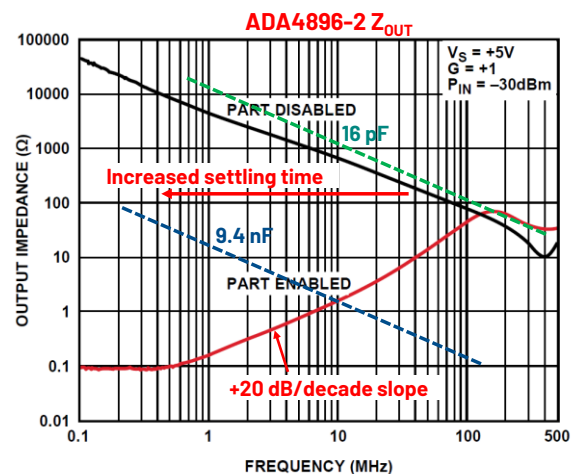


Figure 3. Closed Loop Z_{OUT} plot for ADA4896-2

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An R-C filter will add some series resistance and changes the characteristic of the Z_{LOAD} curve. Figure 4 illustrates the ADA4896 Z_{OUT} ($G=1$) plotted along with two examples of the Z_{LOAD} curves for different R-C filter combinations that have bandwidths higher than 5.026 MHz. For $R=30$ ohms, $C=1000$ pF (5.3 MHz bandwidth, green trace), the Z_{LOAD} plot asymptotically approaches $R=30$ ohms, and intersects the closed loop Z_{OUT} trace (red) at approximately 80 MHz. For $R=36$ ohms and $C=820$ pF (5.39 MHz bandwidth, blue trace), the Z_{LOAD} plot intersects the closed loop Z_{OUT} trace at approximately 90 MHz. Both filter examples have nearly flat slope at the intercept frequencies, indicating that either filter should have acceptable settling time.

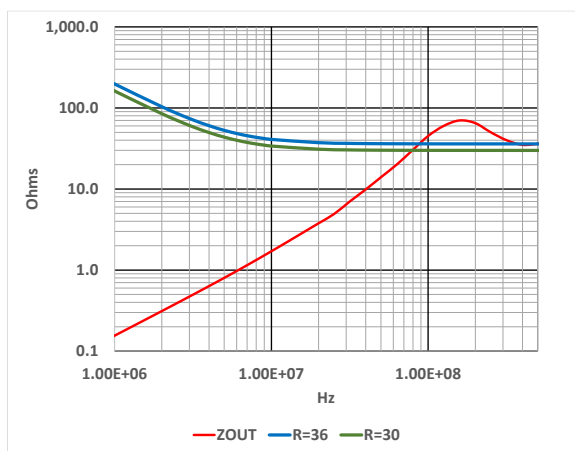


Figure 4. ADA4896 Z_{OUT} vs two R-C options

The following steps can be used to select R_{FILT} and C_{FILT} .

- Calculate the value of R_{FILT} that, when combined with the initial value of the filter cap used to calculate the voltage droop (820 pF in this case), the required bandwidth is achieved. Use equation (6) and rearrange to solve for R_{FILT} .

$$R_{FILT} = \frac{1}{2\pi \cdot f_{RC-BW} \cdot C_{FILT}}$$

$$= \frac{1}{2\pi \cdot 5.026 \cdot 10^6 \cdot 820 \cdot 10^{-12}} = 38.6 \text{ ohms}$$

The closest standard value is 39 ohms but using a slightly smaller R_{FILT} value will increase the filter bandwidth and reduce the settling time. Smaller values of R_{FILT} will also reduce the distortion generated in the ADC (see reference [2], part 7). For this design, we will use $R_{FILT} = 36$ ohms, $C = 820$ pF.

- Calculate and plot the $|Z_{LOAD}(f)|$ curve over a relevant frequency range using:

$$|Z_{LOAD}(f)| = \sqrt{R_{FILT}^2 + \left(\frac{1}{2\pi \cdot f \cdot C_{FILT}}\right)^2} \quad (8)$$

Plot this along with Z_{OUT} , as in Figure 4

- Ensure that the slope of the Z_{LOAD} curve at the intersect frequency (f_{INT}) is *much* less than -20 dB/decade. This assumes that Z_{OUT} of the amplifier, at the frequency intercept point, has an inductive characteristic of +20 dB/decade at the intersection frequency. The slope of Z_{LOAD} (from step b above) at any frequency f can be checked using the derivative:

$$\frac{dZ_{LOAD}}{df} = \frac{-R_{FILT} \cdot f_{RC-BW}}{f^2} \quad (9)$$

f_{RC-BW} is from equation (6). Using equation (9) and noting that we want the equivalent slope expressed in dB/decade to be less than some boundary value, the following inequality can be used to test the slope of $|Z(f)|$ at the intercept frequency f_{INT} :

$$\frac{R_{FILT}}{|Z_{LOAD}(f_{INT})|} \cdot \frac{f_{RC-BW}}{f_{INT}} < M \quad (10)$$

[See the Appendix for derivation of inequality (10)]

The integer-valued boundary value M is chosen based upon the amount of desired margin in the slope of Z_{LOAD} . For example, if we want to verify that the slope of Z_{LOAD} is -20 dB/decade or less, $M = 10$. If -10 dB/decade is the chosen slope limit, then $M = 3.16$. The appendix explains how to calculate the boundary value.

Using $R_{FILT} = 36$ ohms, $f_{RC-BW} = 5.39$ MHz, $f_{INT} \approx 87$ MHz, and $|Z(f_{INT})| = 36$ ohms (estimated from the Z_{LOAD}/Z_{OUT} plot), check inequality (10):

$$= \frac{36}{36} \cdot \frac{5.39e6}{87e6} \approx 0.06195 < 3.16$$

Inequality (10) assumes that the slope of Z_{OUT} at the intercept point is +20 dB/decade and furthermore, does not include any margin. However, it is possible that Z_{LOAD} intercepts Z_{OUT} at a point where the slope of the latter is slightly more or less than +20 dB (but still positive). The key point to understand is that if the two slopes have opposite sign, but equal magnitude, there is a risk of excessive oscillation during settling of the filter. The derivation of inequality (10) in the appendix explains how to modify the right side of the inequality to adjust for a significant departure from +20 dB in the slope of Z_{OUT} , or to achieve more design margin.

Design Simulations

An LTspice simulation schematic was built to check the filter performance and verify that it settles to within

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½ LSB in the required time, using the LTspice models for the ADA4896 and the AD4630-24. The simulation schematic is shown in Figure 2. The ADA4896 is configured as a pair of unity gain buffers, followed by the R-C filter and the ADC. The simulation was run with both AC and DC inputs. The AC simulation is used to estimate the size of the voltage glitch at the start of the acquisition period, and the DC simulation is used to measure the settling time and settling error.

The differential voltage glitch at the beginning of the acquisition period, from the AC simulation, is shown in Figure 5. Figure 6. Cursor values for Figure 5 Figure 6 shows that the simulated voltage droop is approximately -539 uV, which is approximately one-half the predicted 1.088 mV. As noted before, the predicted value assumes that the sampling switch has zero on-resistance, while the ADC macro model uses 37 ohms (from the data sheet). The on-resistance will moderate the charge transfer and reduce the voltage glitch. Consequently, the voltage glitch estimate by equation (2) is a worst-case estimate.

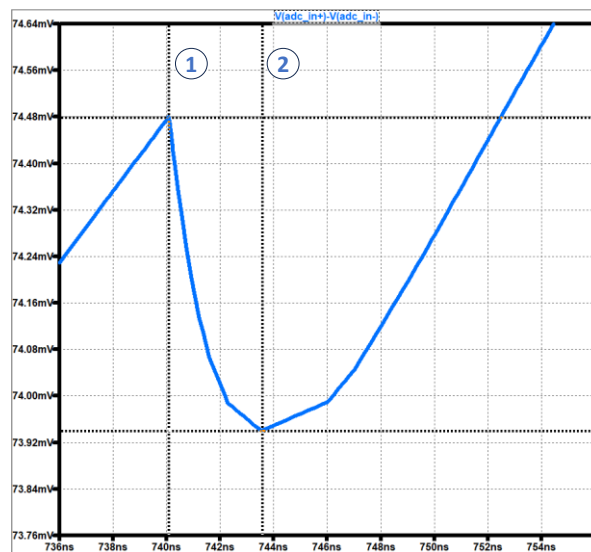


Figure 5. LTspice AC simulation – voltage glitch at start of acquisition

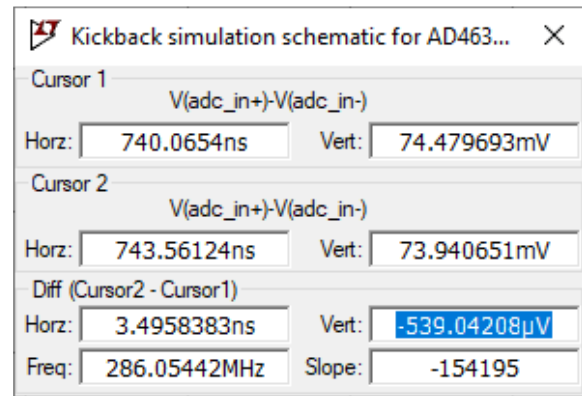


Figure 6. Cursor values for Figure 5

Figure 7 illustrates the settling time obtained from the DC simulation. Figure 8 shows that the measured settling time is less than 242 ns, at which point the settling error is -244.1 nV. This settling time agrees closely with the expected settling time of 244 ns.

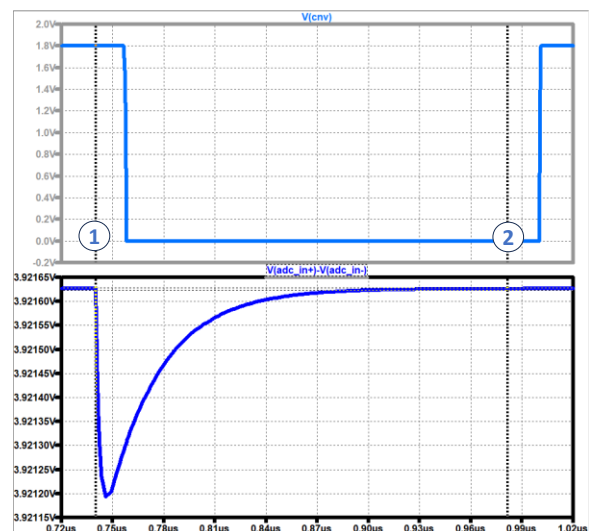


Figure 7. LTspice DC simulation - settling time.

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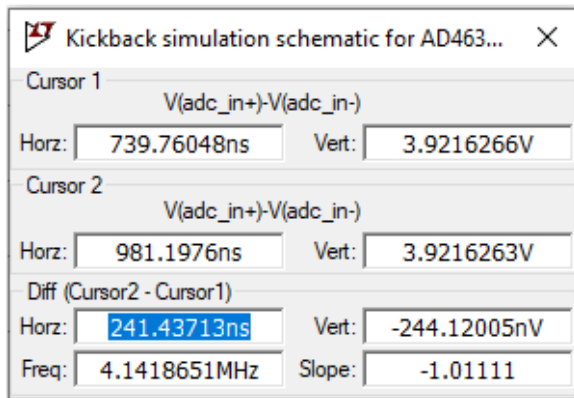


Figure 8. Cursor values for Figure 7

Figure 9 illustrates the settling error at the start of the next conversion and Figure 10 shows that it's approximately -132.6 nV.

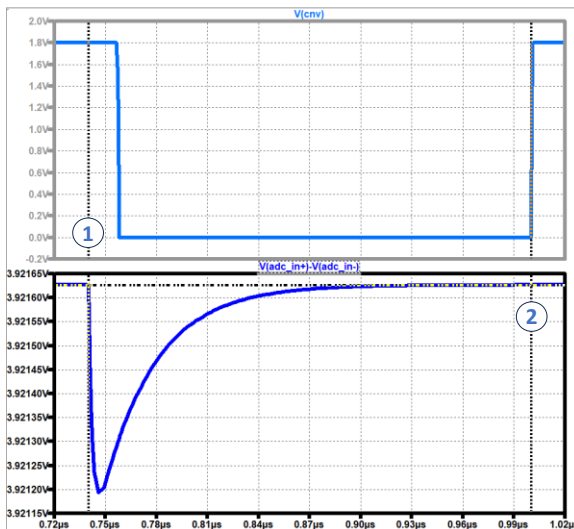


Figure 9. Simulated settling error at start of conversion.

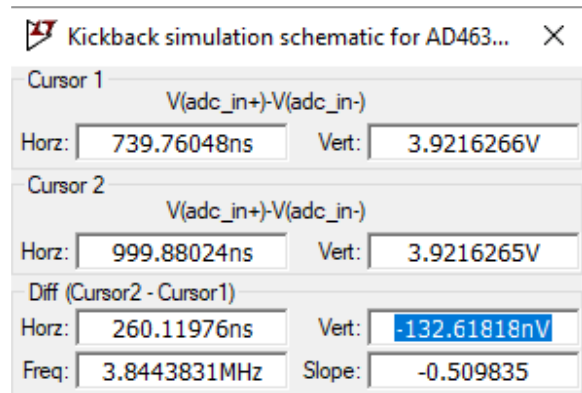


Figure 10. Cursor values for Figure 9

Table 2 summarizes the design goals and the simulation results. In this case, because the designed filter bandwidth is slightly higher than the calculated value, the design goals were met with some small margin. To account for variation over temperature and component tolerance, the design goal of 244 ns can be reduced to increase the design margin and better ensure that the maximum settling error is not violated.

Table 2. Design Goal vs. Simulation

Parameter	Design Goal	Simulation
Settling error at the start of the next conversion period	≤ 244.1 nV	132.6 nV
Settling time to within the error goal	≤ 244 ns	< 242 ns

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Design Devices

Table 3. Op Amp

Part Number	V _{os} (μ V) max	I _{bias} (μ A) typ.	GBP, V _{out} = 2 V _{pp} (MHz) typ	Slew Rate (V/ μ s) typ.	V _{noise} ($\frac{nV}{\sqrt{Hz}}$) typ	I _s (A) typ	V _s span (V ⁺ /V ⁻) (V)
ADA4896-2	+/- 500	-11	30	120	2.4	0.003	+5/-5

Table 4. ADC

Part Number	Resolution (bits)	F _{SAMPLE} (MSPS) max	Input Type (SE or DIFF)	V _{IN} range per input pin. (V)	SNR (dB) typ (1 kHz f _{IN})	INL (ppm) typ	Data Interface (I2C, SPI,Parallel)
AD4630-24	24	2	Fully DIFF	0v to V _{REF}	105.7	+/- 0.1	Flexi-SPI

Table 5. Voltage Reference

Part Number	Output Voltage (V)	Initial Accuracy, Max. (%)	Temperature Coefficient, Max. (ppm/ $^{\circ}$ C)	Line Regulation, Typ. (ppm/V)	Output Noise, Typ. (ppm _{RMS})	Long Term Drift, Typ. ($\frac{ppm}{\sqrt{kHr}}$)
LTC6655-4.096	4.096	+/-0.025	2	5	0.21	60

References

- [1] "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter", Alan Walsh, Analogue Dialogue 46-12, December 2012.
- [2] "Stability 101: Loop Gain in Operational Amplifiers", Analog Devices, Inc. Part 1 of a five-part series on operational amplifiers and stability. <https://www.analog.com/en/resources/media-center/videos/1834668354001.html>
- [3] "Driving SAR ADCs Part 1: Analog Input Model", Analog Devices, Inc. This is part 1 of a seven-part video series on driving SAR ADCs. <https://www.analog.com/en/resources/media-center/videos/5990687361001.html>
- [4] KWIK Classes, "Op Amp Stability Basics: Part 1-Part 6". <https://ez.analog.com/precision-technology-signal-chains/w/kwik-circuits/32236/kwik-classes>

Acknowledgments

Tyler Schmitt, Senior Supervisor, Product Applications, Analog Devices, Inc.

LTspice

LTspice® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

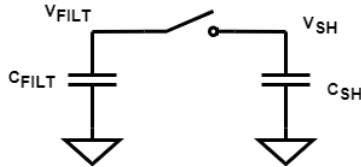
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Appendix

Derivation of equation (2)

$$V_{GLITCH} = -V_{STEP} \cdot \frac{C_{SH}}{C_{FILT} + C_{SH}}$$

C_{FILT} = the filter capacitor, C_{SH} = the sample capacitor



Assumptions:

1. Before the switch closes, $V_{SH} = \frac{Q_{SH}}{C_{SH}}$, and $V_{FILT} = V_{SH} + V_{STEP} = \frac{Q_{FILT} + Q_{STEP}}{C_{FILT}}$. Q_{STEP} is the charge added to C_{FILT} due to V_{STEP} .
2. The R_{ON} resistance of the switch is zero (or negligible).

After the switch closes, $V_{FINAL} = \frac{Q_{FILT} + Q_{STEP} + Q_{SH}}{C_{FILT} + C_{SH}}$.

$$\begin{aligned} V_{GLITCH} &= V_{FINAL} - V_{FILT} \\ &= \frac{Q_{FILT} + Q_{STEP} + Q_{SH}}{C_{FILT} + C_{SH}} - \frac{Q_{FILT} + Q_{STEP}}{C_{FILT}} \\ &= \frac{C_{FILT} \cdot (Q_{FILT} + Q_{STEP} + Q_{SH}) - (C_{FILT} + C_{SH}) \cdot (Q_{FILT} + Q_{STEP})}{C_{FILT} \cdot (C_{FILT} + C_{SH})} \\ &= \frac{C_{FILT} \cdot Q_{SH} - C_{SH} \cdot Q_{FILT} - C_{SH} \cdot Q_{STEP}}{C_{FILT} \cdot (C_{FILT} + C_{SH})} \\ &= \frac{V_{SH} \cdot C_{SH}}{C_{FILT} + C_{SH}} - \frac{C_{SH}}{C_{FILT}} \cdot \left(\frac{V_{FILT} \cdot C_{FILT} + V_{STEP} \cdot C_{FILT}}{C_{FILT} + C_{SH}} \right) \\ &= V_{FILT} \cdot \left(\frac{C_{SH}}{C_{FILT} + C_{SH}} \right) - \frac{C_{SH}}{C_{FILT} + C_{SH}} \cdot (V_{FILT} + V_{STEP}) \\ &= \frac{-V_{STEP} \cdot C_{SH}}{C_{FILT} + C_{SH}} \end{aligned}$$

Derivation of equation (10):

$$\frac{R}{|Z_{LOAD}(f_{INT})|} \cdot \frac{f_{RC-BW}}{f_{INT}} < 10$$

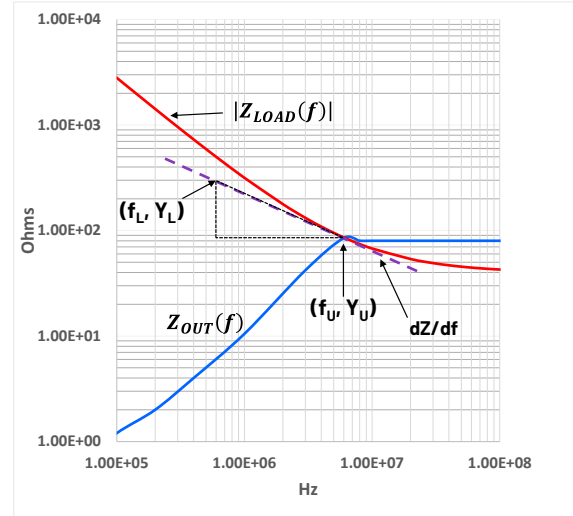


Figure A.

Refer to Figure A. Starting with $m = \text{slope} = \frac{(Y_U - Y_L)}{(f_U - f_L)} = \frac{dZ}{df} = \frac{-R \cdot f_{RC-BW}}{f^2}$

$$f_U = f_{INT}$$

$$f_L = \frac{f_U}{10} = \frac{f_{INT}}{10}$$

$$Y_U = |Z(f_{INT})|$$

$$\therefore m = \frac{(Y_L - |Z(f_{INT})|)}{f_{INT} - \frac{f_{INT}}{10}} = \frac{-R \cdot f_{RC-BW}}{f_{INT}^2}$$

Solving for Y_L and then writing the ratio Y_U/Y_L :

$$Y_L = |Z(f_{INT})| + \frac{0.9 \cdot R \cdot f_{RC-BW}}{f_{INT}}$$

$$\frac{Y_U}{Y_L} = \frac{Z(f_{INT})}{|Z(f_{INT})| + \frac{0.9 \cdot R \cdot f_{RC-BW}}{f_{INT}}} = \frac{1}{1 + \frac{0.9 \cdot R \cdot f_{RC-BW}}{|Z(f_{INT})| \cdot f_{INT}}}$$

$$\text{Since } -\frac{20\text{dB}}{\text{dec}} = 20 \cdot \log\left(\frac{Y_U}{Y_L}\right) \rightarrow \frac{Y_U}{Y_L} = \frac{1}{10},$$

$$\therefore \frac{1}{1 + \frac{0.9 \cdot R \cdot f_{RC-BW}}{|Z(f_{INT})| \cdot f_{INT}}} > \frac{1}{10} \rightarrow \frac{R \cdot f_{RC-BW}}{|Z(f_{INT})| \cdot f_{INT}} < 10$$

Designing a Kickback filter for a Precision SAR ADC with Easy Drive

Satisfying the above condition ensures that the slope of $|Z(f_{INT})|$ is less than -20 dB/dec.

However, if the slope of Z_{OUT} is less than +20 dB/decade at the intercept point, then the boundary value on the right side of the inequality must be adjusted. As well, to improve operating margin, the designer may want to ensure that the slope magnitude of Z_{LOAD} is much less than that of Z_{OUT} . In either case, the adjustment operation is the same.

Example: Assume that the slope of Z_{OUT} is +20 dB/decade at the intercept point, but we want

significant margin in the slope of Z_{LOAD} . For example, we can specify that the slope of Z_{LOAD} must be less than -10 dB/decade. This means,

$$-\frac{10\text{dB}}{\text{dec}} = 20 \cdot \log\left(\frac{Y_U}{Y_L}\right) \rightarrow \frac{Y_U}{Y_L} = \frac{1}{3.16}$$

Thus, the boundary value of 10 on the right side of the inequality is replaced with 3.16. The rewritten inequality becomes:

$$\frac{R \cdot f_{RC-BW}}{|Z(f_{INT})| \cdot f_{INT}} < 3.16$$