KWIK CIRCUIT FAQ

Bipolar Input, Fully Differential Output, Single Supply ADC Driver Design – Guy Hoover

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

FAQ: What do I need to consider when designing a bipolar input fully differential output ADC Driver

Introduction

Most ADC driver circuits require both positive and negative supply voltages, as well as having supply voltage that exceeds the input range of the ADC. This requirement is to ensure that there is enough headroom swing at the input and output stages. Sometimes, due to budget or space constraints, having a positive and negative supply rails is just not possible. To combat this, we will go through some of the steps that need to be consider when designing and ADC driver for a bipolar input that has a fully differential output, while ensuring that the desired noise and distortion performance are met.

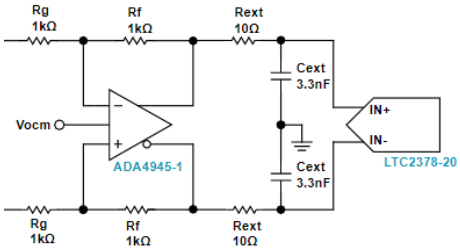

Figure 1. – ADC Driver and ADC

The circuit in Figure 1 provides an ADC driver, that operates from a single supply, scaled to operate for an input signal range of $\pm 0.8V_{REF}$, for a differential input ADC.

Design Specifications Example

For this example the design requirement specifications are shown in Table 1

Table 1. Design Goal Key Specifications

Specification	Design Requirement
Input Single Ended	+/-4Vp
Output Differential	+/-4Vp
Output Common Mode	2.5V
Supplies +Vs/-Vs	+5.75V/0V
ADC Fully Differential	20 Bit
Vref	5V
THD	-120dB
SNR	98db

For this example the circuit in in Figure 1is used, where the ADA4945-1 a fully differential amplifier (FDA) was selected as the ADC driver, which includes is anti-aliasing filter, for the ADC the LTC2378-20, 20-bit, 1Msps was selected.

As can be seen from in Figure 1the ADA4945-1 is configured as a single-ended-to-differential driver. The ADC selected for this example is the LTC2378-20, usually most ADCs have an absolute input range from 0 to V_{REF}, it should be noted that the LTC2378-20 has a digital gain compression mode, which enables the upper boundary of the input signal range to be rescaled to a value between 0.1Vref and 0.9Vref, this eases the voltage output swing requirements of the ADC input driver.

Design Tips / Considerations

1. If a larger or smaller signal range is required, the ratio of RF/RG can be modified.
   For example, if a +/-10V signal range were required, RG can be increased while keeping RF at its original value.
   The following formula can be used to recalculate RG:
   $RG=(V_{IN}/V_{OUT})*RF$

   where:
   $V_{OUT}=ADC_{IN+}(MAX) - ADC_{IN-}(MIN)$
   $V_{IN}=V_{IN}(MAX)-V_{IN}(MIN)$.

2. A gain error will result if the filter between the driver and ADC does not have time to settle. Depending on the application, a small gain error may be tolerable, however the inability to settle can also cause distortion which must be avoided.

For further information on the impact of the settling use Analog Devices Precision ADC Driver Tool, this tool offers a quick and easy way to review the typical performance and obtain an estimate of the circuits SNR and THD performance.

3. The limitation of the bandwidth of the signal provided to the ADC, is determined but resistors Rfilt1, Rfilt2 and capacitors Cfilt1, Cfilt2 limits. This filter helps to reduce the noise seen at the ADC inputs. This filter also helps to isolate the input driver ADA4945-1 output from the sampling glitches generated by the ADC inputs if they the ADC input is not buffered.

Design Procedure

(See Figure 2 for ADA4945-1 Circuit Definitions)

1. ADC (LTC2378-20)

Full scale input, $\pm V_{FS}$, digital gain compression enabled
V_{REF}=5V
$\pm V_{FS}$=±5V*0.8= ±4V

2. Driver Amp (ADA4945-1):

V_{OCM} will be biased to $V_{REF}/2$.
Gain = V_{OUTdm_pp}/V_{INdm_pp}
Gain = 8Vpp/8Vpp=1

Best THD, from the datasheet, is by using 1kΩ for RF and RG.
If SNR is more important than THD, 499Ω can be used for RF and RG with a 1dB improvement in SNR.

2.1 Driver Amp (ADA4945-1) Output Swing:

This driver Amp has a differential output, swinging about V_{OCM},

Calculating the positive and negative output swing of V_{OUT+} and V_{OUT-}

$$V_{OCM} = \frac{V_{REF}}{2} = \frac{5V}{2} = 2.5V$$
$$V_{OUTdm} = \pm 4V$$
$$V_{OUTdm} = V_{+OUT} - V_{-OUT}$$

For $V_{OUTdm} = +V_{FS}$:

$$V_{OUTdm} = 4V$$
$$V_{+OUT} = V_{OCM} + \frac{V_{OUT\_dif}}{2}$$
$$V_{+OUT} = 2.5V + \frac{4V}{2} = 4.5V$$
$$V_{-OUT} = V_{OCM} - \frac{V_{OUT\_dif}}{2}$$
$$V_{-OUT} = 2.5V - \frac{4V}{2} = 0.5V$$

Thus The ADA4945-1 outputs must be able to swing from 0.5V to 4.5V for this application.

2.1 Driver Amp (ADA4945-1) Input Swing:

For
$V_{OUTdm} = +V_{FS}$ Compute Input common mode voltage

$$V_{OUTdm} = +4V, +D_{I_N} = 4V, -D_{IN} = 0V,$$
$$V_{OUT+} = 4.5V, V_{OUT-} = 0.5V$$

$$V_{+IN} = +D_{IN}\left(\frac{RF}{RF+RG}\right) + V_{-OUT}\left(\frac{RG}{RF+RG}\right)$$

$$V_{+IN} = +4V\left(\frac{1k}{1k+1k}\right) + 0.5V\left(\frac{1k}{1k+1k}\right) = 2.25V$$

$$V_{-IN} = -D_{IN}\left(\frac{RF}{RF+RG}\right) + V_{+OUT}\left(\frac{RG}{RF+RG}\right)$$

$$V_{-IN} = 0V\left(\frac{1k}{1k+1k}\right) + 4.5V\left(\frac{1k}{1k+1k}\right) = 2.25V$$

For $V_{OUTdm} = -V_{FS}$

Compute Input Common Mode Voltage:

$$V_{OUTdm} = -4V, +D_{I_N} = -4V, -D_{IN} = 0V, V_{OUT+} = 0.5V, V_{OUT-} = 4.5V$$
$$V_{+IN} = +D_{IN}\left(\frac{RF}{RF+RG}\right) + V_{-OUT}\left(\frac{RG}{RF+RG}\right)$$
$$V_{+IN} = -4V\left(\frac{1k}{1k+1k}\right) + 4.5V\left(\frac{1k}{1k+1k}\right) = 0.25V$$
$$V_{-IN} = -D_{IN}\left(\frac{RF}{RF+RG}\right) + V_{+OUT}\left(\frac{RG}{RF+RG}\right)$$
$$V_{+IN} = 0V\left(\frac{1k}{1k+1k}\right) + 0.5V\left(\frac{1k}{1k+1k}\right) = 0.25V$$

The ADA4945-1 inputs must be able to swing from 0.25V to 2.25V for this application

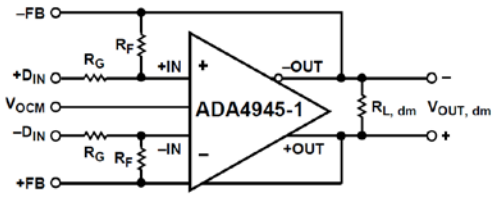

Figure 2 ADA4945-1 Circuit Definitions

3. **Driver Amp (ADA4945-1) Input Common Mode**

Datasheet:

$$-V_S \le V_{CM} \le (V_S - 1.3V)$$

Application:

$$V_{+IN\_min} \le V_{CM} \le (V_{+IN\_MAX})$$

$$0.25V \le V_{CM} \le 2.25V$$

$$V_{+IN\_min} = (V_{+IN\_MAX}) + 1.3V$$

$$+V_S = (V_{+IN\_MAX}) + 1.3V$$

$$+V_S = 2.25V + 1.3V = 3.55V$$

$$-V_S = V_{+IN\_min}$$

$$-V_S = 0.25V$$

4. **Driver Amp (ADA4945-1) Input Common Mode**

Datasheet:
At 1kΩ *Load*
Application:
$V_{+OUT\_min} \le 0.5V, (V_{+\mathrm{OUT}_{MAX}}) = 4.5V$
$-V_{S\_min} = (V_{+\mathrm{OUT}\_min}) - 0.1V$
$-V_{S\_min} = 0.5V - 0.1V = 0.4V$
$+V_S = (V_{+OUT\_MAX}) + 0.1V$
$+V_S = 5V + 0.1V = 4.6V$

5. **Voltage Reference (LTC6655-5) Supply Voltage**

Datasheet:

Operating Voltage:
$(V_{OUT} + 0.5V) \le +V_S \le (13.2V)$
Application:
$V_{OUT} = 5V$
$+V_S OUT_{min}$
$+V_{S\_min}$
Assume 4.5% power supply
(Load, Line, Initial Accuracy,Temp):
$+V_{S\_min}$
Use $+V_S = 5.75V$

If instead V_{REF}=4.096V, power supply could be $+V_S$=5V, with about 2dB in degradation of the SNR.

6. **Driver Amp (ADA4945-1) VOCM set**

$(-V_S + 0.4) \le V_{O_{CM}} \le (+V_S - 1.4V)$
Application:
Application V_{OCM} is inside allowed range.
$-V_S = 0V, +V_S = 5.75V, V_{OCM} = 2.5V$
$(-0 + 0.4) \le V_{OCM} \le (5.75 - 1.4V)$
$(+0.4) \le 2.5V \le (4.35V)$
Application V_{OCM} Scaling:

$$V_{OCM} = \frac{+V_S * R3}{R4 + R3}$$

$$R4 = R3\frac{+V_S - V_{OCM}}{V_{OCM}}$$

Choose R3 = 10kΩ

$$R4 = 10k\Omega\frac{5.75V - 2.5V}{2.5V} = 13k\Omega$$

Design Simulations

Using the **Precision ADC Driver Tool** as shown in *Figure 3*, settling time, noise and THD performance are estimated. The Precision ADC Driver Tool does not currently allow the V_{OCM} center point to be shifted so it is necessary to put a small bias voltage on -Vs for the tool to simulate correctly.

The Precision ADC Driver Tool uses a more conservative 4.8V minimum (+Vs) - (-Vs) supply voltage to implement its calculations, since it is assuming a 4V reference.

The 4V reference is used in the Precision ADC Driver Tool simulation due to this being the actual signal range that is available, when the digital gain compression is enabled, while using a 5V reference. As can be seen, the driver tool warns that the selected ADC driver will significantly degrade the overall noise performance. Also note that RF and RG are the largest contributors to the ADC driver noise. Decreasing RF and RG to 499Ω will increase SNR performance by approximately 1dB. *Table 2* highlights the summary of design goals versus the results obtained from simulated.

Table 2. Design Goal v's Simulation

Parameter	Design Goal	Simulation
SNR	98dBFS	98.7dBFS
THD	-120dB	-123dB

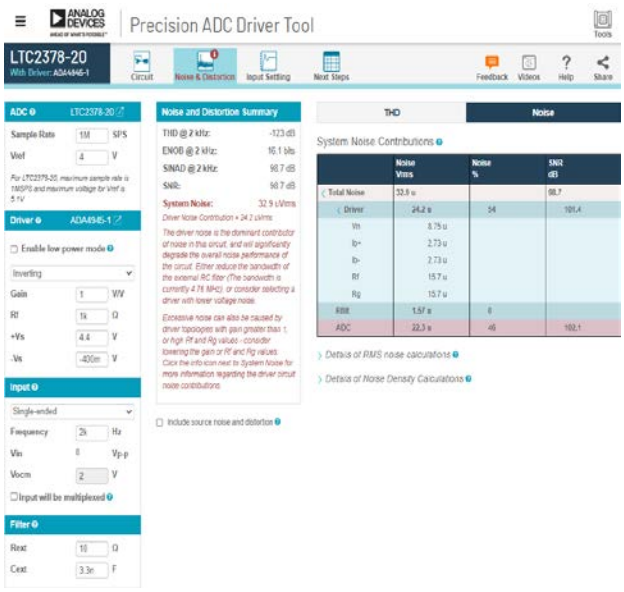

Figure 3. Precision ADC Driver Tool: Noise and THD Results

Measured Results

Looking at the results shown, the ADC SNR performance is 2dB off from datasheet typical of 102dB and THD performance in line with the data sheet typical specification of -125dB, as shown in Figure 4. Table 2 shows a summary of design goals versus measured results.

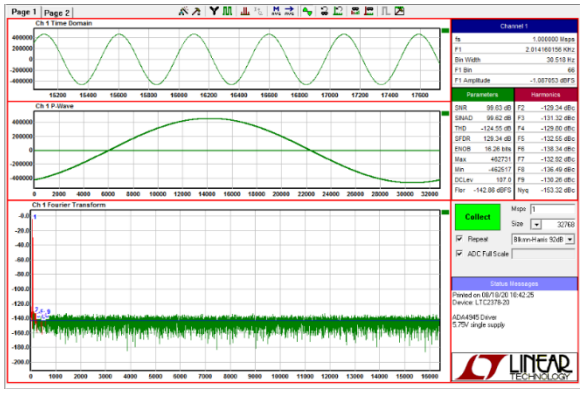

Figure 4. Evaluation Software – Measured Results

Table 3. Design Goal v's Measured

Parameter	Design Goal	Measured
SNR	98dBFS	99.6dBFS
THD	-120dB	-124.6dB

Figure 5 highlights the circuit performance when the supply is taken below 5.2V, It can be seen that the performance degrades rapidly. This data was taken at 25°C, therefore it is important to note that at lower or higher temperatures the performance may start to fall off earlier. Variations in circuit processing may also result in a different voltage where performance starts to degrade.

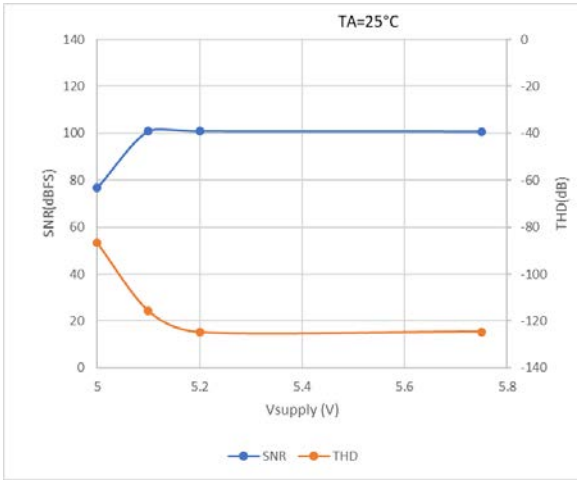

Figure 5. Circuit Performance vs Supply Voltage

References

LTSPICE® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

ADIs, ***Precision ADC Driver Tool*** provides a specialized simulation environment where the engineer can quickly determine the impact of the drive amplifier and R-C filter selection on the overall performance of an ADC signal chain.