KWIK CIRCUIT FAQ

1MHz, Single Supply, Photodiode Transimpedance Amplifier (TIA) Design – by Arthur Roxas

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FAQ: How to design a Transimpedance Amplifier circuit to measure different uric acid concentration samples

Introduction

This KWIK (Know-how With Integrated Knowledge) Circuit application note offers a step by step guide to address a specific design challenge associated with a Transimpedance Amplifier (TIA) design. The TIA circuit shown in Figure. 1 is used as the analog front end in current conversion of near-infrared light intensity applications. This definition-by-example KWIK Circuit FAQ will focus on the measurement of different uric acid concentration samples.

This circuit uses an op amp, configured as a TIA, for amplifying the light dependent current of a photodiode. Also, a small bias voltage, VB, derived from the positive supply, is applied to the op amp's non-inverting input to prevent the output from saturating at the negative supply rail, in the absence of input current. This ensures that the op amp is operating in its linear region of operation, for no light to full light, into the photodiode

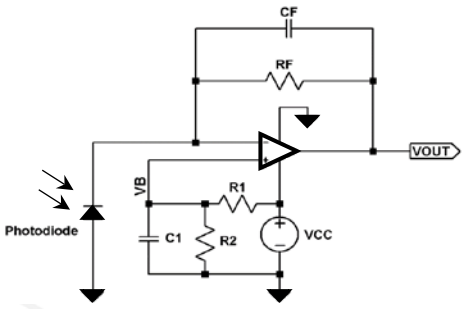

Figure 1. – Photodiode TIA Front End Circuit Design

Design Specifications Example

A high-speed InGaAs PIN photodiode, MTPD1346D-100, by Marktech Optoelectronics, is selected for this design. This photodiode is suitable in detecting uric acid concentrations because it operates at 800 to 1750nm wavelength, in which this compound has maximum absorption. The photodiode is minimally reversed biased and therefore the junction capacitance for diode reverse voltage of zero, VR = 0V will be used for stability calculations. Also, the effects of the dark current on the amplifier output will be neglected. Table 1 lists the photodiode parameters. Table 2summarizes the design target and the simulated design results. To achieve the design performance, Table 3 shows the analysis of the op amp characteristics needed and the specifications of the chosen op amp, AD8615.

Table 1. Photodiode Parameters

Parameter	Conditions	Typ
Junction Capacitance (Cj)	VR = 0V	60 pF
Photodiode Current at 1300nm*1 (IL)	Ee = 1mW/cm2	150 µA

Table 2. Design Target and Simulation Results

Parameter	Target	Simulated
Gain	26.67 kV/A (88.5dB ohm)	26.67 kV/A (88.5dB ohm)
Vout (Input Current = 0 µA)	500 mV	505.465 mV
Vout (Input Current = 150µA)	4.5 V	4.510 V
-3dB Bandwidth	1 MHz	1.3 MHz
Phase Margin	> 45 deg	66.735°
Total Noise	< 200µVrms	204.95uVrms

Table 3. Op Amp Requirements

Parameter	Required	AD8615
Minimum Supply Voltage	< 5	2.7 V
Quiescent Current	< 2mA	1.7 mA
Input Bias Current	1 pA	0.2 pA
Input Offset Voltage	< 100 µV	80 µV
Input Capacitance (CM || DM)	< 20 pF	(6.7 || 2.5) pF
Input Voltage Range	(V-) + 0.5, (V+)	(V-), (V+)
Output Voltage Range	(V-) + 0.1, (V+) - 0.1	(V-) + 0.01, (V+) - 0.01
Gain Bandwidth Product	> 12.5 MHz	24 MHz

Design Description

Transimpedance amplifiers (TIA) are commonly used to amplify the light-dependent current of photodiodes. For a single-supply photodiode amplifier, there are many factors to consider, such as the stability, input and output voltage range limitations, noise, and dc error sources, including input bias current and input offset voltage. This design will present the proper design process for photodiode amplifiers used in single-supply applications.

The basic configuration of a TIA consists of an op amp and a feedback resistor and is shown in Figure 2. The input current is applied to the inverting input and amplified through the feedback resistor, which in turn sets the gain. The output voltage is defined by VOUT=I_N*RF.

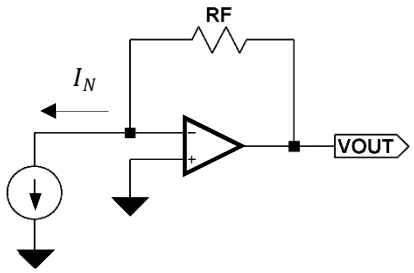

Figure 2. – A Basic Op Amp TIA

The photodiode on this design operates in the "photoconductive" mode shown in Figure 3. This means that exposure to light will cause a reverse current through the photodiode and causes a linear increase in output voltage for each input current. A feedback capacitor, CF, is necessary to maintain stability and compensate for the input capacitances (photodiode capacitance and op amp input capacitance) at the inverting input of the op amp.

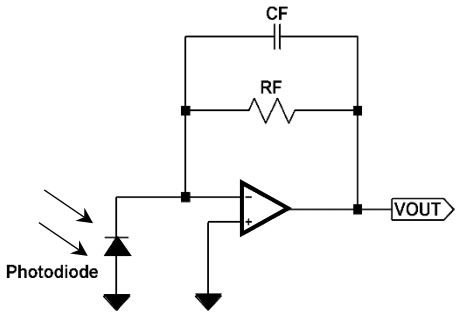

Figure 3. – TIA For Photoconductive Mode

Design Tips / Considerations

1. Consider JFET or CMOS input op amps because they have much lower bias current (pA range) compared to BJT input op amps (nA range). The lower bias current results in reduced dc error voltages and lower input current noise.
2. CF will be necessary and can analytically be designed for op amp stability. The computed value can then be adjusted as a compromise of desired pulse response, settling time, signal bandwidth and noise bandwidth
3. Scale the TIA for desired photodiode current range to be inside the linear operation of the op amp output for fastest response, as to keep the output out of saturation. For single supply applications this requires a VB, as shown in Figure 1. Check for op amp linear operating range under the test conditions for Large Signal Voltage Gain.
4. For a more accurate Output Offset, when I_N=0A, consider generating VB from a DC, filtered Reference Voltage.
5. Use C1 to heavily filter VB from power supply and resistor noise.

Design Procedure

For AC Frequency analyses, poles and zeros will be plotted on a Bode plot. The frequency at which a respective pole or zero occurs will be denoted as fx, where x is a specific letter for an associated pole or zero. f3dB will denote the -3dB frequency point for a single pole, which has -20dB/decade magnitude slope for frequencies greater than f3dB. A zero will have a +20dB/decade magnitude slope for frequencies greater than fx.

Refer to Figure 1 for schematic and for the bode plot refer to Figure 4

1. VB, Output Offset for IN=0A

AD8615 linear operation is from 0.5V to 5V

Choose R1=2.49kΩ, standard value, for reasonable current from VCC. Compute R2 and choose closest standard value.

$$VB = \frac{VCC * R2}{R1 + R2}$$

$$R2 = \frac{VB * R1}{VCC - VB}$$

$$R2 = \frac{0.5V * 2.49k}{5V - 0.5V} = 276.6667\Omega \rightarrow 280\Omega$$

C1 filter capacitor for VB noise filter:

Choose C1=1µF for low f3dB.

$$f_{3dB} = \frac{1}{2\pi\left(\frac{R1 * R2}{R1 + R2}\right) * C1}$$

$$f_{3dB} = \frac{1}{2\pi\left(\frac{2.49k * 280}{2.49k + 280}\right) * 1uF} = 632Hz$$

2. TIA gain:

Photodiode max current, from Table 1, is 150uA.

$$RF = \frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{I_{N(MAX)}}$$

$$RF = \frac{4.5V - 0.5V}{150\mu A} = 26.667k\Omega \rightarrow 26.7k\Omega$$

3. Feedback Capacitor, CF:

After RF is chosen, the closed loop bandwidth and op amp stability are determined by CF. Together RF and CF form a closed loop pole, fp. From Table 1, the -3dB bandwidth is 1MHz.

$$fp = \frac{1}{2\pi * RF * CF}$$

$$CF = \frac{1}{2\pi * RF * fp}$$

$$CF = \frac{1}{2\pi * 26.7k * 1MHz} = 5.96pF \rightarrow 6.2pF$$

$$fp = \frac{1}{2\pi * 26.7k * 6.2pF} = 961.42kHz$$

4. Find 1/β fZ due to Photodiode Capacitance

Cj = photodiode capacitance

$$fz\_pd = \frac{1}{2\pi * RF * Cj}$$

$$fz\_pd = \frac{1}{2\pi * 26.7k * 60pF} = 99.348kHz$$

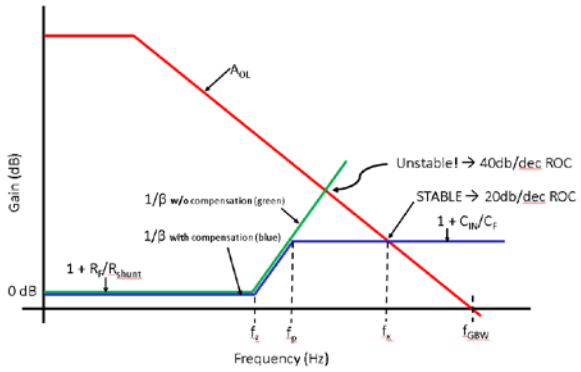

Figure 4. Op Amp Aol with Compensated and Uncompensated 1/β

5. Op Amp Gain Bandwidth:

In Figure 4, the 1/β w/o compensation, shows the effect of the op amp instability, due to f_Z (caused by op amp input and photodiode capacitance). At the intersection of 1/β and A_{OL}, the rate-of-closure (difference between 1/β and A_{OL}) is 40dB/dec ($|A_{OL}$ slope-1/β slope$|$ = |-20dB/dec - +20dB/dec|= 40dB/dec). This first order check of stability requires a 20dB/dec rate-of-closure for stable operation.

fp was set for the desired closed loop bandwidth as minimum of 1MHz. fp causes the final 1/β to flatten out, such that at f_X the final 1/β crosses the A_{OL} curve at a rate-of-closure that is 20dB/dec and, by first order criteria, stable.

To allow for component tolerances and A_{OL} variance over process and temperature, a good design rule is to set fx at: fx ≥ 1.5*fp.

The high frequency 1/β is given by $1+C_{IN}/CF$.

For initial assessment, use $C_{IN} = C_J$.

$$1/\beta\_HiF = 1 + \frac{C_{IN}}{CF}$$

$$1/\beta\_HiF = 1 + \frac{60pF}{6.2pF} = 10.677 \rightarrow 20.57dB$$

The op amp *minimum* unity gain bandwidth, for unity gain stable op amps is computed as follows.

$$GBW\_\min = fx * (1/\beta\_HiF)$$

$$GBW\_\min = (1.5 * fp) * (1/\beta\_HiF)$$

$$GBW\_\min = (1.5 * 1MHz) * (10.667) = 16MHz$$

Unity Gain Bandwidth (min):

$$f_{GBW\_min} = \frac{GBW\_min}{1} = \frac{16MHz}{1} = 16MHz$$

6. Op Amp Parasitics and Op Amp Gain Bandwidth:

As shown in Figure 5, op amps have an input differential capacitance, Cdm, and common mode input capacitances, Ccm+ & Ccm-. For this TIA circuit configuration, Ccm+ is shorted to an equivalent AC ground, through C1 (see Figure 1) for any frequency of interest.

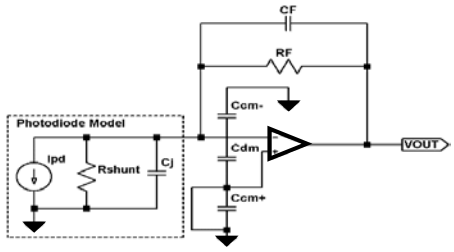

Figure 5

The total input capacitance for this TIA circuit is now C_{IN}=Cj + Cdm + Ccm-.
Final computations using the AD8615 Op Amp Parasitics are as follows (refer to Figure 4 for pole/zero locations):
AD8615 Ccm=6.7pF, Cdm=2.5pF, f_{GBW}=24MHz
Cj=60pF, CF=6.2pF, RF=26.7k.

$$fz = \frac{1}{2\pi * RF * (CF + C_{IN})}$$

$$fz = \frac{1}{2\pi * 26.7k * (6.2pF + (6.7pF + 2.5pF + 60pF))}$$

$$fz = 79.056kHz$$

$$fx = \frac{CF}{C_{IN} + CF} * f_{GBW}$$

$$fx = \frac{6.2pF}{(6.7pF + 2.5pF + 60pF) + 6.2pF} * 24MHz$$

$$fx = 1.97MHz$$

$$\frac{fx}{fp} = \frac{1.97MHz}{961.42kHz} = 2.049$$

Note that fx/fp ≥ 1.5 ensures stability design margin for Aol frequency change, with process and temperature.

7. Noise Analysis

The op amp noninverting input is heavily bypassed by the 1uF capacitor so resistor noise and power supply noise will be assumed to be negligible and not included in the noise analysis. The remaining dominant noise sources are the op amp voltage noise and current noise and the feedback resistor, RF. The shunt resistor, internal to the photodiode, will also be included but shown to be a negligible contributor. Refer to Table 4. TIA Noise Calculation.

For the AD8615:

$$VN = \frac{10nV}{\sqrt{Hz}}, IN = \frac{0.05pA}{\sqrt{Hz}}$$

Noise Bandwidth, BWN, for a single pole roll-off:

$$BW_N = 1.57 * fx = 1.57 * 1.97MHz = 3.09MHz$$

For noise computations:

$$\sqrt{BW_N} = \sqrt{1.57 * fx} = \sqrt{1.57 * 1.97MHz}$$

$$\sqrt{BW_N} = 1758.66\sqrt{Hz}$$

Total referred-to-output noise:

$$V_{N\_RTO} = \sqrt{V_N{}^2 + V_{N\_RF}{}^2 + V_{N\_IN}{}^2 + V_{N\_Rshunt}{}^2}$$

$$V_{N\_RTO} = \sqrt{(213.88\mu Vrms)^2 + (36.98\mu Vrms)^2 + (2.348\mu Vrms)^2 + (0.1911\mu Vrms)^2}$$

$$V_{N\_RTO} = 217.07\mu Vrms$$

8. Final Tuning of the TIA Circuit:

After the final selection of the op amp, the initial CF value may want to be adjusted for optimum signal closed loop bandwidth versus stability. Input capacitances will be op amp dependent, and therefore partly determine the design trade-offs for signal bandwidth versus noise bandwidth versus stability.

Table 4. TIA Noise Calculation

Noise Source	Voltage Noise Formula	Voltage Noise Calculation	Voltage Noise at 27°C (~300°K)
Op Amp Voltage Noise **Assume dominant noise contribution is at higher frequencies.**	$V_N * \left(1+\frac{C_{IN}}{CF}\right) * \sqrt{1.57\,fx}$	$10\frac{nV}{\sqrt{Hz}} * \left(1+\frac{69.2pF}{6.2pF}\right) * 1758.66\sqrt{Hz}$	$V_N = 213.88\mu Vrms$
Feedback Resistor	$\sqrt{4kTR_F * 1.57\,f_x}$	$\sqrt{4\left(1.38x10^{-23}\,J/K\right)(300K)(26.7k) * 1758.66\sqrt{Hz}}$	$V_{N\_RF} = 36.98\mu Vrms$
Op amp Current Noise	$I_N * R_F * \sqrt{1.57\,fx}$	$0.05\frac{pA}{\sqrt{Hz}} * 26.7k * 1758.66\sqrt{Hz}$	$V_{N\_IN} = 2.348\mu Vrms$
Photodiode Shunt Resistance Assume Rshunt=1 GΩ	$Rshunt\_noise * \frac{R_F}{R_{shunt}} * \sqrt{1.57\,fx}$	$\sqrt{4\left(1.38x10^{-23}\,J/K\right)(300K)\left(1\times10^{9}\right)} * \frac{26.7k}{1\times10^{9}} * 1758.66\sqrt{Hz}$	$V_{N\_Rshunt} = 0.1911\mu Vrms$

Design Simulations

1. DC Transfer Function:

Figure 6 is the LTspice test circuit for the DC Transfer Function, using standard resistor values. The results of the test are shown in Figure 7. For I_N=0A, Vout=0.50546509V and for I_N=150uA, Vout=4.5104647V with Vout/I_N=26.67kV/A.

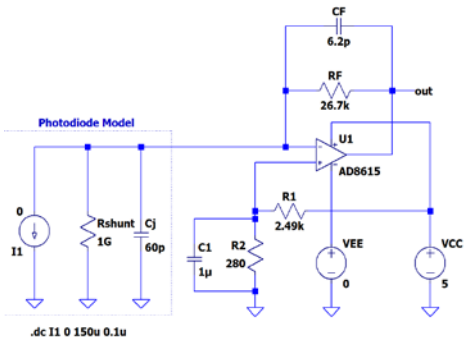

Figure 6. DC Transfer Test Circuit

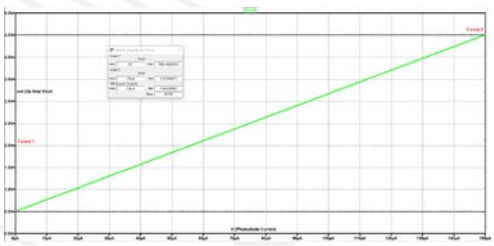

Figure 7. DC Transfer Simulation Results

2. AC Transfer Function:

Figure 7 is the LTSPICE test circuit for the AC Transfer Function, using standard component values. The results of the test are shown in Figure 8. The simulated fp (measured at -3dB from low frequency gain) is 1.3MHz, which is slightly greater than the design target bandwidth of 1MHz.

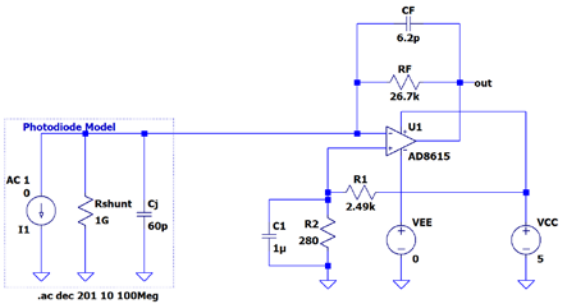

Figure 8. AC Transfer Test Circuit

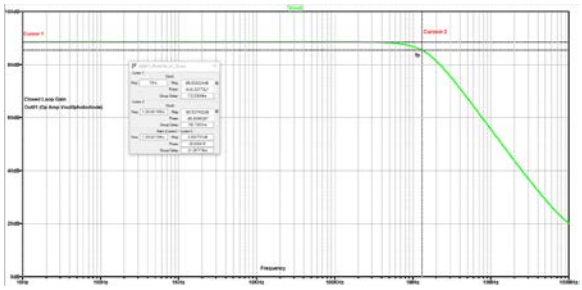

Figure 9. AC Transfer Simulation Results

3. Loop Gain Analysis:

Figure 10 is the LTspice Test Schematic for Loop Gain with Compensation. Figure 11is the LTspice Schematic for Loop Gain without Compensation. Since the loop gain circuit uses an inductor, LT, to create an open between VFB and VinM for any frequency of interest, we must add in externally the appropriate op amp common mode capacitance, Ccm, and differential mode capacitance, Cdm. These capacitances are necessary to be included for the effects of 1/Beta in the circuit. Figure 12shows the A_{OL} and $1/\beta$ plots for both compensated and uncompensated design. Figure 13 shows the Compensated Loop Gain with loop gain phase margin at 66.7349 degrees for loop gain at 0db at 2.179MHz

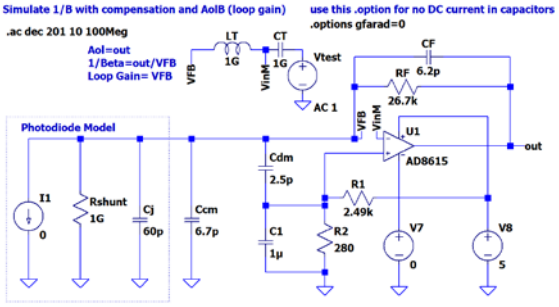

Figure 10. Test Schematic for Compensated TIA

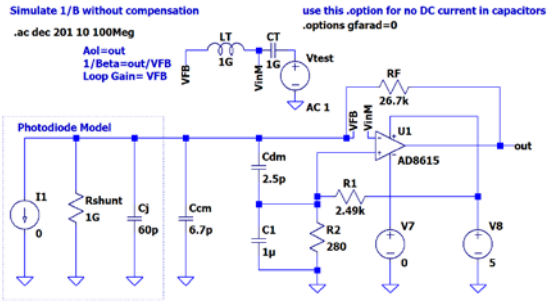

Figure 11. Test Schematic for Uncompensated TIA

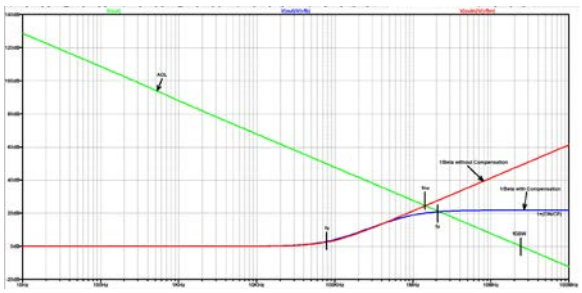

Figure 12. Aol and 1/β: Compensated and Uncompensated

Simulation Results

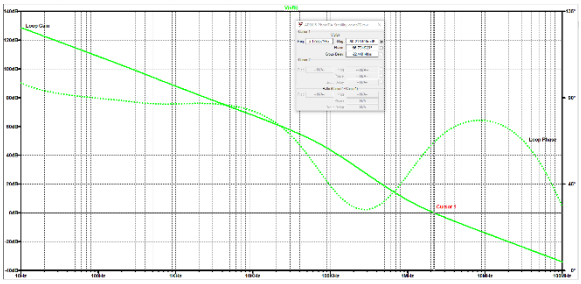

Figure 13. Compensated TIA Loop Gain Simulation Results

4. Transient Analysis:

Figure 14 is the LTspice Test Schematic for Compensated Transient Response. Figure 15is the simulation results for the Transient analysis. The photodiode current, I1, was given a fast 1ns rise/fall time to disturb the TIA circuit to look for excessive overshoot and ringing, which would indicate marginal stability.

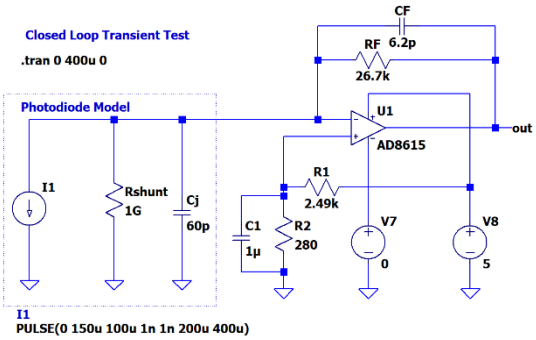

Figure 14. Test Circuit for Fast Transient

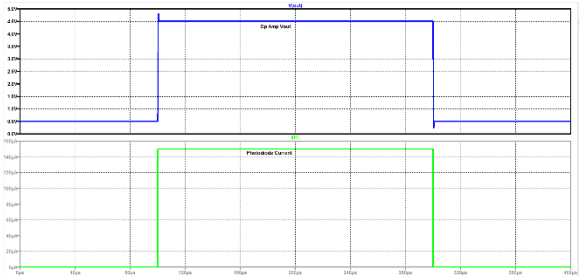

Figure 15. Fast Transient Simulation Results

5. Noise Analysis:

Figure 16 is the LTspice Test Schematic for Noise Analysis. Figure 17is the Noise Analysis results. The question arises as to what integration bandwidth to use for predicting RMS noise from the simulation. The black line shown in Figure 17 is a
-20dB/decade slope of spectral noise density. Beyond about 2MHz we see that spectral noise density declines as a decade reduction in noise voltage per decade of frequency. This implies the integrated noise (or Total Noise or RMS Noise) will begin to become constant. To see the RMS Noise in LTspice, over a desired bandwidth, right click on the x-axis and scale for the desired frequency integration range. Then, do a CTRL+Left Mouse Click, while hovering over the plot waveform name, here V(onoise), and a pop-up window will display the frequency interval of the integration and the Total RMS noise. The Total RMS noise measured for 1Hz-200MHz is shown as 204.95uVrms. For 1Hz-20MHz it is 197.27uVrms and for 1Hz-2MHz it is 119.68uVrms. As a noise simulation rule, we see if we use the spectral roll-off frequency, estimated here as 2MHz, times 10 for the upper frequency integration bandwidth we will capture most of the RMS noise. The RTO noise simulation is then 204.95uVrms. Total RTO noise calculation using Table 4 was 217.07uVrms, and the design target was <200uVrms. This is within a noise simulation versus hand analysis calculation design rule of +/-10%. For accurate noise and stability simulations any macromodel should be verified, by simulation, to match the datasheet for correct Aol, Input Voltage Noise, Input Current Noise, Input Capacitances, and Closed Loop Output Impedance. Since the datasheet is used for the hand analysis, there will be poor correlation if the macromodel does not match the datasheet.

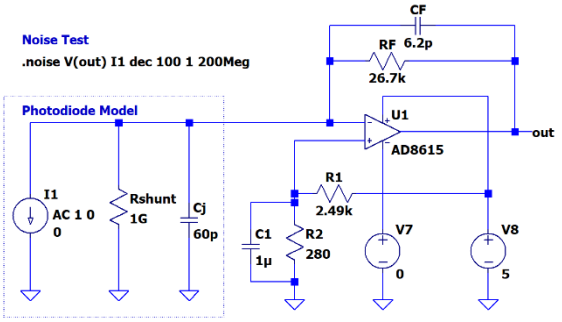

Figure 16. Test Circuit for Noise

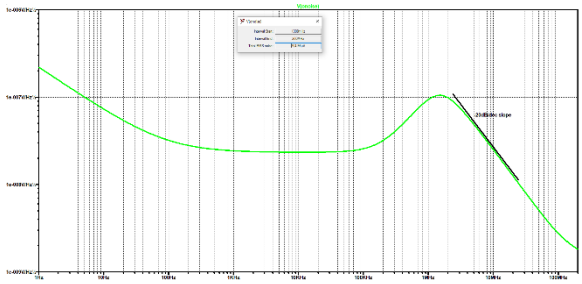

Figure 17. Noise Simulation Results

Design Devices

Table 5. Op Amps

Part Number	Vos (V) typ	Ibias (A) typ	Input Capacitance (Ccm | Cdm) (pF) typ	GBP (Hz) typ	Vnoise (V/rt-Hz) typ	Inoise (A/rt-Hz) typ	Iq/Amp (A) typ	Input Voltage Range (V)	Output Voltage Swing (V)	Vs span min/max (V)
AD8615	80µ	0.2p	6.7 | 2.5	24M Linear Vout = 0.5 V to 5V	10n @ 10kHz	0.05p	1.7m	(V+) to (V-)	(V+) –0.01 V(-) – 0.01	2.7 V 5.5 V

References

[1] ***LTSPICE***
LTspice® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

[2] ***Photodiode Circuit Design Wizard***
Use Photodiode Wizard to design a transimpedance amplifier circuit to interface with a photodiode. Select a photodiode from the library included in the tool or enter custom photodiode specifications. Quickly observe tradeoffs.

[3] ***Practical Design Techniques Sensor Signal Conditioning – Section 5***
By Walt Kester, Scott Wurcer and Chuck Kitchin, 1999. This book is a compete sensor signal conditioning manual including bridge circuits, strain, force, pressure, flow measurements. high impedance sensors, position and motion sensors, temperature sensors. Fundamentals of amplifiers and ADCs for signal conditioning. A section on hardware design techniques relating to sensor conditioning circuits gives important PC board layout guidelines.

[4] ***Does Your Op Amp Oscillate?***
Application note on op amp stability including effects of input capacitance.

[5] ***Stability 101: Parasitic Capacitance in Operational Amplifiers***
Video where Analog Devices' Matt Duff explains why parasitic capacitance at the inverting terminal of an operational amplifiers (op amp) can cause instability.

[6] ***Stability 101: Bode Plots and Operational Amplifiers***
Video where Analog Devices' Matt Duff explains how to use Bode Plots to quickly determine whether an operational amplifiers (op amp) circuit will be stable.

[7] ***Stability 101: Loop Gain in Operational Amplifiers***
Video where Analog Devices' Matt Duff explains the key term, loop gain, in determining whether an operational amplifier (op amp) circuit is stable.

Acknowledgements

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Tim Green, Senior Applications Engineer, Linear Products Group, Instrumentation and Precision Technology
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Paul Blanchard, Product Applications Manager, Instrumentation and Precision Technology