KWIK CIRCUIT FAQ

High Current Voltage Reference for Sensor Excitation

by Andy Li

FAQ: How to build a high current voltage reference for sensor excitation

Introduction

There are many applications that use Wheatstone Bridge Sensors, such as flowmeters, and pressure measurement sensors. A high current buffer for a precision reference source is often needed, as a bridge sensor excitation voltage. The buffer must be precise and stable, when driving the sensor and its decoupling capacitor. (Refer to Figure 1)

This KWIK (Know-how With Integrated Knowledge) Circuit application note offers a step-by-step guide to address a specific challenge of designing a precision excitation voltage source, with a high current output. For a given set of application circuit requirements, it illustrates how these are addressed, using generic formulae, and makes them easily scalable to other similar application specifications.

Design Specifications

For this example, the design requirement specification of the precision excitation voltage is shown in Table 1. It will be designed to drive a 120Ω Wheatstone Bridge type strain gauge.

Table 1. Key Design Specifications

Specification	Design Requirement
Output Voltage	+4.096V@35mA
Load Resistor	120Ω
Load Capacitor	100nF
Power Supply	+5V
Noise (0.1Hz to 10Hz)	<10uVpp
Temperature Coefficient	<20ppm/°C
Bandwidth	1kHz
Slew Rate	0.01V/us
Operating Temperature	-40°C~+125°C

The following design concerns for first-pass PCB design will be addressed: capacitive load stability compensation, the temperature effects of the PNP Transistor, power dissipation in the PNP transistor, accuracy, load transient response, and DC design of the topology for performance optimization.

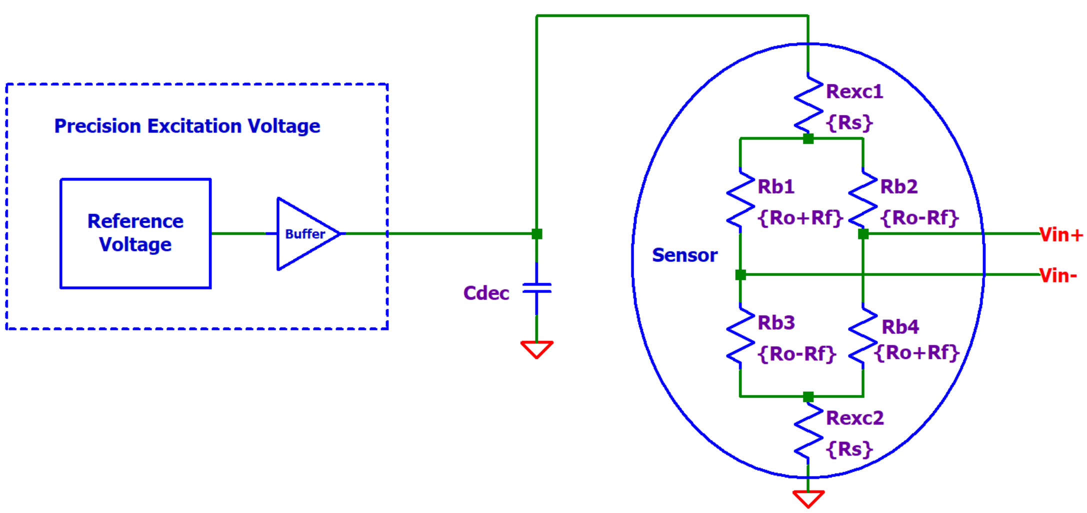

Figure 1. The Basic Diagram of Sensor Excitation

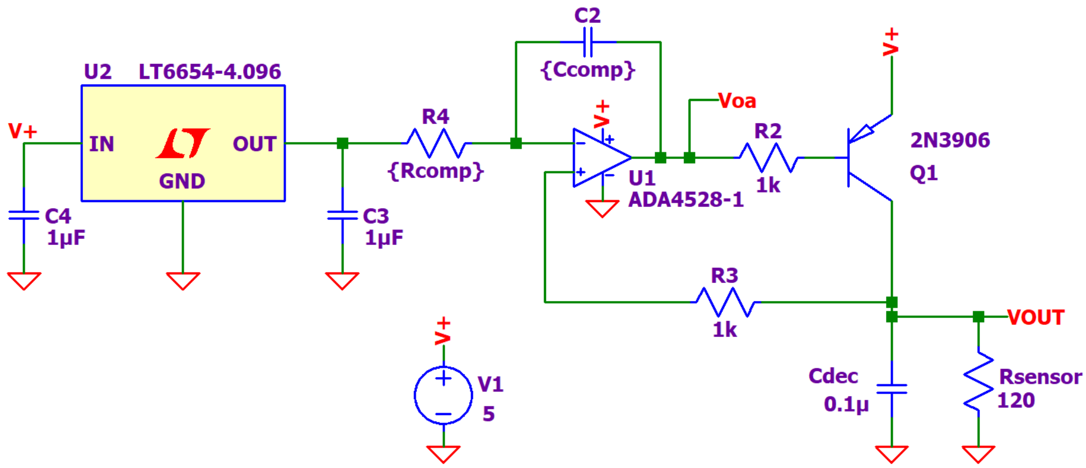

Figure 2. Reference Voltage and Buffer

Design Description

The circuit of the voltage reference and buffer is shown in Figure 2. A voltage reference of 4.096V is used for the signal chain ADC and will be used for the reference voltage to drive the sensor. To drive the 120Ω strain gauge bridge requires about 35mA, at 4.096V. On a 5V single supply application, most op amps cannot provide 35mA at 4.096V and stay in the linear output swing of the op amp. Many precision references cannot provide the 35mA for the strain gauge excitation, along with other ICs that need to use the reference. Enter a high current, single supply, accurate reference buffer. A zero-drift op amp and one small PNP external transistor will provide an architecture that can operate the op-amp in the linear region and provide an accurate 4.096V, at 35mA, to the strain gauge.

Design Tips/Considerations

1. The op amp driver's specifications, including Power Supply, Temperature Coefficient, and Noise guide towards a selection of a zero-drift op amp, with a single power supply, as the error amplifier. Due to the amplifier's input and output voltage, which are close to the power rail, a rail-to-rail input and output op amp is also necessary for the application.

2. The high current reference buffer may operate from a 5V power supply, assumed to have a 10% tolerance. So the power supply may be as low as 4.5V. A commonly used architecture of the buffer is an Emitter-Follower, as shown in Figure 3. The Vbe of an NPN is about 0.6V and the power supply is 4.5V. And so the Vout of the op-amp can't output 4.096V to equal the Input voltage.

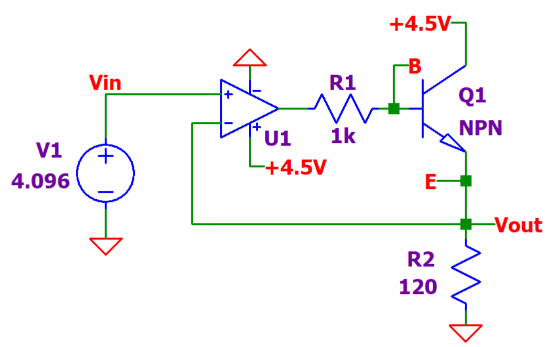

Figure 3. Emitter-Follower Architecture

So the better topology is the Common-Emitter Amplifier architecture, which uses a PNP, as shown in Figure 4. In operation, the output of U2 will get to about 3.9V, which is less than the power rail of 4.5V. And the Vce saturation voltage is well below 0.6V. For example, the Vce(sat) of a 2N3906 is about 200mV, when the Ic is 100mA. So, the Vout of the buffer can theoretically output the same as the input 4.096V. Note the feedback connection of the op amp is at the non-inverting input, because the Common-Emitter amplifier's gain inversion introduces a 180° phase shift. If it connects to the inverting input, the phase will shift 180° again, and the control loop of the buffer becomes positive feedback, due to a total

360° phase shift. So the feedback network has to connect to the non-inverting input of the op amp for negative feedback.

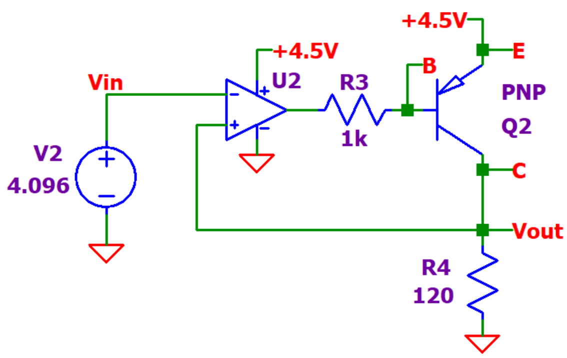

Figure 4. Common-Emitter Amplifier Architecture

3. The loop is unstable if it is left as in Figure 4, with just the negative feedback for large signal. We have to add a compensation network Rcomp and Ccomp for stability (as shown in Figure 5).

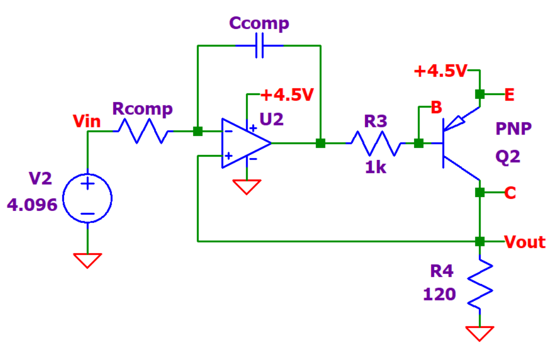

Figure 5. Compensation Network for the Loop

Design Procedure

1. Select the key parts according to the specification requirements of the driver. The max temperature coefficient of LT6654A-4.096 as the voltage reference is 10ppm/°C, less than the requirement. And the typical noise is about 8.2uVp-p which is also less than the requirement. We choose ADA4528, a zero-drift and rail-to-rail Op-Amp with ultra-low noise as the error amplifier. A 2N3906 is selected as the power stage for driving 120Ω.
2. Analyze why the control loop is unstable without compensation by Rate-of-Closure, first order stability check.
3. Add a compensation network, Ccomp, to create Beta- feedback path and verify the stability, by using the “Double-L Break” simulation method.

Design Simulations

1. Simulate the DC operating point and calculate the PNP’s hFE

We must check that the loop of the buffer (shown in Figure 6) is effective by a DC operating point simulation. By the DC Operating Point Analysis, a “.op” directive in LTspice, we can get the Operating Point list, including all the nodes DC voltage and current as shown in Figure 7. The Vout is 4.096V equal to the Vin, so the control loop is verified as a negative feedback loop.

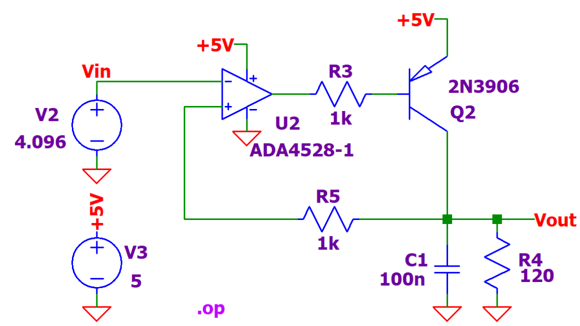

Figure 6. The Buffer without Compensation

* C:\1-MyWork\KWIK Circuits\35mA Ref Buffer\Simulation\...

--- Operating Point ---

V(vin):	4.096	voltage
V(n002):	4.24436	voltage
V(n001):	4.1519	voltage
V(vout):	4.096	voltage
V(n003):	4.096	voltage
V(+5v):	5	voltage
Ic(Q2):	-0.0341333	device_current
Ib(Q2):	-0.000184934	device_current
Ie(Q2):	0.0343183	device_current
I(C1):	4.096e-19	device_current
I(R3):	0.000184934	device_current
I(R4):	0.0341333	device_current
I(R5):	9.18346e-11	device_current
I(V2):	7.96226e-11	device_current
I(V3):	-0.0357227	device_current
Ix(u2:1):	9.18346e-11	subckt_current
Ix(u2:2):	-7.96226e-11	subckt_current
Ix(u2:3):	0.00140448	subckt_current
Ix(u2:4):	-0.00158941	subckt_current
Ix(u2:5):	0.000184934	subckt_current

Figure 7. DC Operating Point list

According to the Ib(Q2) and Ic(Q2), from our LTspice simulation, by a .op analysis, we can calculate the

2N3906's hFE is 184.57. The calculated value of 2N3906's hFE is within the parameter range in its datasheet, using Ic=10mA as a guide, as shown in Figure 8, excerpted data from 2N3906 datasheet.

Conditions	hFE Min	hFE Typ
Ic=0.1mAdc, Vce=1.0Vdc	60	---
Ic=1.0mAdc, Vce=1.0Vdc	80	---
Ic=10mAdc, Vce=1.0Vdc	100	300
Ic=50mAdc, Vce=1.0Vdc	60	---
Ic=100mAdc, Vce=1.0Vdc	30	---

Figure 8. 2N3906's hFE (DC Current Gain)

2. *Simulate the stability of the buffer circuit without compensation network*

The buffer output always drives a bypass capacitor which is normally 100nF except for the 120Ω load. And we also need a 1k resistor to protect the ADA4528 +input from any real-world voltage transient disturbances and provide a breakpoint in the 1/Beta signal with the final compensation capacitor. The buffer circuit is shown in Figure 9 for a Transient Analysis.

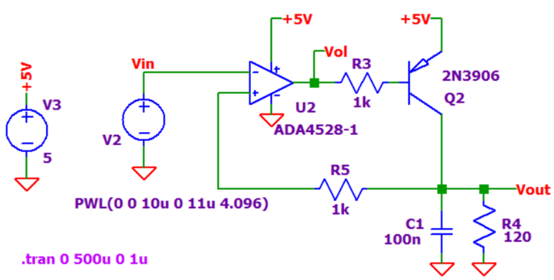

Figure 9. Step Response of the Buffer Circuit

First, perform LTspice Transient analysis with a step response for checking the buffer's stability. It is easy to find that the loop oscillates as shown in Figure 10. We can also find the op-amp output oscillates and not only the Vout of the buffer.

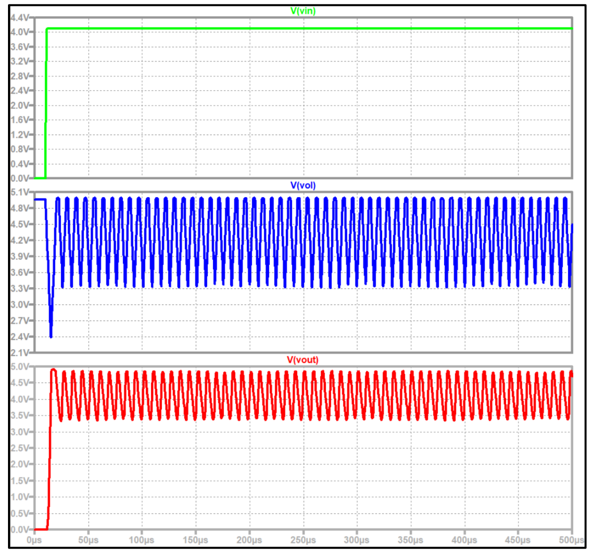

Figure 10. The Simulation of the Step Response

Second, analyze the 1/Beta and Aol with Rate-of-Closure in an AC simulation in more detail. (Aol is Op-Amp's open loop gain, and 1/Beta is the reciprocal of the feedback coefficient, Beta=Vol/VFB.)

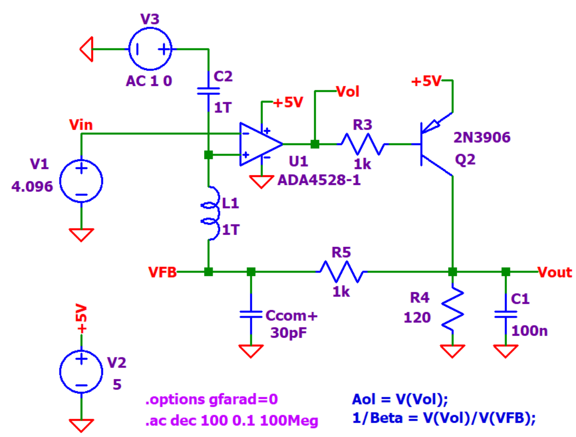

Figure 11. Open Loop Analysis of the Buffer

As shown in Figure 11, break the closed loop op-amp circuit at the +input, which is the feedback node by putting in a large value inductor, L1. And then inject an AC source, V3, through a large capacitor, C2, into the +input. Since this technique will isolate the internal $Ccom+$ of ADA4528, add the $Ccom+$ onto the VFB node. At last, we can get the Aol and 1/Beta curves according to the equations $Aol = V(Vol)$, $1/Beta = V(Vol)/V(VFB)$ in LTspice as shown in Figure 12.

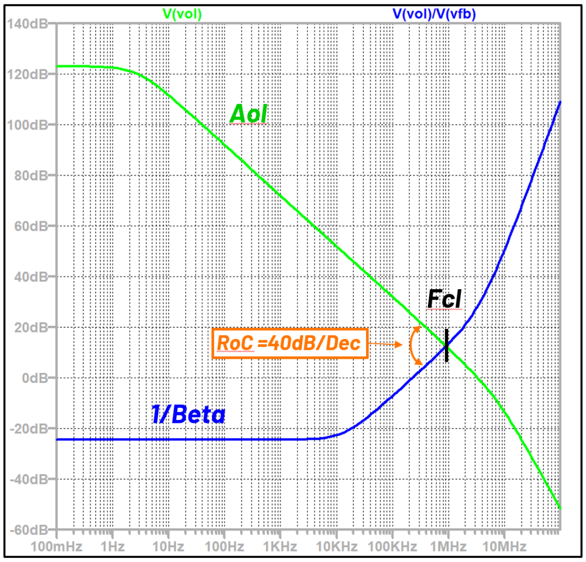

Figure 12. Aol and 1/Beta without compensation

As shown in Fig 12, we can find the Rate-of-Closure is 40dB/Dec at Fcl, which indicates the loop is unstable.

3. Design the compensation network for worst case

The 2N3906's hFE, R4, and C1 (shown in Figure 11) dominate the transfer function of the 1/Beta. It should be noted that the hFE of 2N3906 varies greatly with the temperature as shown in Figure 13, excerpted data from the 2N3906 datasheet. When the Ic is 34mA, the hFE is about 180 at 25°C, 250 at 150°C, and 90 at -55°C. So, we have to consider designing the compensation network for the worst case hFE variance.

Conditions	hFE Typ
Vce=1V, Ic=34mA, Tj= 25C	180
Vce=1V, Ic=34mA, Tj= 150C	250
Vce=1V, Ic=34mA, Tj= -55C	90

Figure 13. 2N3906's hFE over Temperature

Use a test circuit (shown in Figure 14) to verify the hFE of 2N3906 macromodel in LTspice and check whether the simulation result matches the datasheet's data. The Vb biasing the base of 2N3906 is 0.3V, and another current source Ie drives the emitter. This method can bring the Vce of 2N3906 close to 1V which equal the testing condition. The Ie changes linearly from 0.1mA to 200mA with the DC Sweep simulation command. We can capture the hFE curve according to the formula $hFE = Ic/Ib$ and find the simulated value of the hFE is about 184 which is close to the datasheet's parameter when $Ic = 34mA$ at 25°C as shown in Fig 15.

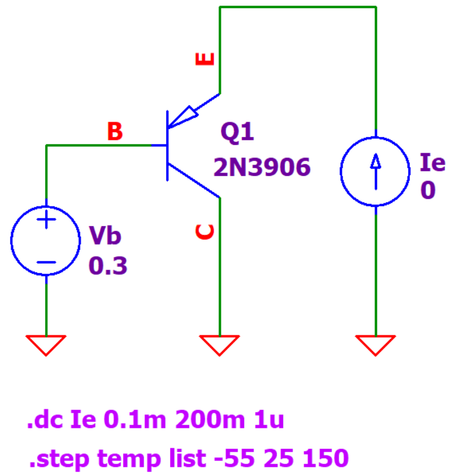

Figure 14. hFE Test Circuit

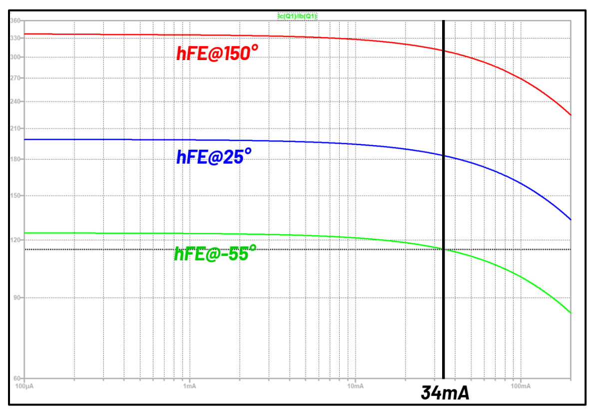

Figure 15: The Simulation Results of the hFE

We can capture the different hFE curves at different temperatures with the LTspice directive ".step temp list <temp1> <temp2> <temp3>" as shown in Figure 14. This command can also help us to capture Aol and 1/Beta frequency response curves at different temperatures in the open loop with AC simulation, as shown in Figure 16. We find the worst case is at -55°C, because the Unity-Gain Crossover Frequency of the 1/Beta @ -55°C is less than other 1/Beta curves. That means the compensation network we designed needs to be applicable in the worst case of -55°C. Note that this over temperature simulation sweep is only valid for the 2N3906, since most op amp macromodels do not model Aol change, with Global Simulation Temperature.

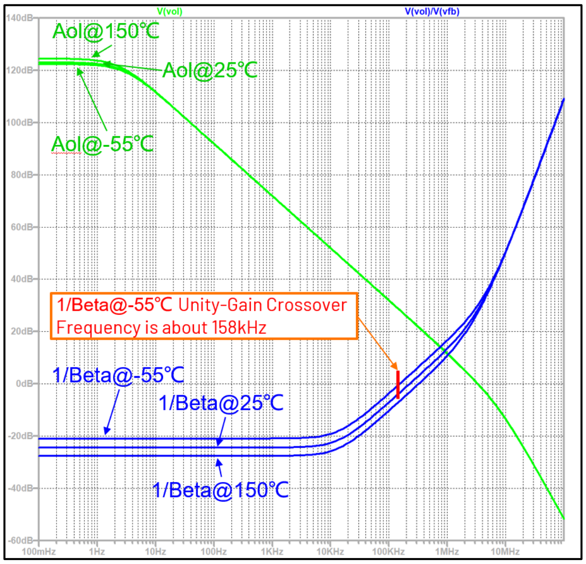

Figure 16. Aol and 1/Beta at different temperatures

In Figure 17 the 1/Beta network, whose feedback to the IN+ of Op-Amp is labeled 1/Beta+, and the compensation network, whose feedback to the IN- is labeled 1/Beta-. The 1/Beta- will provide another feedback path to ensure the loop stability. And the total 1/Beta equals (1/Beta-) – (1/Beta+).

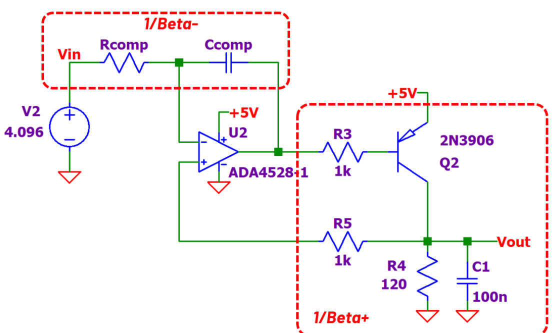

Figure 17: 1/Beta+ and 1/Beta- Circuit

As shown in Figure 18, analyze the buffer topology without compensation and propose a solution using two feedback paths. The other feedback path is the 1/Beta-. But how does one find the correct compensation parameters? We observe that we want to get a 20dB/dec Rate-of-Closure at Fcl ,which is the interception of ADA4528 Aol and total 1/Beta curves. The $Rcomp$ and $Ccomp$ determine the zero of the 1/Beta-. We must make sure the zero frequency ($Fz1$) of the 1/Beta- is far less than the unity-gain crossover frequency of the curve labeled 1/Beta+@-55°C. In the simulated circuit, the unity-gain crossover frequency of the 1/Beta+ is about 158kHz. We can set the Fz1 at 50kHz which is far less than 158kHz. According to the formula $Fz1 = 1/(2\pi * Rcomp * Ccomp)$, we can select 1k and 3.3nF as $Rcomp$ and $Ccomp$ for the frequency point. Since $Ccomp$ is a short at high frequency, then 1/Beta- will go to 1 or 0dB. With two feedback paths, 1/Beta+ and 1/Beta-, combining the lowest 1/Beta path will dominate, since it is the largest Beta path, meaning more voltage is fed back from the op amp output to its input.

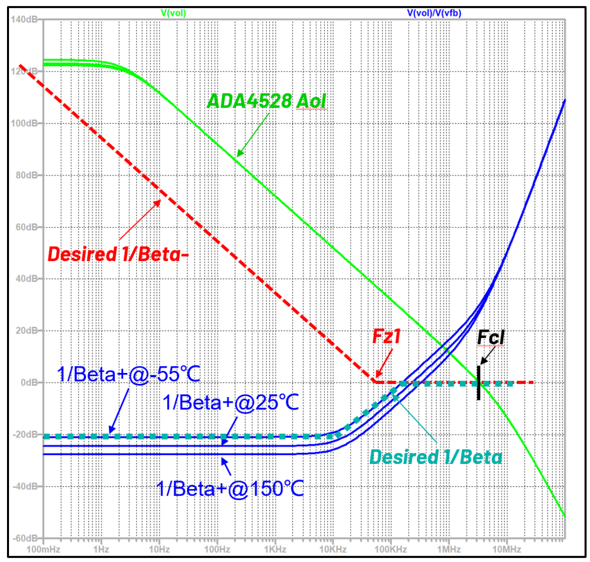

Figure 18: Analysis: Aol&1/Beta+, 1/Beta-

So, the calculated compensation final circuit is shown in Figure 19.

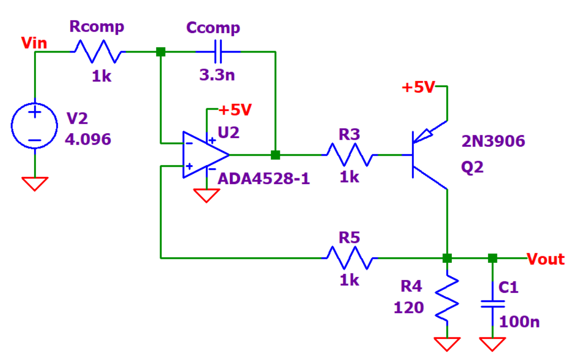

Figure 19: The Calculated Compensation Circuit

4. *Verify the final buffer circuit*

First, we can use the "Double-L Break" method to analyze the stability according to the Rate-of-Closure criteria in an open loop AC simulation. The loop of the buffer includes two feedback paths, one feedback to the IN+ of the Op-Amp and another feedback to the IN-. As shown in Figure 20, the “Double-L Break” means that two large inductors separately break the two feedback loops for capturing the 1/Beta+ and 1/Beta- curves. Since 1/Beta equals (1/Beta-) – (1/Beta+), use a Voltage Dependent Voltage Source (E1) to achieve the calculation. It is important to add the internal common mode and differential capacitances of ADA4528 into the two feedback nodes, since they have been isolated by large inductors for any frequency of interest. Inject an AC source through a 1T capacitor between the IN+ and IN-. The IN+ and IN- nodes also need to add two large resistors connected to GND separately, to avoid a floating excitation source in LTspice. With one LTspice AC Analysis Run, we can generate all curves of interest as indicated by the equations detailed in Figure 20.

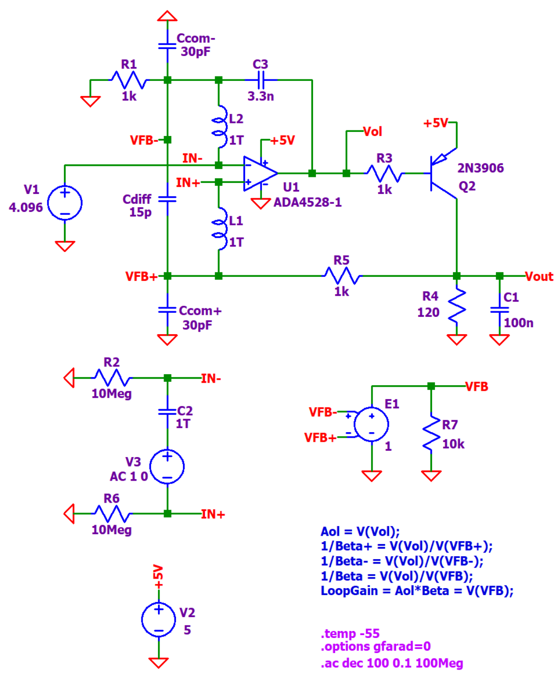

Figure 20: "Double-L Break" Method

In Figure 21 the ADA4528 Aol curve and 1/Beta+, 1/Beta-, and 1/Beta plots are shown. Also, the 1/Beta curve is as predicted, and a 20dB/dec Rate-of-Closure at Fcl illustrates the loop is stable.

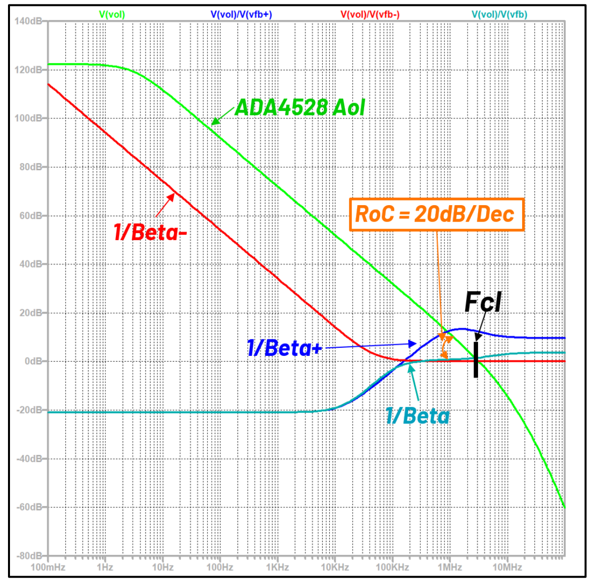

Figure 21: 1/Beta, 1/Beta-, 1/Beta+ and Aol Plots

We can also use Loop Gain magnitude and phase plots to recheck the stability. If the phase margin is more than 45° at unity gain frequency, we can consider the loop stable. In Figure 22 the phase margin of the Loop Gain is about 51° at unity gain frequency, so the loop is stable.

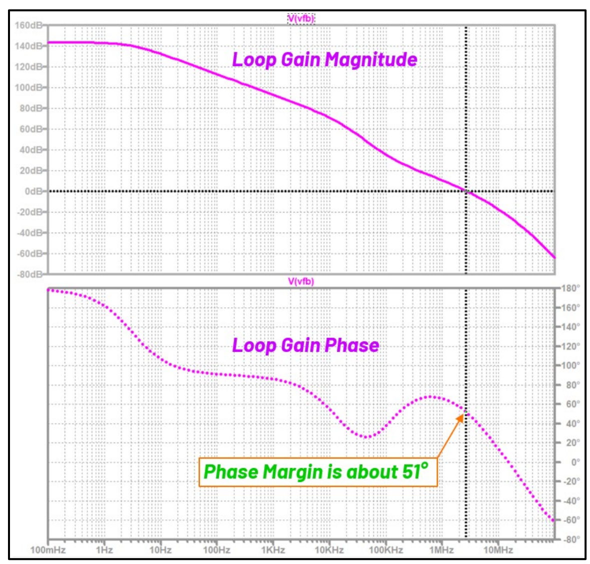

Figure 22: Loop Gain Magnitude and Phase Plot

Second, verify the stability with step response in a Transient Analysis. The overshoot and ringing of the step response will illustrate if the loop is unstable. As shown in Figure 23, inject a Pulse voltage source at the Vin of the buffer circuit and test the response at Vout.

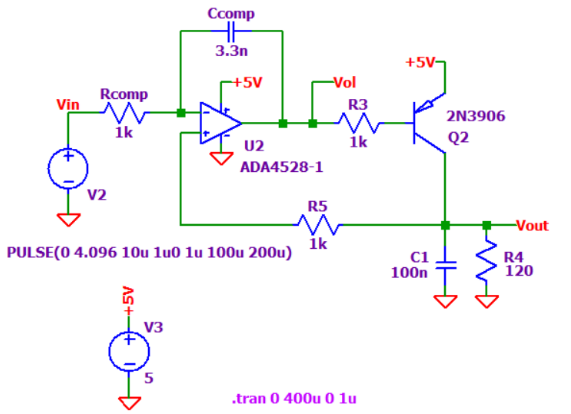

Figure 23: Transient Stability Test Circuit

The simulation results shown in Figure 24, from LTspice Transient Analysis of the step response, show that Vout exhibits no excessive overshoot or ringing which is what we would predict from our Loop Stability analysis. There are some overshoots and undershoots at Vol which is the op-amp output. These are due to the output impedance of the op-amp and don't affect the stability. But if you find there are some rings at Vol, it predicts the loop is unstable.

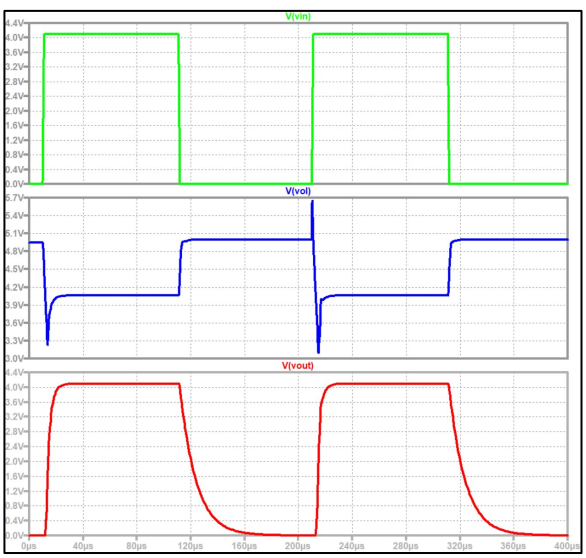

Figure 24: Transient Stability Test SPICE Result

Measured Results

1. Step Response Test without Compensation

Figure 25 shows the real-world PCB implementation of the High Current Voltage Reference for Sensor Excitation.

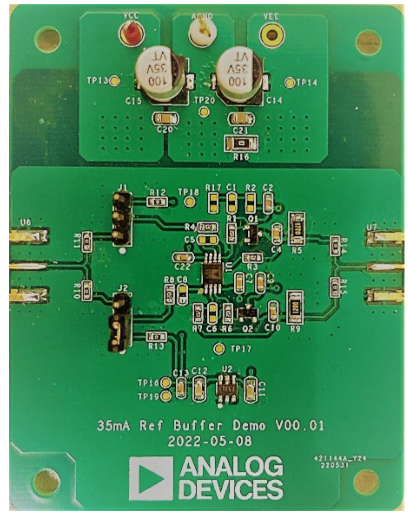

Figure 25: The Practical Circuit

The step response results of a Pulse wave excitation are shown in Figure 26. The buffer circuit, without compensation, is unstable as predicted by the simulation results.

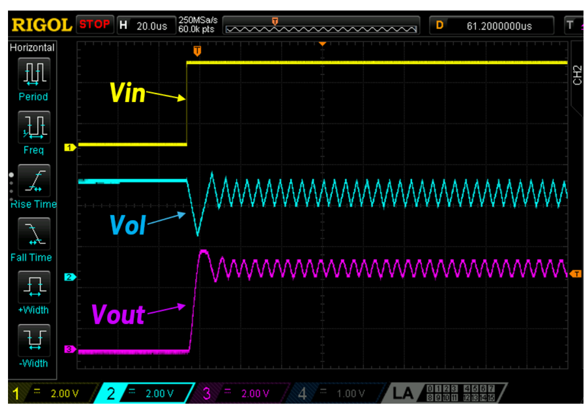

Figure 26: Step Response Result without Compensation

2. Step Response Test with Compensation

After adding the compensation network to the lab circuit, a transient stability test shows the results in Figure 27. It's stable! The buffer circuit is shown to be stable from analysis to LTspice simulation and finally to the real-world PCB implementation.

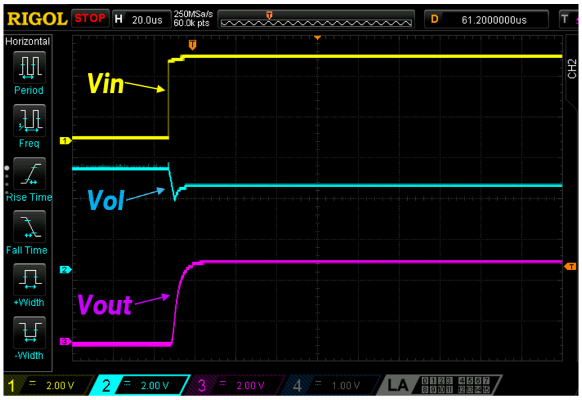

Figure 27: Step Response Result with Compensation

Design Devices

Table 2. Op Amps

Part Number	Vos(V) Type	Vos Drift (V/℃) Type	Vnoise (Vp-p) Type	Slew Rate(V/us)	GBP(Hz)	Vs (V) min/max
ADA4528	0.3u	0.002u	97n	0.45	4M	2.2/5.5

Table 3. Voltage References

Part Number	Vout (V) Type	Initial Accuracy (%) max	Vout Tempco (ppm/V) max	Vnoise (Vp-p) Type	Iout Sourcing (A) max	Vs+ (V) min/max
LT6654A-4.096	4.096	0.05	10	8.2u	10m	5.2/38

References

1. "Operational Amplifier Stability Part 5 of 15: Real World Design of a Single Supply Buffer Circuit", 2006, Tim Green, originally published on AnalogZone (EnGenius)
2. "Intuitive Analog Circuit Design, Second Edition", Marc Thompson, 2013, Elsevier
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Additional Resources

LTspice

LTspice® is a high-performance SPICE III simulator, schematic capture, and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

Acknowledgments

Tim Green, Principal Engineer, Product Applications, Precision Amplifiers Group