KWIK CIRCUIT FAQ

ADC Driver Design Considerations for 15Msps 18bit ADC

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FAQ: What should I consider when designing an input driver for a 15Msps 18bit ADC

Introduction

ADC drivers are a key building block in the design of a data acquisition signal chain. ADC Drivers are used to perform many key functions like input signal amplitude scaling, single-ended to differential conversion, remove common mode offsets, and are regularly used to implement filtering. This Know-how With Integrated Knowledge (KWIK) Circuit FAQ note discusses how to create a scaled differential output signal from a single ended input signal, and level shift the signal to ensure that it meets the full scale capability of the ADC.

To help answer this FAQ we will use the LTC6228 a low noise, low distortion, very fast, rail to rail output op amp together with the LTC2387-18 SAR ADC. Noise computation is used to show the impact of the design on the overall SNR performance of the signal chain solution.

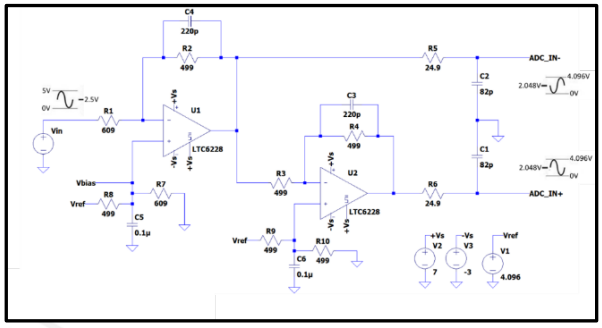

Figure 1. – Single Ended to Differential Conversion with Scaling and Level Shifting

Design Specifications Example

For this example the design requirement specifications are shown in Table 1, here the input signal is a 0V to 5V sine wave. The ADC driver circuit shown in Figure 1 will be used to work through this design. The function of this circuit is to convert, scale and shift the single ended input signal to an appropriate differential output signal so that it can be easily interfaced with the next stage in the signal chain the ADC.

To analyze the performance of the circuit shown in Figure 1 signal-to-noise (SNR) is used, here the noise contribution of each stage is taken and used in the overall computation. The datasheet specifications for the SNR of the LTC2387-18 ADC and spectral noise density of theLTC6228 have been used in the computations.

Table 1. Design Goal Key Specifications

Specification	Design Requirement
Input Single Ended	0 to 5V
Output Common Mode	2.048V
Differential output	8.192Vp-p
Supplies +Vs/-Vs	+7V/-3V
ADC Fully Differential	18 Bits
Vref	4.096V
SNR	93dB

Note that the effect of 1/f noise can be neglected for this example, as the frequency of interest is much higher than 1/f region, and the components selected and shown in Figure 1 are optimized to minimize any noise contribution.

Design Tips / Considerations

1. When selecting between single supply or dual supply some factors should be considered: Single supply can mean a reduced signal swing due to headroom requirements in the signal chain this can result in a decrease in SNR; Dual supply operation has the added complexity of having to generate a negative rail but will allow for higher signal swings due to the increased headroom available and can result in higher SNR performance compared to Single supply case. As you will see from Table 1 an asymmetrical supply of +7V/-3V is used, this supply voltage configuration provides enough headroom to ensure the input and output ranges are maintained.

2. V_{Bias} shown is Figure 1 this signal is required to level shift the output signal of the first stage to the desired common mode voltage level required to match the ADC input. As can be seen from Figure 1, this has been implemented by simply using a resistor divider where the reference voltage Vref is used as the source.
   The Capacitor C5 is used to eliminate any noise generated by the voltage divider.
   Note
   - The impedance of the driver network should be equivalent to the impedance seen by the feedback network. This is important if the internal bias current cancellation is not available. This configuration will ensure that any additional offset voltage introduced by the bias currents is reduced.
   - If internal bias cancellation is being used, then high resistance values should be used, this is to reduce the power consumed by this voltage divider network.
3. To reduce distortion errors high quality capacitors such as C0G (NP0) and resistors should be used in the RC filters.
4. Use standard values of resistors that are greater than the computed value.
5. If power is not a concern, the feedback resistor and gain resistor values of both stages can be reduced to 301Ω to improve SNR performance of the ADC and driver signal chain.

Design Procedure

(See Figure 1 for discussion references)

- **Signal scaling and Level Shifting**

  - Solve for R1 using the transfer function

$$V_o = V_i * \left(-\frac{R_2}{R_1}\right)$$

  It should be noted that, the voltage noise of the LTC6228 dominates for low resistance values. As the resistance increases, resistor noise starts to dominate. As resistance continues to increase, current noise dominates.

  If the resistor value for R2 is selected to be 499Ω, this offers a good balance for noise and power in the design.

  Solving for R1

$$R1 = \left|\left(-\frac{Vi}{Vo}\right) * R2\right| = \frac{5}{4.096} * 499$$
$$\boldsymbol{R1 = 609.13\Omega}$$

  - Calculate the V_{Bias} voltage value. This is done using the Common mode voltage of V_i and V_o . The goal is to level shift the output of the first stage amplifier to 2.048V.
    V_{ocm} = 2.048V and V_{icm}=2.5V
    V_{bias} is then calculated as follows

$$V_{bias} = \frac{Vi_{cm}R2 + Vo_{cm}R1}{R1+R2} = \boldsymbol{2.25V}$$

  - Calculate the ratio, $\frac{R_8}{R_7}$, to ensure that the required bias voltage (V_{bias}) is achieved. Assume R8 = 499Ω to achieve balanced impedance at input pins, then compute for R7. The noise at the voltage divider network is filtered by C5

$$\frac{R_8}{R_7} = \frac{V_{ref} - V_{bias}}{V_{bias}} = \frac{4.096 - 2.25}{2.25} = \boldsymbol{0.82}$$
$$R_7 = \frac{R_8}{0.82} = \frac{499\Omega}{0.82} = \boldsymbol{608.5\Omega}$$

- **Circuit Noise Analysis:**

  - ***1st Stage output - Voltage Noise Calculation***

    The total voltage noise at the output of the 1st stage ($E_{n_{U1}}$) can be calculated using the following equation

$$E_{nU1} = \sqrt{\left(E_{n_v} * NG\right)^2 + \left(E_{n_i} * NG\right)^2 + \left(E_{n_r} * NG\right)^2} \quad (1)$$

    Where:
    E_{n_v} – Op-amp's voltage noise, $\frac{0.88nV}{\sqrt{Hz}}$ for LTC6228
    E_{n_i} – Noise due to current noise * source impedance
    E_{n_r} – Resistor noise

    Calculate the noise gain of the 1st stage:

$$NG_{U1} = 1 + \frac{R_2}{R_1} = \boldsymbol{1.819}$$

    Solve for the voltage noise contribution due to current noise, E_{n_i}. From the LTC6228 datasheet the current noise density is $\frac{3x10^{-12}}{\sqrt{Hz}}$.

$$E_{n_i} = i_n * R_{eq}$$
$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = 247.3\Omega$$
$$E_{ni} = 3 \times 10^{-12} \cdot 274.3 = \frac{0.82\ nV}{\sqrt{Hz}}$$

$$E_{n_r} = \sqrt{4kTR_{eq}} = \sqrt{4 \cdot 1.38 \cdot 10^{-23} \cdot 274.27}$$

$$E_{n_r} = \frac{2.124nV}{\sqrt{Hz}}$$

Solve for the $E_{n_{U1}}$ using equation (1) and the computed values.

$$E_{n_{U1}} = \frac{4.442nV}{\sqrt{Hz}}$$

- **2nd Stage output - Voltage Noise Calculation**

Use the same procedure to calculate for Total Voltage Noise at 2nd stage, $E_{n_{U2}}$.

$$NG_{U2} = 1 + \frac{R_4}{R_3} = 2$$

$$E_{n_i} = \frac{0.749nV}{\sqrt{Hz}}$$

$$E_{n_r} = \frac{2.026nV}{\sqrt{Hz}}$$

$$E_{n_v} = \frac{0.88nV}{\sqrt{Hz}}$$

Utilizing equation 1 and the computed values above, E_{nU2} of the 2nd stage is:

$$E_{n_{U2}} = \frac{4.665nV}{\sqrt{Hz}}$$

- **Noise Bandwidth Calculations**

Calculate the effective noise bandwidth of each stage to convert the voltage noise to rms noise.

1st stage effective noise bandwidth with 2nd order filter

Solve for effective noise bandwidth, BW_n, using the equations below. Here **k** is the correction factor in reference to a brick wall LPF, for this example it is 1.22 and **n** is the order of filter.

$$f_c = \frac{1}{2\pi\sqrt{R_2R_5C_4C_2}} = 10.63MHz$$

$$f_{-3dB} = fc * \sqrt{2^{\frac{1}{n}} - 1} = 6.84MHz$$

$$BW_{n_{U1}} = f_{-3dB} * k$$
$$= 6.84 * 10^6 * 1.22 = 8.35MHz$$

2nd stage effective noise bandwidth: 3rd order filter

$$f_c = \frac{1}{2\pi\sqrt[3]{R_2R_4R_6C_4C_3C_1}} = 5.47MHz$$

$$f_{-3dB} = fc * \sqrt{2^{\frac{1}{n}} - 1} = 2.79MHz$$

$$BW_{n_{U2}} = f_{-3dB} * k$$
$$= 29.35x10^6 * 1.16 = 3.24MHz$$

- **Noise Spectral Density to RMS Noise Conversation**

Convert the spectral density to its equivalent rms noise for each stage.

$$E_{n_{U_{RMS}}} = E_{n_U} * \sqrt{BW_n}$$

Solve for $E_{n_{U1_{rms}}}$

$$E_{n_{U1_{rms}}} = \left(E_{n_{U1}} * \sqrt{BW_{nU1}}\right)$$

$$E_{n_{U1_{rms}}} = 4.442\frac{nV}{\sqrt{Hz}} * \sqrt{8.35x10^6}$$

$$E_{n_{U1_{rms}}} = 12.83\ \mu Vrms$$

Solve for $E_{n_{U2_{RMS}}}$

$$E_{n_{U2_{RMS}}} = \sqrt{BW_{n_{U2}}} * \sqrt{(E_{nU1} \cdot NG_{U2})^2 + {E_{nU2}}^2}$$

$$= \sqrt{3.24 * 10^6} * \sqrt{(4.992 * 10^{-9} * 2)^2 + (4.665 * 10^9}$$

$$E_{n_{U2_{RMS}}} = 18.1\ \mu Vrms$$

- **Calculate ADC Driver Total Noise**

Calculate the Total Differential Voltage Noise of the ADC driver.

$$E_{n_{diff_{RMS}}} = \sqrt{\left(E_{n_{U1_{RMS}}}\right)^2 + \left(E_{n_{U2_{RMS}}}\right)^2}$$

$$E_{n_{diff_{RMS}}} = 22.2\ \mu Vrms$$

- **ADC Noise Calculation**

Solve the Voltage Noise of the ADC for full scale input signal. Use 4.096Vp or 2.9Vrms and $SNR_{adc} = 95.7dB$.

$$E_{n_{adc}} = \frac{E_{s_{adc}}}{10^{\frac{SNR_{adc}}{20}}}$$

$$E_{n_{adc}} = \frac{2.9}{10^{\frac{95.7}{20}}}$$

$$E_{n_{adc}} = 47.6\ \mu Vrms$$

- **Signal Chain SNR Calculation**

Calculate the expected SNR performance based on the computed ADC driver and ADC noise.

a. **FullScale Input Signal**

$$E_{n_{adc+driver}} = \sqrt{\left(E_{n_{adc}}\right)^2 + \left(E_{n_{diff_{RMS}}}\right)^2}$$

$$E_{n_{adc+driver}} = 52.5\ \mu Vrms$$

$$SNR_{adc+driver} = 20\log\left(\frac{2.9}{52.5 * 10^{-6}}\right)$$

$$SNR_{adc+driver} = 94.8dB$$

b. **-1.7dBFS Input Signal:**

Where -1.7dBFS = 2.38V_{RMS}

$$SNR_{adc+driver} = 20\log\left(\frac{2.38}{52.5 * 10^{-6}}\right)$$

$$SNR_{adc+driver} = 93.1dB$$

Design Simulations

The performance of the circuit in *Figure 1* was simulated using the LTSpice simulation tool to determine if the key goal specifications were met.

Results obtained for the simulation test bench are shown in *Figure 2 -Figure 6*

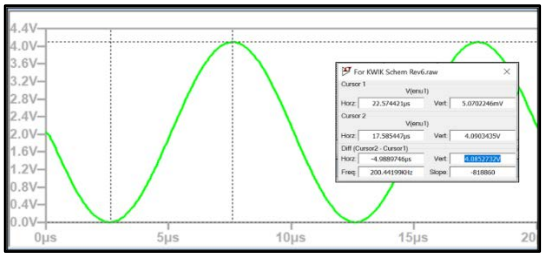

Figure 2. – Input Signal Scaling

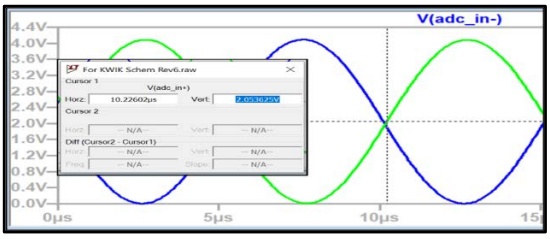

Figure 3. Output Common-mode Voltage, VOCM

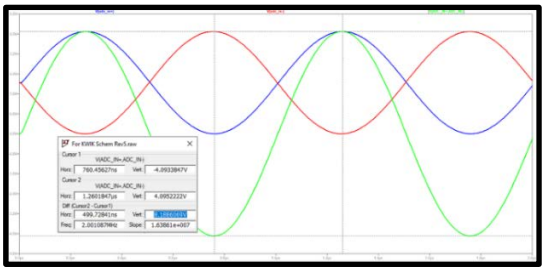

Figure 4: Differential Output

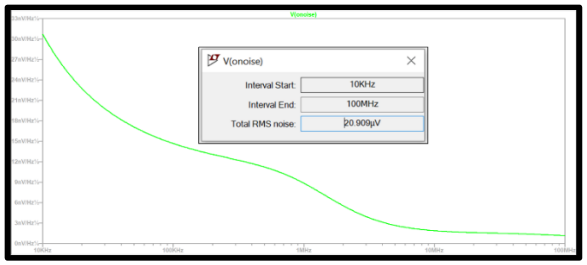

Figure 5 RMS Differential Noise

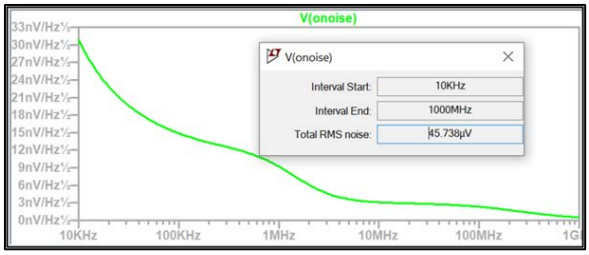

Figure 6. Total Noise, ADC + Driver

Table 2. Design Goal v's Simulation

Parameter	Design Goal	Simulation
Output Single Ended	4.096 Vp	4.085 Vp
Output Common Mode Voltage	2.048 V	2.054 V
Differential Output	8.192 Vp-p	8.189 Vp-p
ADC Driver Noise (RMS)	< 38.46 µV	22.2 µV
Driver + ADC Noise (RMS)	< 61.3 µV	52.5 µV

Measured Results

Results were gathered where the LTC6228 Evaluation Demo board as well as the LTC2387-18 Evaluation demo board . For this the input signal was set to -1.7dBFS. The measured SNR of this signal chain was 92.13 dB. This results is approximately 1 dB below the calculated SNR of 93.1 dB. The 1 dB discrepancy is most likely due to the parasitics of board and non-idealities resulting from the component tolerances used. To achieve the expected Full-Scale SNR add the 1.7dB to the measured value and that will result to 93.83 dB which is higher than the target SNR performance of the circuit design.

Table 3. Design Goal v's Measured

Parameter	Design Goal	Measured
SNR	93.5 dB	93.8 dB

Table 4. LTC6228 Very Fast, Low Noise, Low Distortion Rail to Rail Output Op Amp

Parameter	Specification
Vos Max	95µV
IBias Max	-44µA
GBP Typ	0.88nV/√Hz
Iq	16mA
Vs Span	±5V

Table 5. LTC2387-18 18bit 15Msps SAR ADC

Parameter	Specification
Resolution	18bits
F_{Sample}	15Msps
Input Type	Single Ended, Differential
Vin Span	±Vref
SNR	95.7 dB

Design Devices

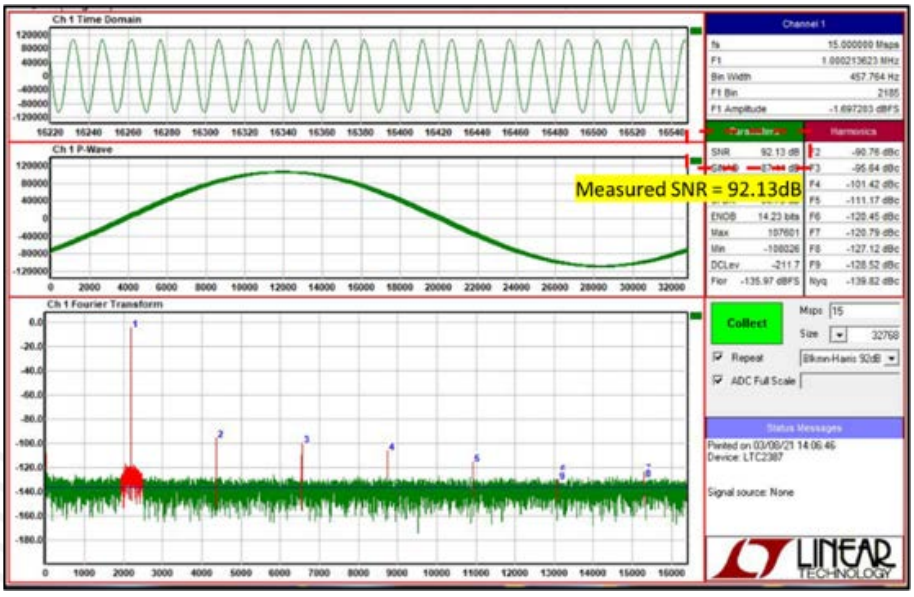

Figure 7- Measured Total SNR, ADC + Driver

References

LTSPICE® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

Analog Devices provides a wide range of minor tutorials for building theoretical foundation. Below are some of the mini tutorials that have been proven useful and worth reading through to gain more ins.

MT-047 – Op Amp Noise

MT-048 – Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth

MT-049 – Op Amp Total Output Noise Calculations for Single-Pole System

MT-050 – Op Amp Total Output Noise Calculations for Second-Order System