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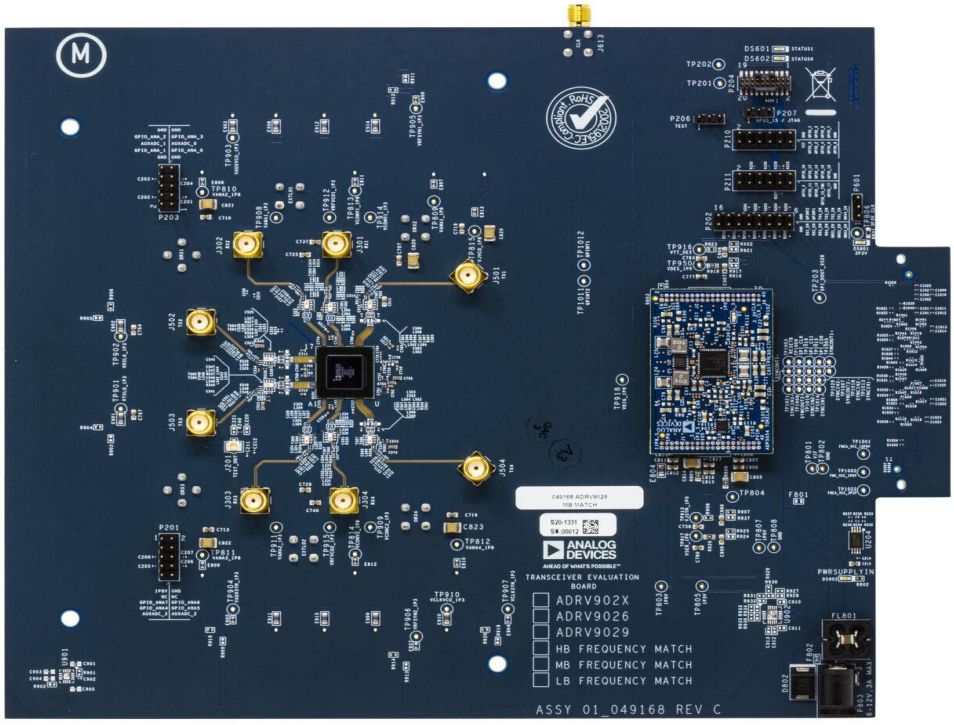
ADRV9029 DPD results with Ampleon PA

Part No: BLM9D2327_25B



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non- Link Sharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Ampleon PA test conditions

Transceiver	ADRV9029
Power Amplifier	BLM9D2327_25B
Driver Amplifier	Mini-circuit ZVA-183-S+
Application	M-MIMO
Output power	37 dBm (5 Watt)
PA Type	LDMOS
Frequency Range	2600 MHz
Gain	29.8 dB
Drain Efficiency %	37.6% @37.6dBm
P3dB	46.3
Bandwidth Tested	10x20 MHz LTE, 2x20MHz LTE
ACLR	-51.5dBc
Supply Voltage	30V

Test setup

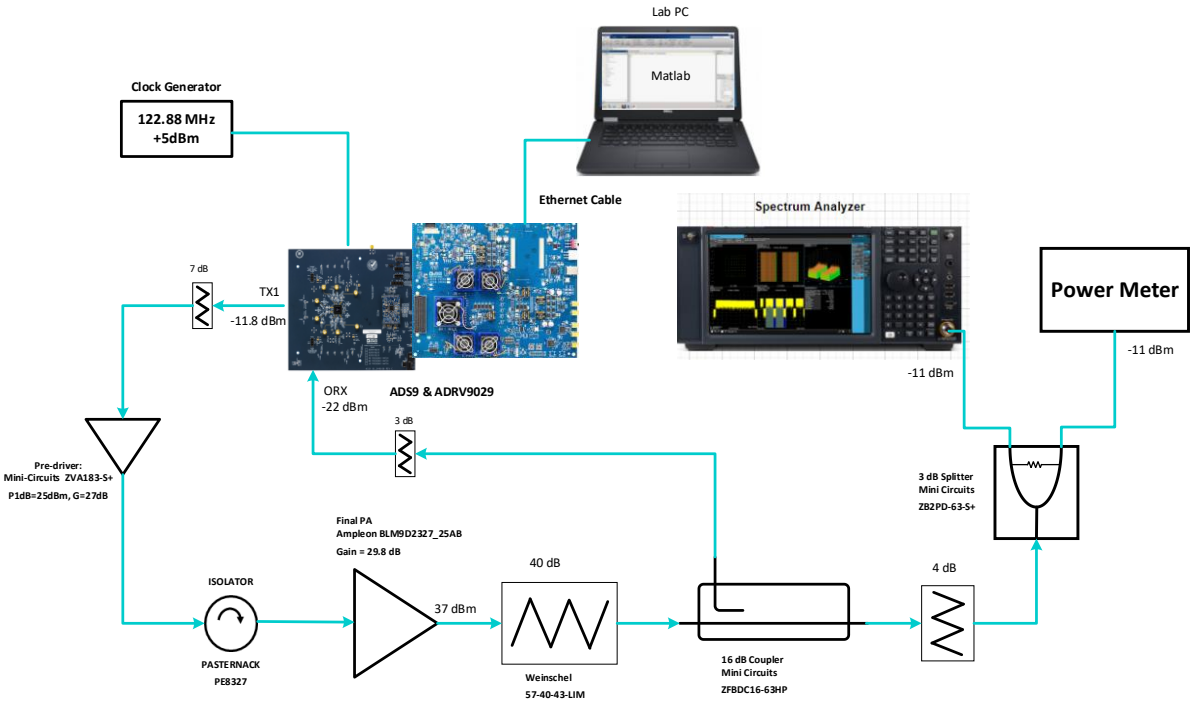


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used is the Mini-circuit ZVA-183-S+. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization

Summary

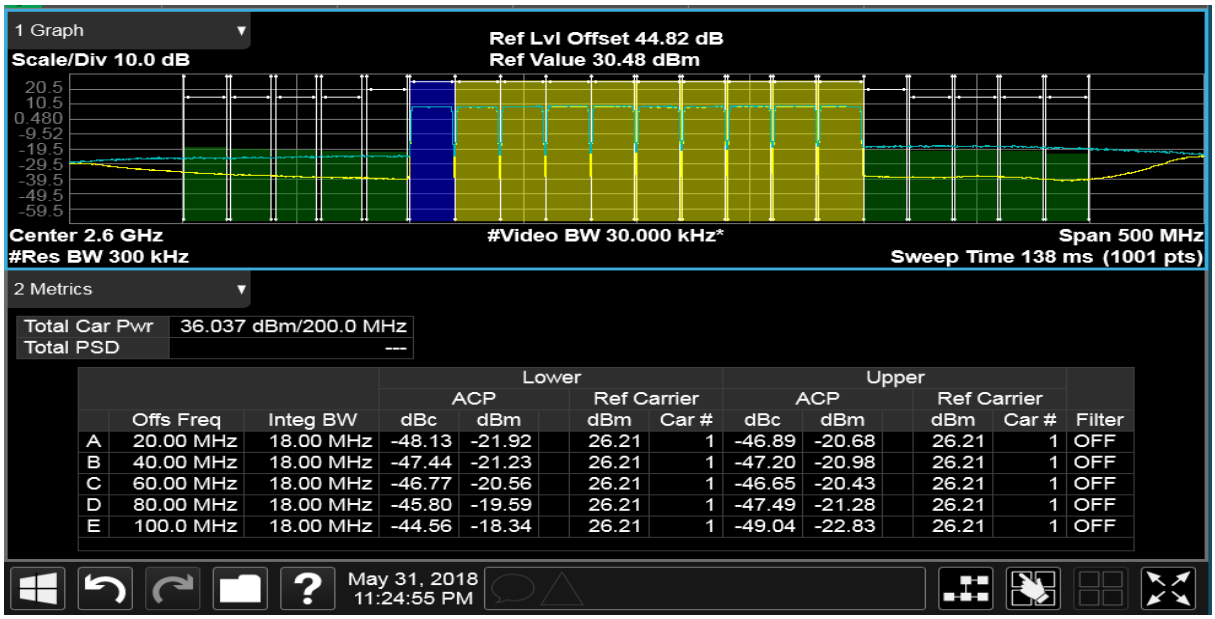
BLM9D2327_25B test conditions are:

- Center Frequency: 2595MHz
- Efficiency: 37.7%
- Average Output Power: 37.6 dBm (5.75 Watt)
- Test signal:10x20 MHz LTE Signal with 8.5 dB PAPR.
- Bias Conditions: Vdd =30V, Idqc =89mA, Vgs_M =2.3V, Vgs_P =1.55V

Test Results

Case 1: Test Signal: 10x20 MHz LTE (PAR = 8dB), Output Power: 36.2 dBm, Frequency : 2600MHz

Post DPD results:



						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	Gain	VDD V	IDD I[A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
2600	36.25	33.55	29.26	30	0.419	-33.41	-27.14	- 33.4	-26.83	-48.13	-46.89	-47.44	-47.2

Case 2: Test Signal: 2x20 MHz 200MHz (PAR = 8dB), Output Power: 37.05 dBm, Frequency : 2600MHz

Bias Conditions: Vdd =28V, Idqc =85mA, Vgs_M =2.3V, Vgs_P =1.55V

Post DPD results:

			Lower				Upper				
			ACP		Ref Carrier		ACP		Ref Carrier		
	Offs Freq	Integ BW	dBc	dBm	dBm	Car #	dBc	dBm	dBm	Car #	Filter
A	20.00 MHz	18.00 MHz	-52.60	-18.32	34.28	2	-50.93	-16.65	34.28	2	OFF
B	40.00 MHz	18.00 MHz	-59.50	-25.22	34.28	2	-58.20	-23.93	34.28	2	OFF
C	60.00 MHz	18.00 MHz	-61.05	-26.77	34.28	2	-61.60	-27.32	34.28	2	OFF
D	80.00 MHz	18.00 MHz	-60.98	-26.70	34.28	2	-61.61	-27.33	34.28	2	OFF
E	100.0 MHz	18.00 MHz	-62.23	-27.95	34.28	2	-62.99	-28.71	34.28	2	OFF

						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq (MHz)	Pout (dBm)	DE (%)	Gain	VDD (V)	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
2600	37.05	37.64	28.79	30	0.419	-34.97	-34.73	- 53.4	-50.58	-52.6	-50.93	-59.5	-58.2

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.