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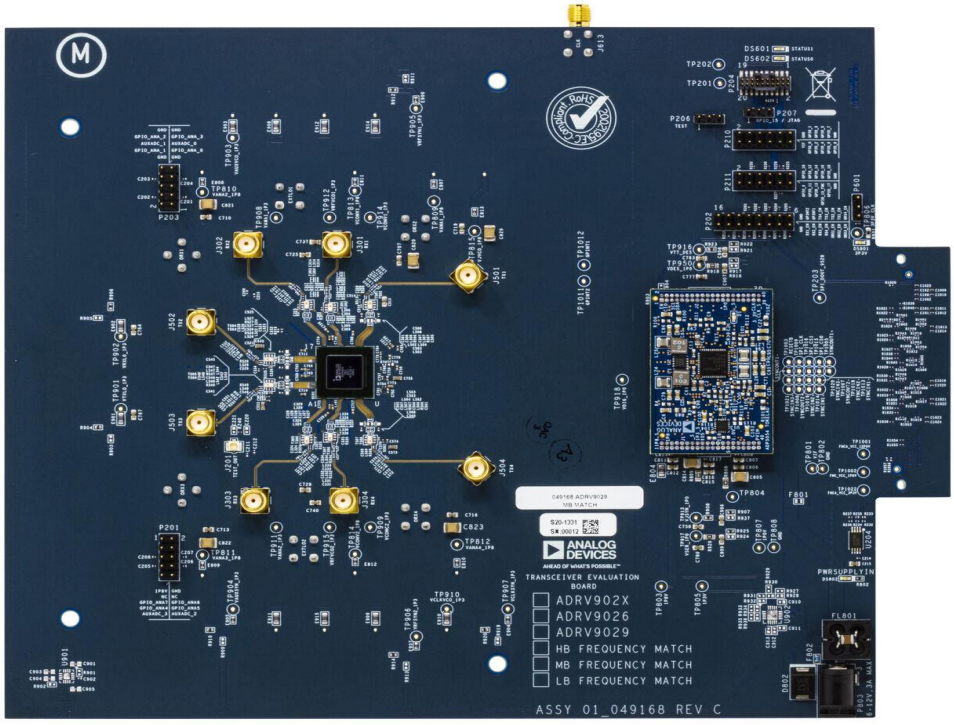
# ADRV9029 DPD results with Ampleon PA

# Part No: BLC10G22XS_400AVT




**ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution**

# Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

**User Case:** 51C_Non-LinkSharing

**Sampling rate:** 245.76Msps

**JESD Lane rate:** 16.22016Gbps

**DFE (CFR ,DPD):** Enabled

**LOL correction:** Enabled

# Ampleon PA test conditions

| | |
|---|---|
| Transceiver | ADRV9029 |
| Power Amplifier | BLC10G22XS-400AVT |
| Driver Amplifier | Wolfspeed PTMC210404MD Driver + Mini Circuits ZVA-183-S+ Pre driver |
| Application | Macro Cell |
| Output power | 47.3 dBm |
| PA Type | LDMOS |
| Frequency Range | 2155 MHz |
| Gain | 17 dB |
| Drain Efficiency % | 43.35% @ 47.5 dBm |
| P3dB | 56 dBm |
| Bandwidth Tested | 2x20 MHz LTE,<br>60 MHz 5G NR |
| ACLR | -50 dBc @ 60 MHz |
| Supply Voltage | 28V |

# Test setup

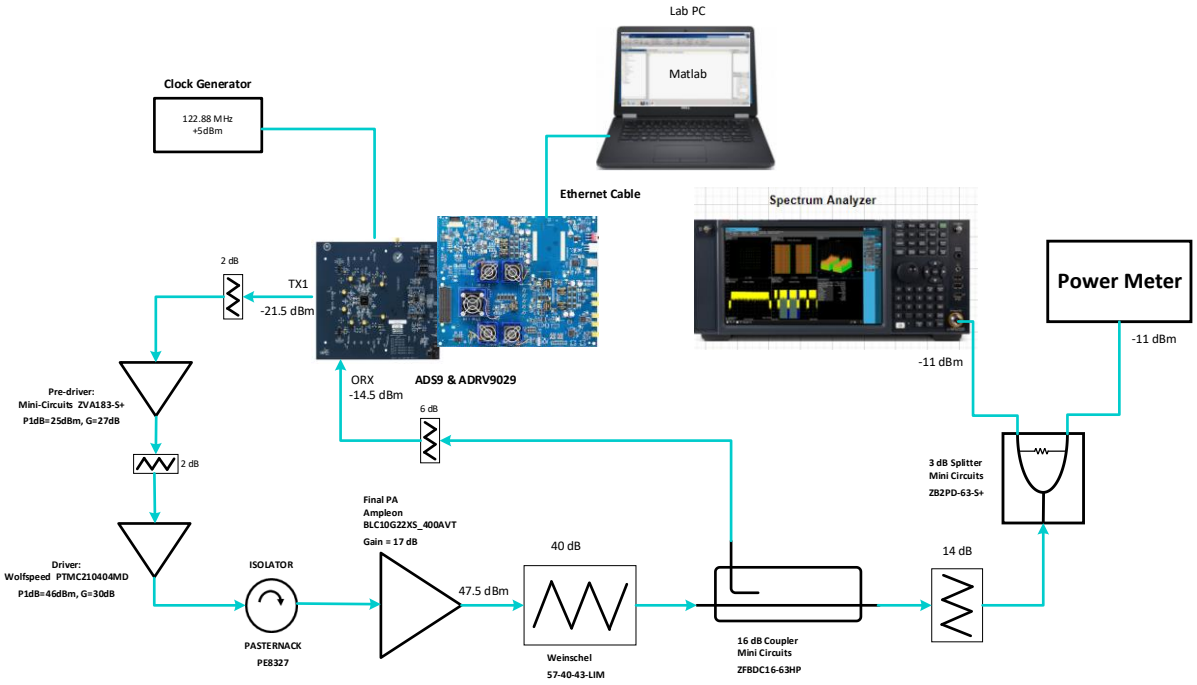



Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used is the Wolfspeed PTMC210404MD Driver. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization

# Summary

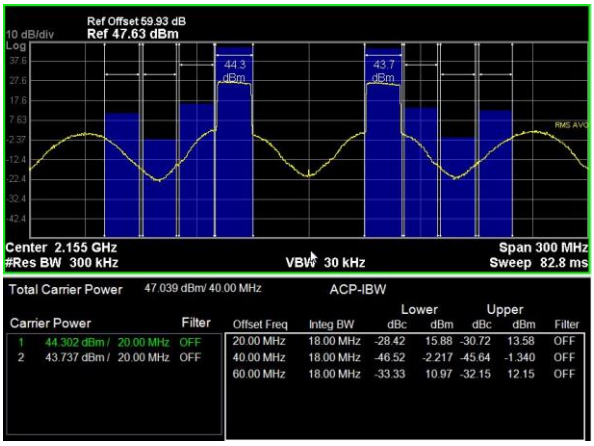
**BLC10G22XS-400AVT test conditions are:**

- Center Frequency: 2155MHz
- Efficiency: 43.35%
- Average Output Power: 47.5 dBm (56.2 Watt)
- Test signal: 2x20 MHz over 100MHz LTE Signal ,60MHz 5G NR Signal with 8 dB PAR.
- Bias Conditions : Vds= 28V, Vgs1= 2.15V, Idq1= 658mA, Vgs2=1.2V

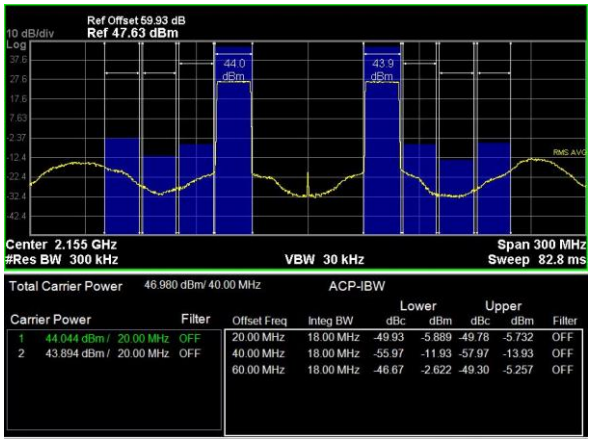
# Test Results

Case 1: Test Signal: 2x20 MHz LTE (PAR = 8dB), Output Power: 47.51 dBm , frequency :2155MHz (PA terminated with 40dB pad)

**Pre DPD**




**Post DPD**




| | | | | | Open Loop [Pre-DPD] | | | | Closed Loop [Post-DPD] | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Freq: MHz | Pout dBm | DE % | VDD V | IDDI | ACP_Lo [dBc] | ACP_Hi [dBc] | ALT1_lo [dBc] | ALT1_hi [dBc] | ACP_LO [dBc] | ACP_HI [dBc] | ALT1_lo [dBc] | ALT1_hi [dBc] |
| 2155 | 47 | 43.35 | 28 | 4.697 | -28.42 | -30.72 | - 46.52 | -45.64 | -49.93 | -49.78 | -55.97 | -57.97 |

Case 2: Test Signal : 60 MHz 5G NR(PAR = 8dB), Output Power: 47.49 dBm , frequency :2155MHz

**Pre DPD**


**Post DPD**


| | | | | | Open Loop [Pre-DPD] | | | | Closed Loop [Post-DPD] | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Freq: MHz | Pout dBm | DE % | VDD V | IDD I | ACP_Lo [dBc] | ACP_Hi [dBc] | ALT1_lo [dBc] | ALT1_hi [dBc] | ACP_LO [dBc] | ACP_HI [dBc] | ALT1_lo [dBc] | ALT1_hi [dBc] |
| 2155 | 47.3 | 41.04 | 28 | 4.883 | -26.98 | -26.66 | - 40.82 | -41.1 | -50.8 | -50.11 | -54.81 | -54.71 |

# Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.