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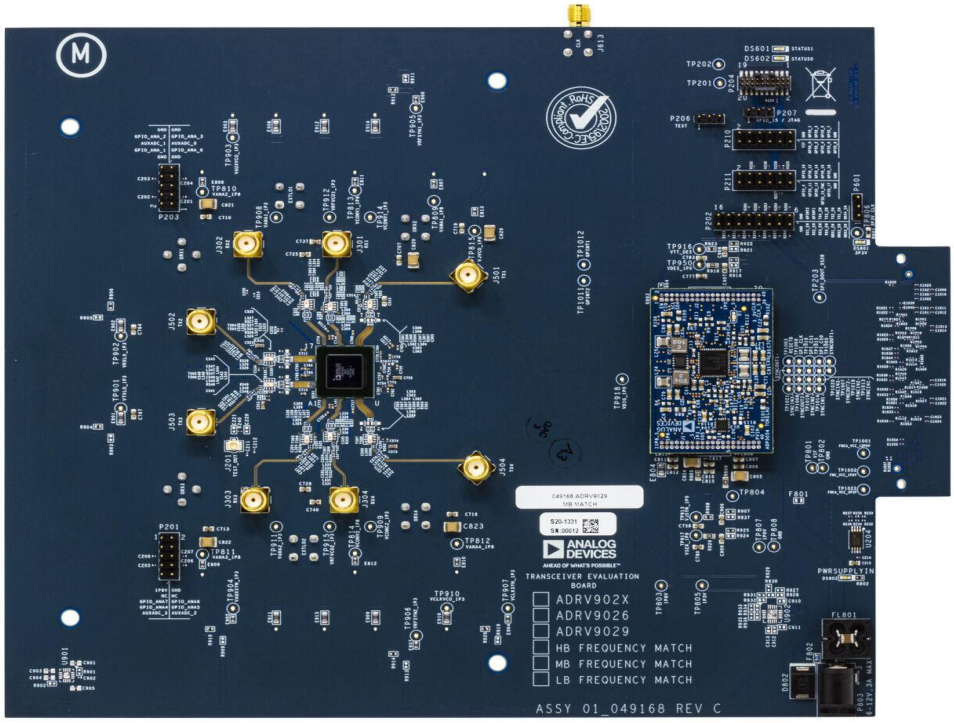
ADRV9029 DPD results with NXP PA

Part No: AFSC5G26E38



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

NXP PA test conditions

Transceiver	ADRV9029
Power Amplifier	AFSC5G26E38
Driver Amplifier	Mini-circuit ZVA183-S+
Application	M-MIMO
Output power	38.23 dBm (5.57 W)
PA Type	LDMOS
Frequency Range	2496-2690 MHz
Gain	35.40
Drain Efficiency %	44.90
P3dB	46.50 dBm
Bandwidth Tested	LTE 8x20 160MHz, LTE 10x20 200MHz
ACLR	-47.20 dBc
Supply Voltage	28V

Test setup

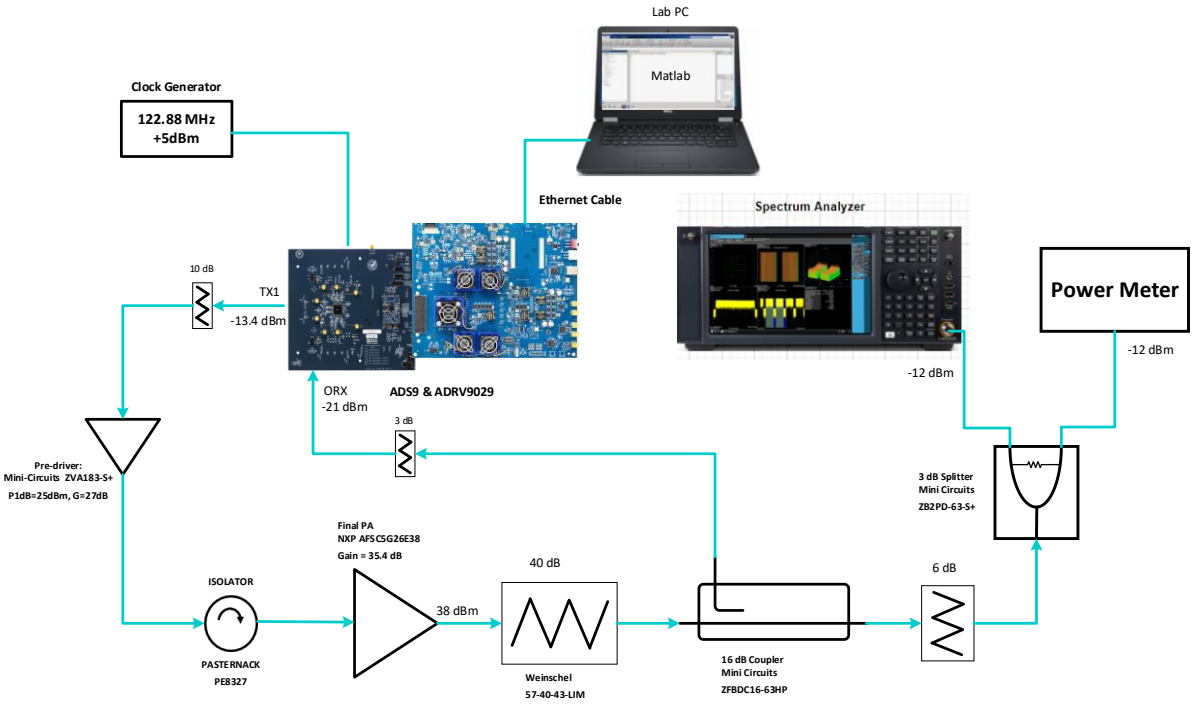


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is broadband Mini-circuit ZVA-183-S+. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

In Fig. 1, the Doherty Amplifier AFSC5G26E38 is loaded with high power attenuator presenting a max VSWR of 1.15 to not detune the PA from its optimum tuning.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization

Summary

AFSC5G26E37 test conditions are:

- Center Frequency: 2600MHz
- Efficiency: 40.80%
- Average Output Power: 38.00 dBm (6.31 Watt)
- Test signal: LTE 5x20MHz 100MHz 8x20 160MHz ,10x20 200MHz LTE signal with 8 dB PAPR
- Bias Conditions : Vdd =28V, Idq =63mA, Vgc1=4.95V, Vgc2=2.86V, Vgp1=1.55V, Vgp2=1.4V.

Test Results

Case 1: Test Signal: LTE 8x20MHz 160MHz (PAR = 7.5 dB), Output Power: 38.23 dBm, Band 41: 2600MHz

Post DPD results:

						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
2600	38.23	40.82	35.44	28	0.582	-25.17	-23.65	-25.50	-24.08	-51.5	-51.24	-51.6	-51.80

Case 2: Test Signal: LTE 10x20MHz 200MHz (PAR = 8dB), Output Power: 37.46 dBm, Band 41: 2600MHz

Post DPD results:

						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
2600	37.46	35.47	34.67	28	0.561	-24.83	-22.66	-24.97	-22.63	-48.20	-47.20	-47.60	-47.40

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.