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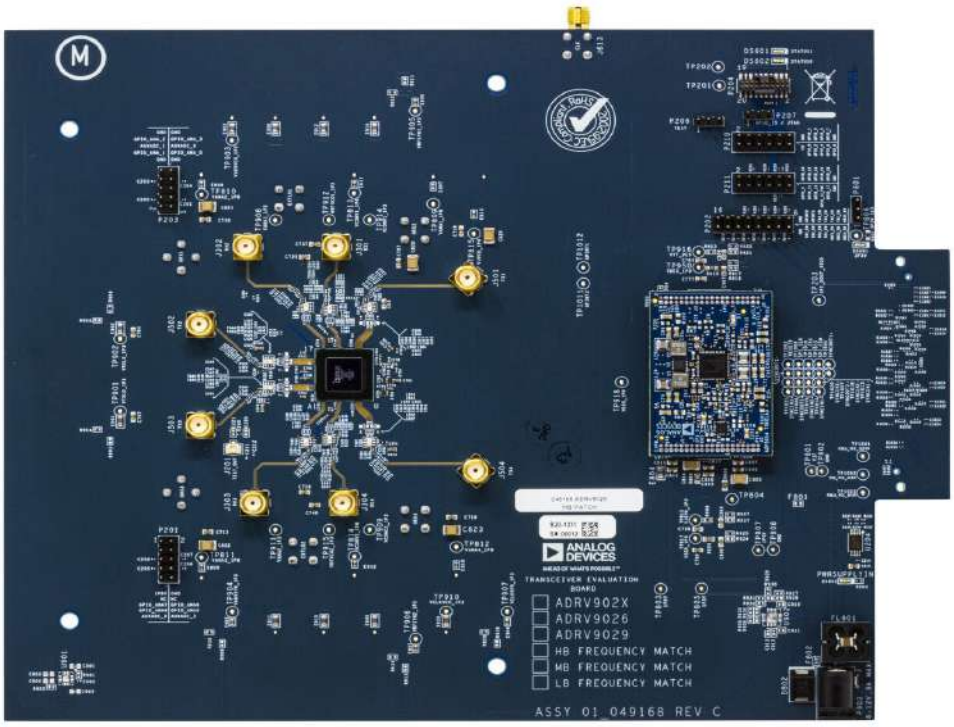
ADRV9029 DPD results with WOLFSPEED PA

Part No: WS1A3640



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

WOLFSPEED PA test conditions

Transceiver	ADRV9029
Power Amplifier	WS1A3640
Driver Amplifier	WSGPA01
Application	M-MIMO
Output power	39.5 dBm (~9 Watt)
PA Type	GaN
Frequency Range	3700 MHz
Gain	13.5dB
Drain Efficiency %	~40.57%
P3dB	47.78 dBm(60W)
Bandwidth Tested	10x20 MHz LTE,8x20 MHz LTE 5X20 MHz LTE
ACLR	-49.68 dBc @ 200 MHz
Supply Voltage	48V

Test setup

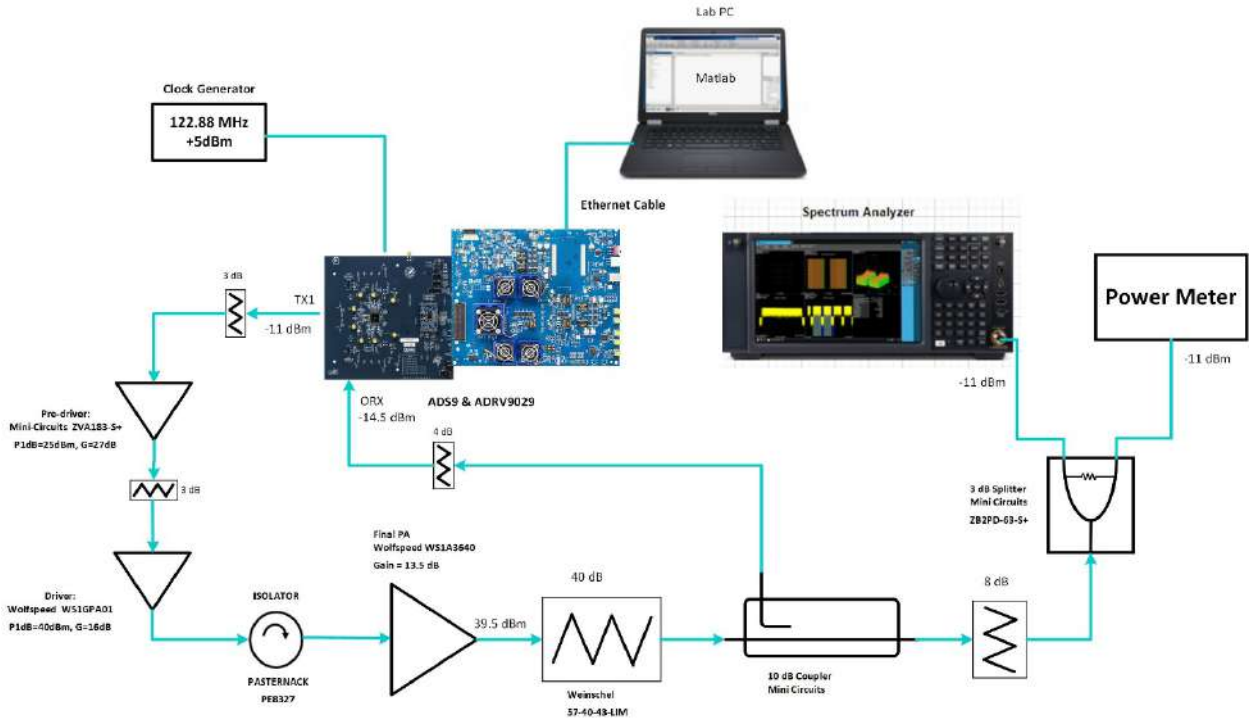


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is broadband Wolfspeed WSGPA01. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

In Fig. 1, the Doherty Amplifier WS1A3640 is loaded with high power attenuator presenting a max VSWR of 1.15 to not detune the PA from its optimum tuning.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design.

Summary

WS1A3640 test conditions are:

- Center Frequency: 3700 MHz
- Efficiency: 40.57%
- Average Output Power: 39.5dBm dBm (9 Watt)

Test signals: 10x20 MHz LTE,8x20 MHz LTE, 5X20 MHz LTE

Test Results

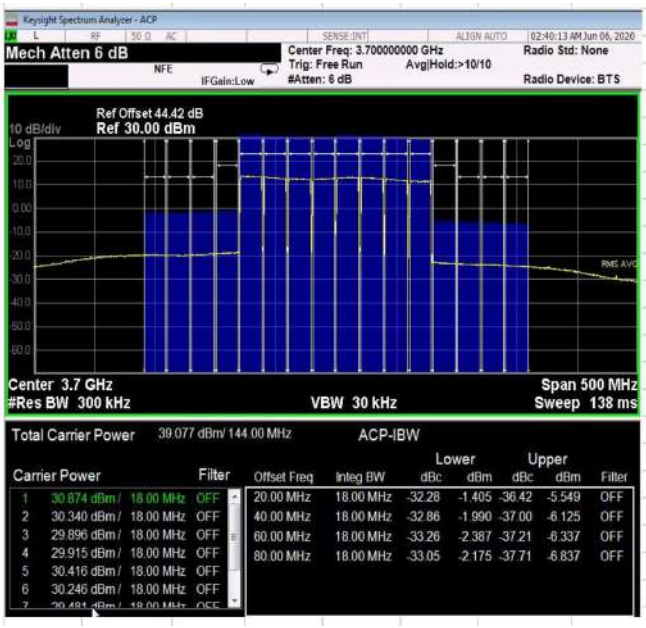
Case 1: Test Signal: LTE 10x20MHz (PAR = 8dB), Output Power: 39.5 dBm, 3700MHz

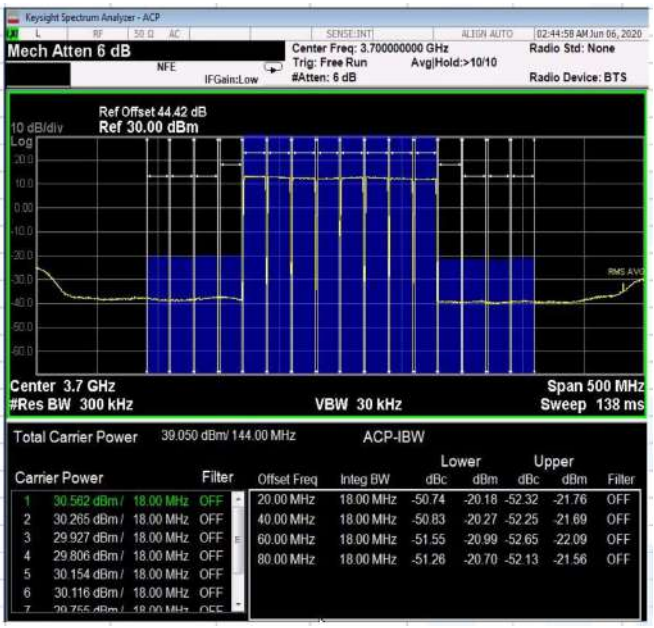
Post DPD results:

						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3700	39.55	40.57	13.5	48	0.463	-31.86	-36.22	-31.95	-36.27	-49.68	-50.43	-49.59	-50.39

Case 2: Test Signal: LTE 8x20MHz (PAR = 8dB), Output Power: 39.48 dBm, 3700MHz

Post DPD results:





						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3700	39.48	40.35	13.5	48	0.458	-32.28	-36.42	-32.86	-37	-50.83	-53.05	-50.99	-53.22

Case 3: Test Signal: LTE 5x20MHz (PAR = 8dB), Output Power: 39.5 dBm, 3700MHz

Post DPD results:

						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3700	39.5	40.54	13.5	48	0.458	-32.59	-35.66	-33.84	-37.4	-54.98	-55.64	-54.91	-56.11

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.