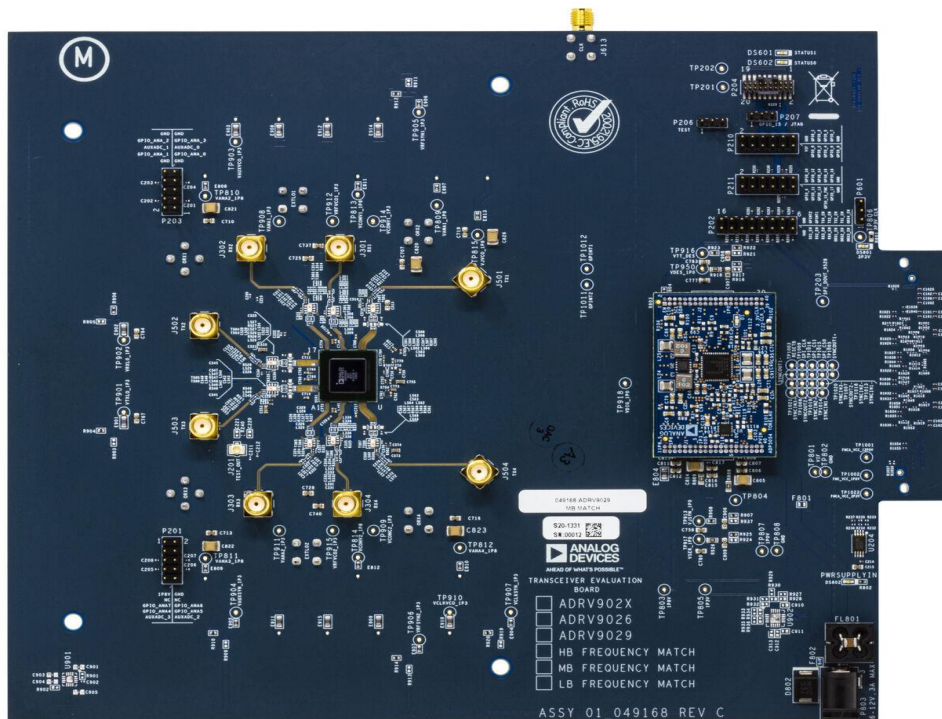




ADRV9029 DPD results with SKYWORKS PA

Part No: SKY66523-11



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Skyworks PA test conditions

Transceiver	ADRV9029
Power Amplifier	SKY66523-11
Driver Amplifier	Mini Circuits ZVA183-S+
Application	Small-Cell
Output power	29.9 dBm (0.97W)
PA Type	GaAs
Frequency Range	3550-4200 MHz
Gain	30.8dB
Drain Efficiency %	23.9%
Bandwidth Tested	1x100MHz NR ,2x100MHz NR
ACLR	-52dBc
Supply Voltage	12.6V

Test setup

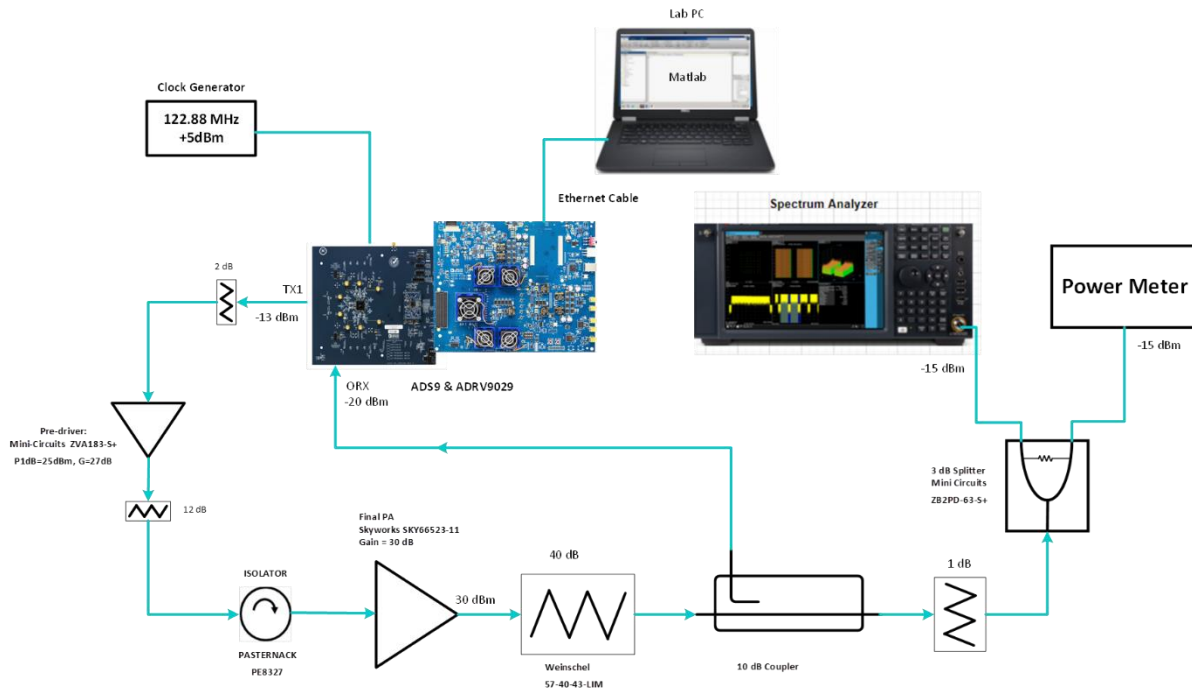


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is EV1HMC788ALP2. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design.

Summary

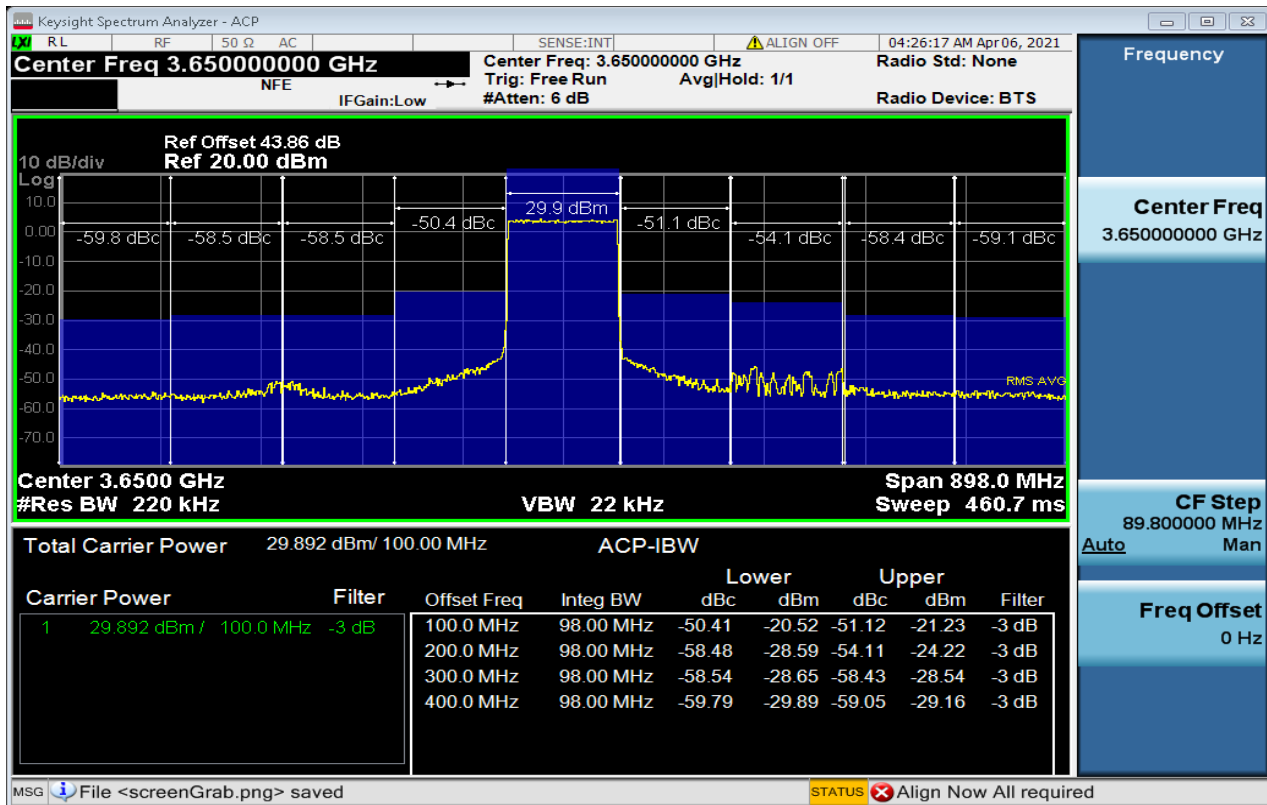
SKY66523-11 test conditions are:

- Center Frequency: 3650 MHz
- Efficiency: 23.9%
- Average Output Power: 29.9dBm
- Test signal: 1x100MHz,2 x100MHz NR
- Bias conditions: Vcc2: 12.6V , 139.5mA, Vcc1: 5.0V , 54.6mA, Ven: 2.0V , 0.0mA

Test Results

Case 1: Test Signal:1x100MHz NR(PAR=8.5dB), Output Power: 29.9dBm, Frequency: 3650MHz
 Bias conditions: Vcc2: 12.6V , 139.5mA, Vcc1: 5.0V , 54.6mA, Ven: 2.0V , 0.0mA

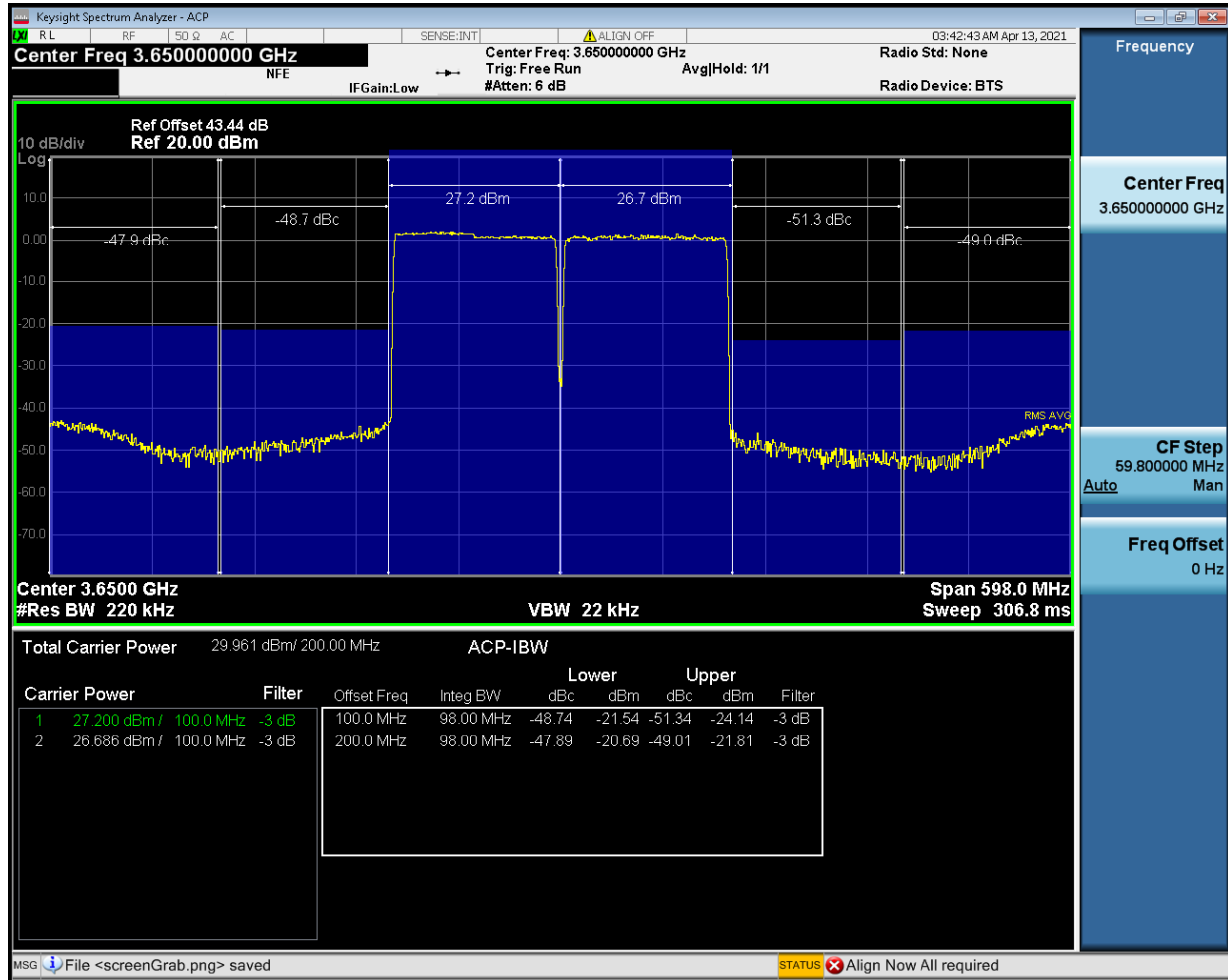
Post DPD results:



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	VDD [V]	Idd [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3650	29.9	23.9	12.6	0.3	-25.4	-27.5	-46.8	-46	-50.4	-51.1	-58.5	-54.1

ADRV9029- SKYWORKS PA test report

Case 2: Test Signal: 2x100MHz NR(PAR=8.5dB), Output Power: 29.9dBm, Frequency: 3650MHz
 Bias conditions: Vcc2: 12.6V , 140.1mA, Vcc1: 5.0V , 54.6mA, Ven: 2.0V , 0.0mA



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq:	Pout	DE	VDD	Idd	ACP_Lo	ACP_Hi	ALT1_lo	ALT1_hi	ACP_LO	ACP_HI	ALT1_lo	ALT1_hi
MHz	[dBm]	[%]	[V]	[A]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]
3650	29.9	23.8	12.6	0.3	-25.3	-28.5	-36.9	-37.6	-48.7	-51.3	-47.9	-49

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.