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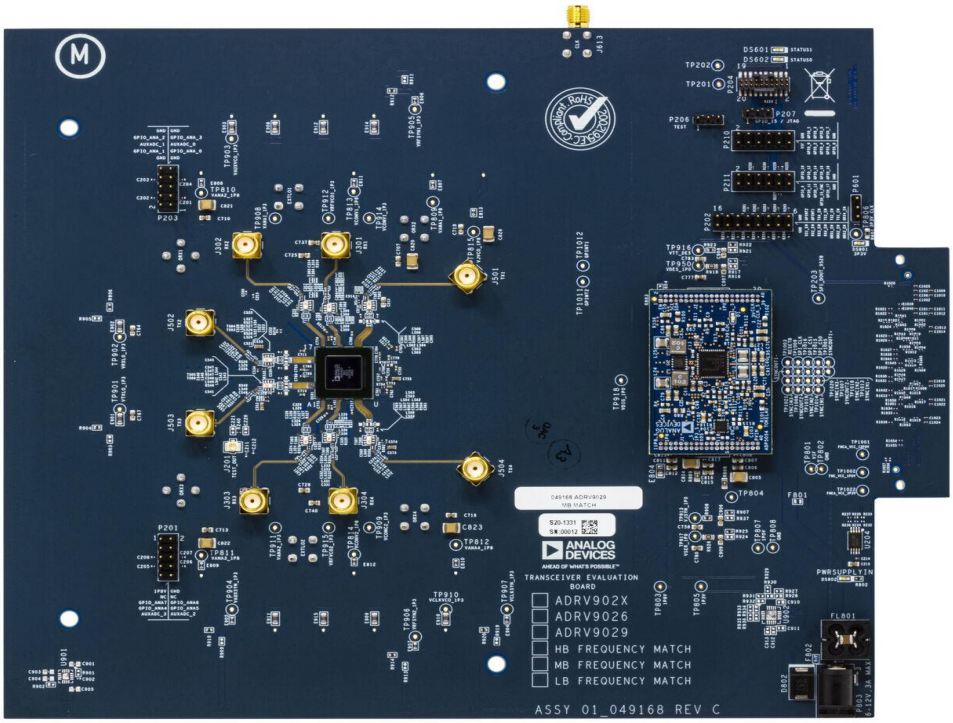
ADRV9029 DPD results with SKYWORKS PA

Part No: SKY66318-11



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Skyworks PA test conditions

Transceiver	ADRV9029
Power Amplifier	SKY66318-11
Driver Amplifier	Mini Circuits ZVA183-S+
Application	Small-Cell
Output power	24 dBm (0.25W)
PA Type	GaAs
Frequency Range	3300-3600 MHz
Gain	37dB
Drain Efficiency %	17.4%
Bandwidth Tested	5x20MHz
ACLR	-48dBc
Supply Voltage	5V

Test setup

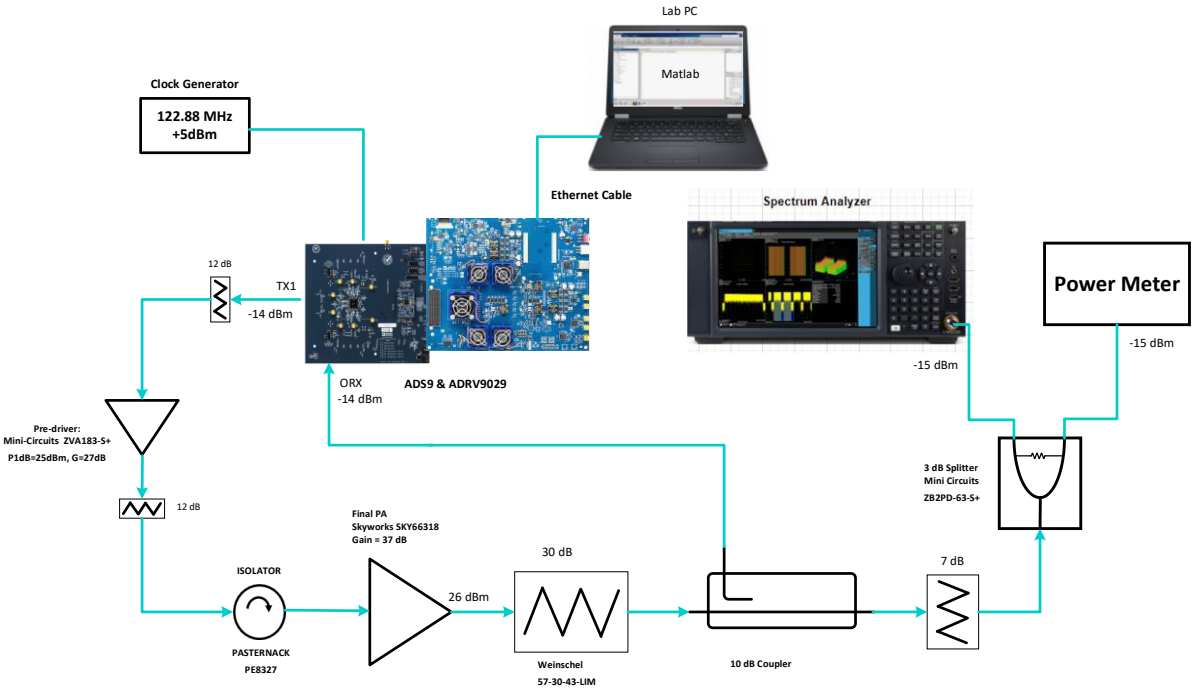


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is EV1HMC788ALP2. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design.

Summary

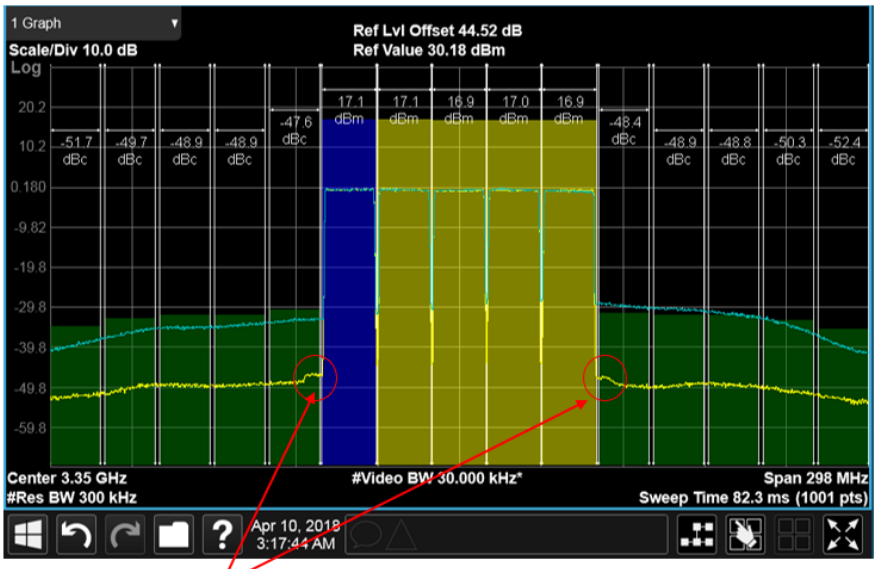
SKY66318-11 test conditions are:

- Center Frequency: 3350 MHz
- Efficiency: 17.4%
- Average Output Power: 24dBm
- Test signal: 5x20MHz
- Bias conditions: Vdd=5V, Idq=111mA

Test Results

Case 1: Test Signal:5x20MHz (PAR=8dB), Output Power: 24dBm, Frequency: 3350MHz

Post DPD results:



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	VDD [V]	Idd [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3350	24.2	17.4	5	0.3	-32.8	-29.1	-34	-30	-47.7	-48.3	-49	-48.8

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.