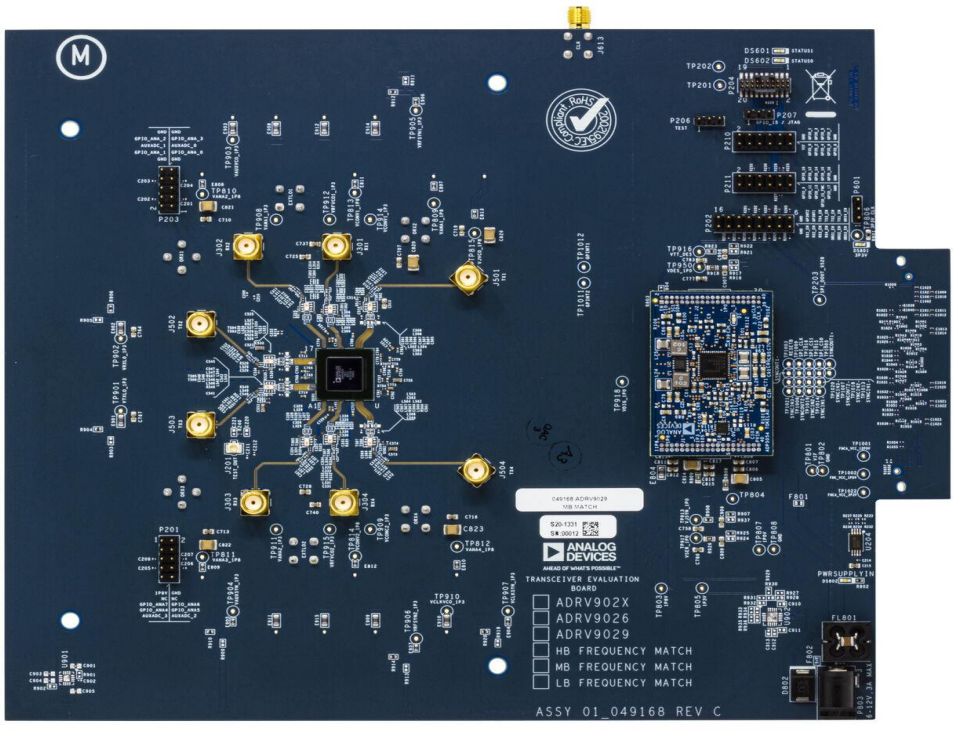
ADRV9029 DPD results with NXP PA

Part No: A3I35D025N



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

NXP PA test conditions

Transceiver	ADRV9029
Power Amplifier	A3I35D025N
Driver Amplifier	Mini-circuit ZVA183-S+
Application	M-MIMO
Nominal Output Power	33 dBm
PA Type	LDMOS
Frequency Range	2500-2700 MHz
Gain	24 dB
Drain Efficiency %	32.5% @37dBm
P3dB	45.3dBm
Bandwidth Tested	10x20MHz LTE @ Pout=33dBm, 10x20MHz LTE@ Pout=36.5dBm
ACLR	-53.1dBc (10x20 MHz LTE @Pout=33dBm)
Supply Voltage	28V

Test setup

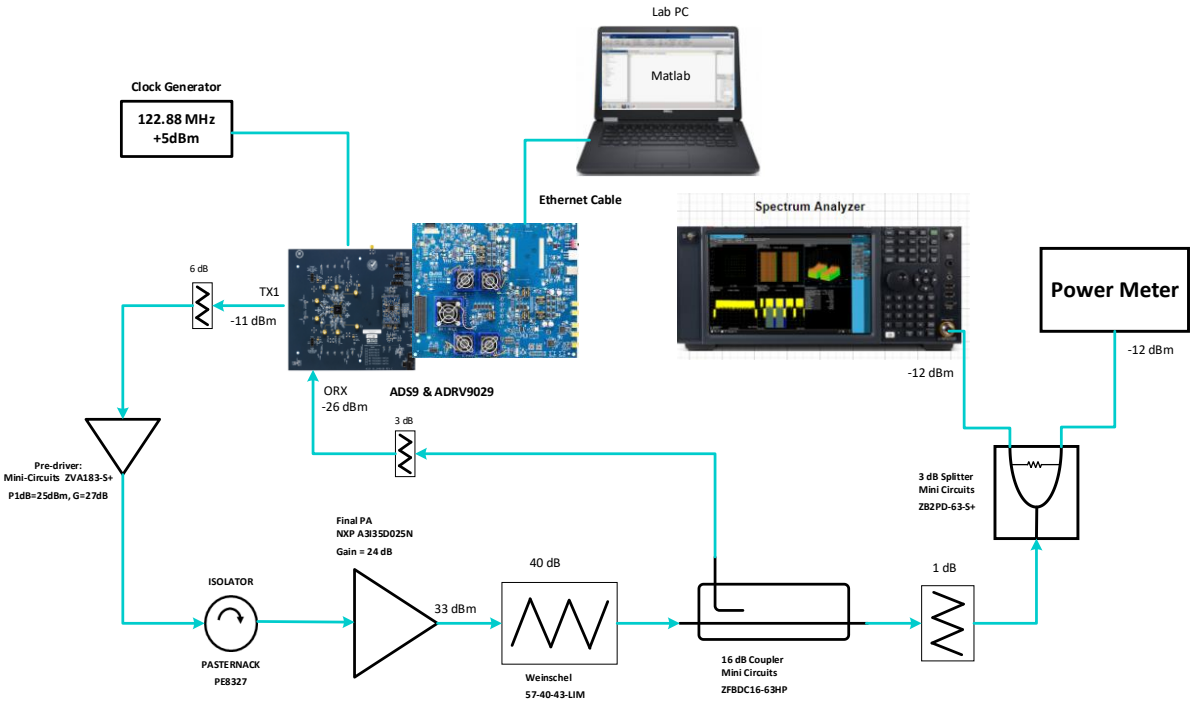


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used is the Mini-circuit ZVA-183-S+. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization

Summary

A3I35D025N has been tested for:

- Operating Frequency: 3600 MHz
- Efficiency: 32.5% @37dBm
- Average Output Power: 33dBm(2.01W) and 36.5dBm(4.47W)
- Test signal: 10x20MHz LTE @Pout=33dBm, 10x20MHz LTE @Pout=36.5dBm
- Bias Conditions : Vdd =28V, Vgc =7V, Vgp=7V, Idq=151mA

Test Results

Case 1 : Test Signal : 10X20MHz LTE 200MHz (PAR=8dB), Output Power:33 dBm ,Band 42: 3600 MHz

Post DPD results :

					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: (MHz)	Pout (dBm)	DE (%)	VDD (V)	IDD (I)	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3600	33	21.2	28	0.339	-29.72	-31	- 30.4	-31.87	-53.4	-53.14	-54.26	-53.39

Case 2: Test Signal :10x20MHz LTE - 200MHz (PAR=8dB),Output Power:36.5 dBm , Band 42:3600MHz.

Post DPD Results:

					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: (MHz)	Pout (dBm)	DE (%)	VDD (V)	IDD (I)	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3600	36.50	30.8	28	0.518	-25.31	-27.31	-25.72	-27.72	-50.61	-51	-50.36	-52.01

Conclusion

The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.