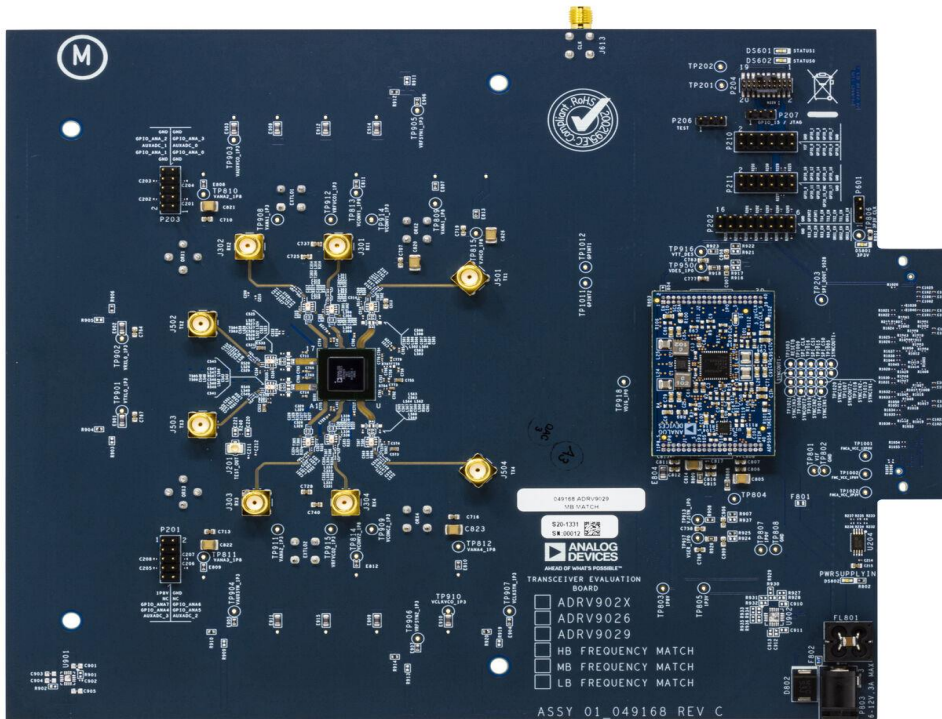




# ADRV9029 DPD results with NXP PA

## Part No: A3M37TL039



### ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

## Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

**User Case:** 51C\_Non-LinkSharing

**Sampling rate:** 245.76Msps

**JESD Lane rate:** 16.22016Gbps

**DFE (CFR ,DPD):** Enabled

**LOL correction:** Enabled

## NXP PA test conditions

Transceiver	<a href="#">ADRV9029</a>
Power Amplifier	<a href="#">A3M37TL039</a>
Driver Amplifier	Mini-circuit ZVA-183-S+
Application	M-MIMO
Output power	37 dBm (5 Watt)
PA Type	LDMOS
Frequency Range	3600-3800 MHz
Gain	28 dB
Drain Efficiency %	29.7% @37dBm
P3dB	47.3 dBm
Bandwidth Tested	LTE 5MHz, 20MHz, (2*5, 2*20, 4*5, 4*20)@160MHz, 1*100MHz NR, 2*100MHz NR, LTE 8*20MHz
ACLR	-61.8dBc @LTE 20MHz
Supply Voltage	30V

## Test setup

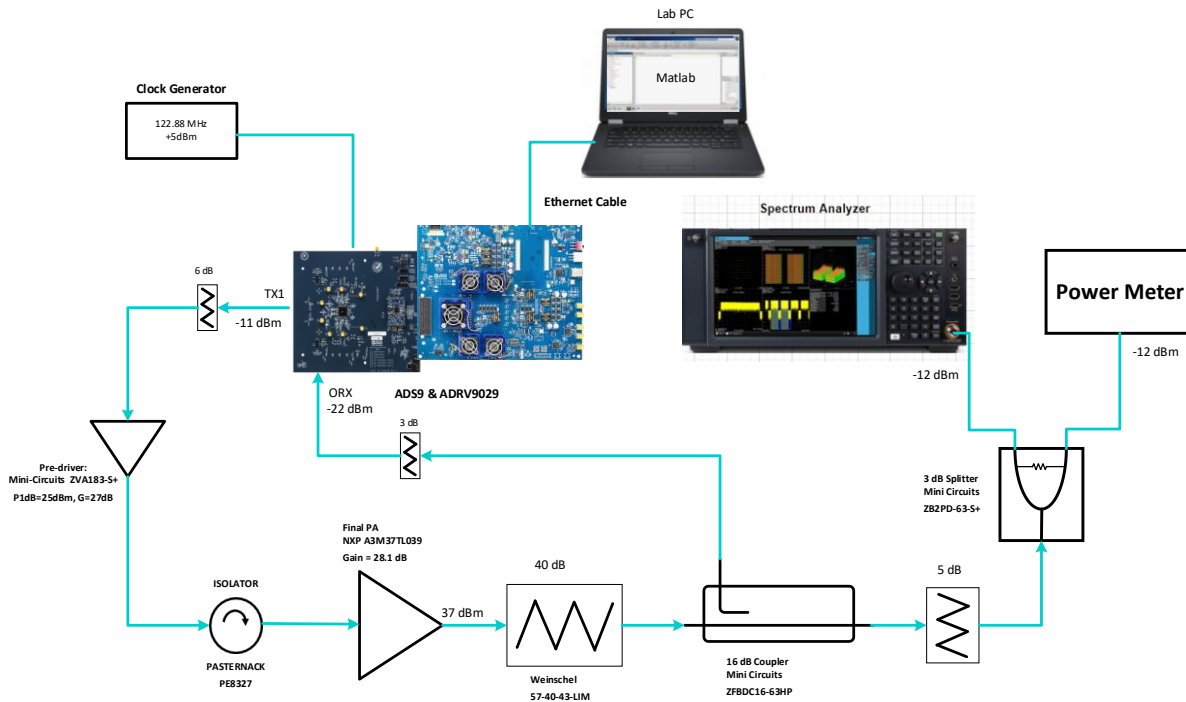


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment, that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used is the Mini-circuit ZVA-183-S+. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

[https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd\\_model\\_optimization](https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization)

## Summary

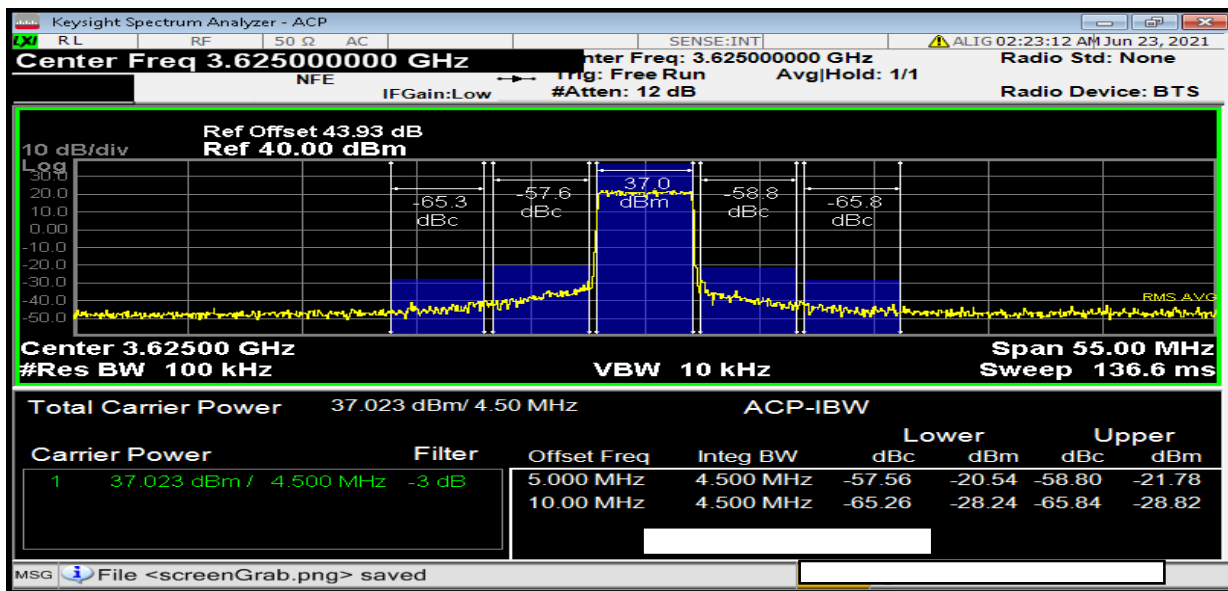
### A3M37TL039 test conditions are:

- Center Frequency: 3625MHz
- Efficiency: 29.7%
- Average Output Power: 37 dBm (5 Watt)
- Test signal : LTE 5 MHz, 20MHz, 2\*5MHz, 2\*20MHz, 4\*5MHz, 4\*20MHz, 8\*20MHz, 1\*100 MHz - 5G NR, 2\*100 MHz -5G NR
- Bias conditions : Vdc\_Vdp: 29.99 V , 112.00 mA, Vgc1: 5.69 V , 2.00 mA,  
Vgc2: 2.90 V ,0.30 mA, Vgp1: 1.40 V , -0.20 mA,Vgp2: 1.60 V , -0.10 mA

## Test Results

Case 1: Test Signal: 5MHz LTE (PAR = 8dB), Output Power: 37 dBm , Frequency: 3625 MHz.

### Post DPD results:

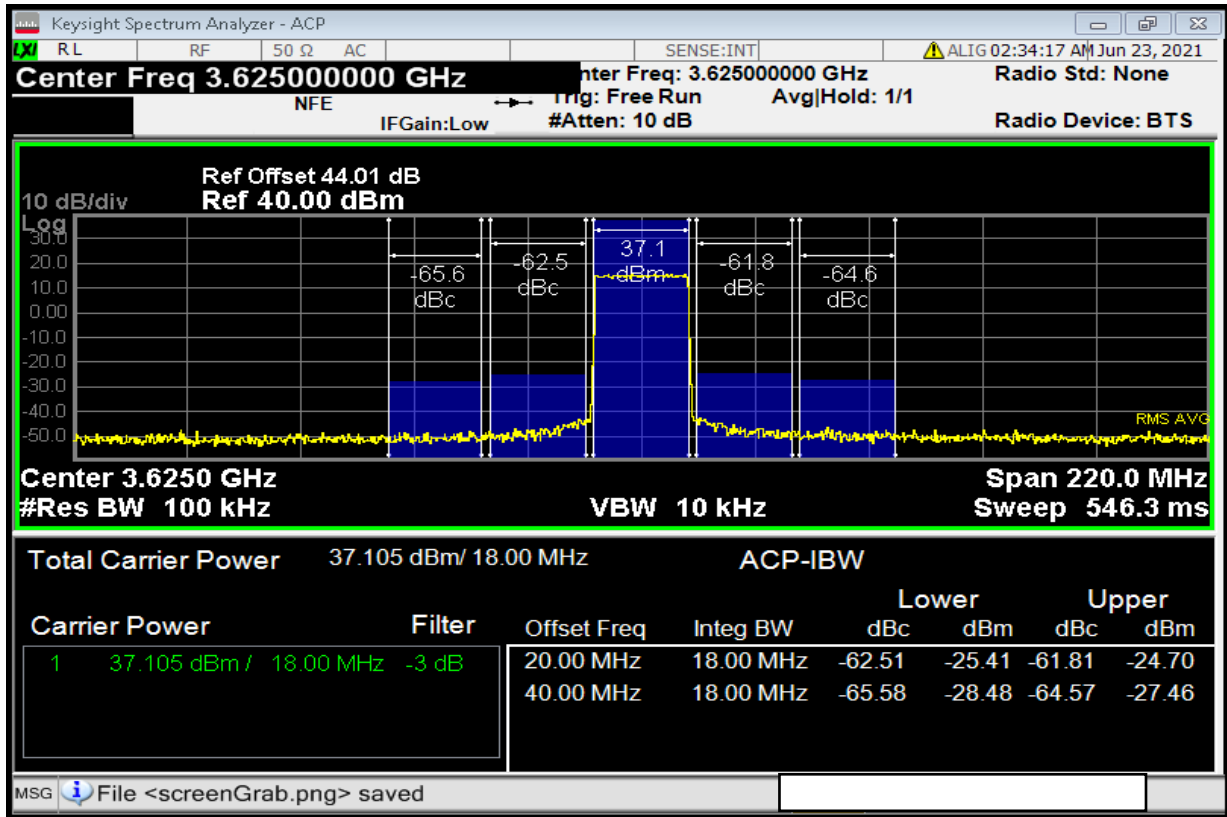


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.112	-29.2	-29.1	-52	-51.8	-57.6	-58.8	-65.3	-65.8

# ADRV9029- Ampleon PA test report

Case 2: Test Signal: 20MHz LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz.

## Post DPD results:

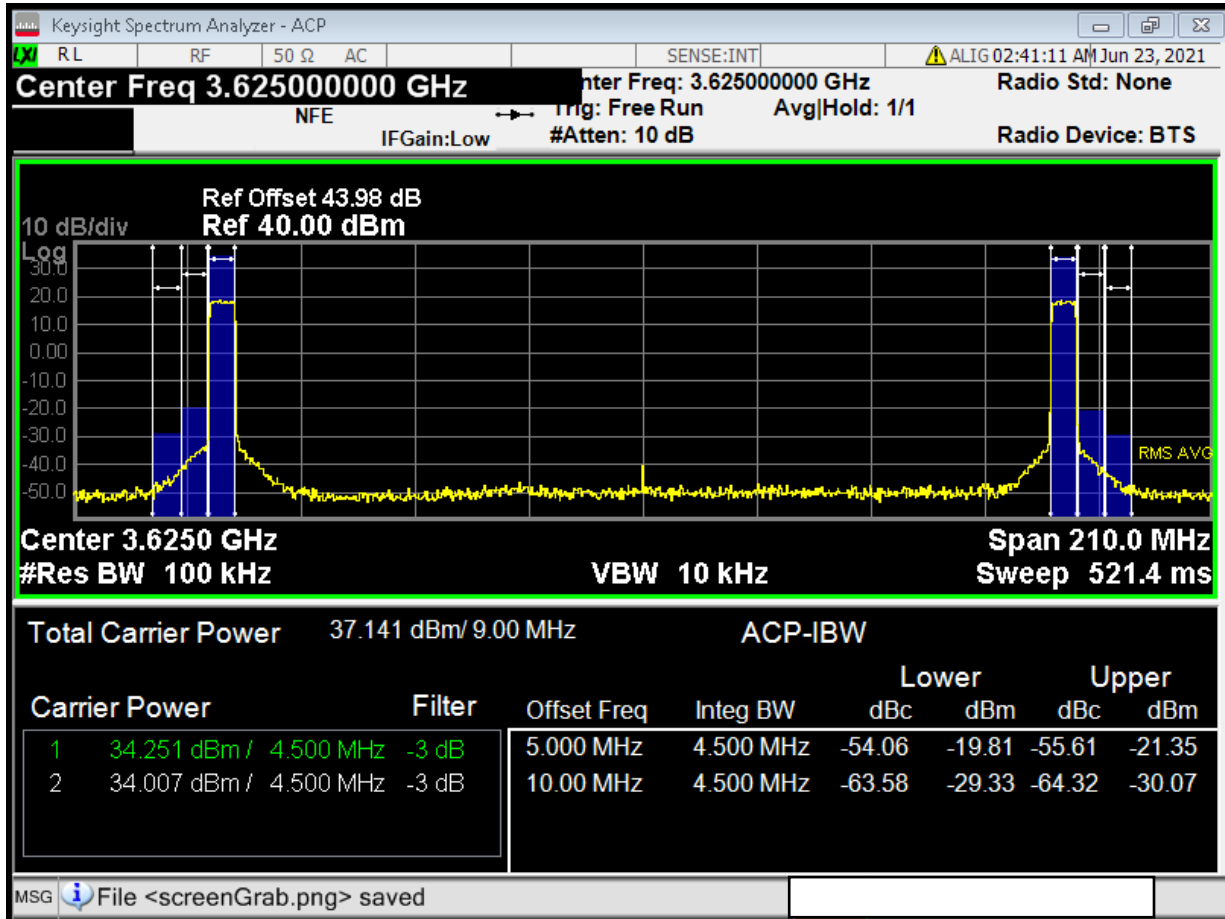


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq:	Pout	DE	VDD	IDD	ACP_Lo	ACP_Hi	ALT1_lo	ALT1_hi	ACP_LO	ACP_HI	ALT1_lo	ALT1_hi
MHz	dBm	%	V	I	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]
3625	37	29.7	29.99	0.112	-29.5	-28.9	-52.3	-52.2	-62.5	-61.8	-65.6	-64.6

# ADRV9029- Ampleon PA test report

Case 3: Test Signal: 2x 5MHz 160MHz LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz

## Post DPD results:

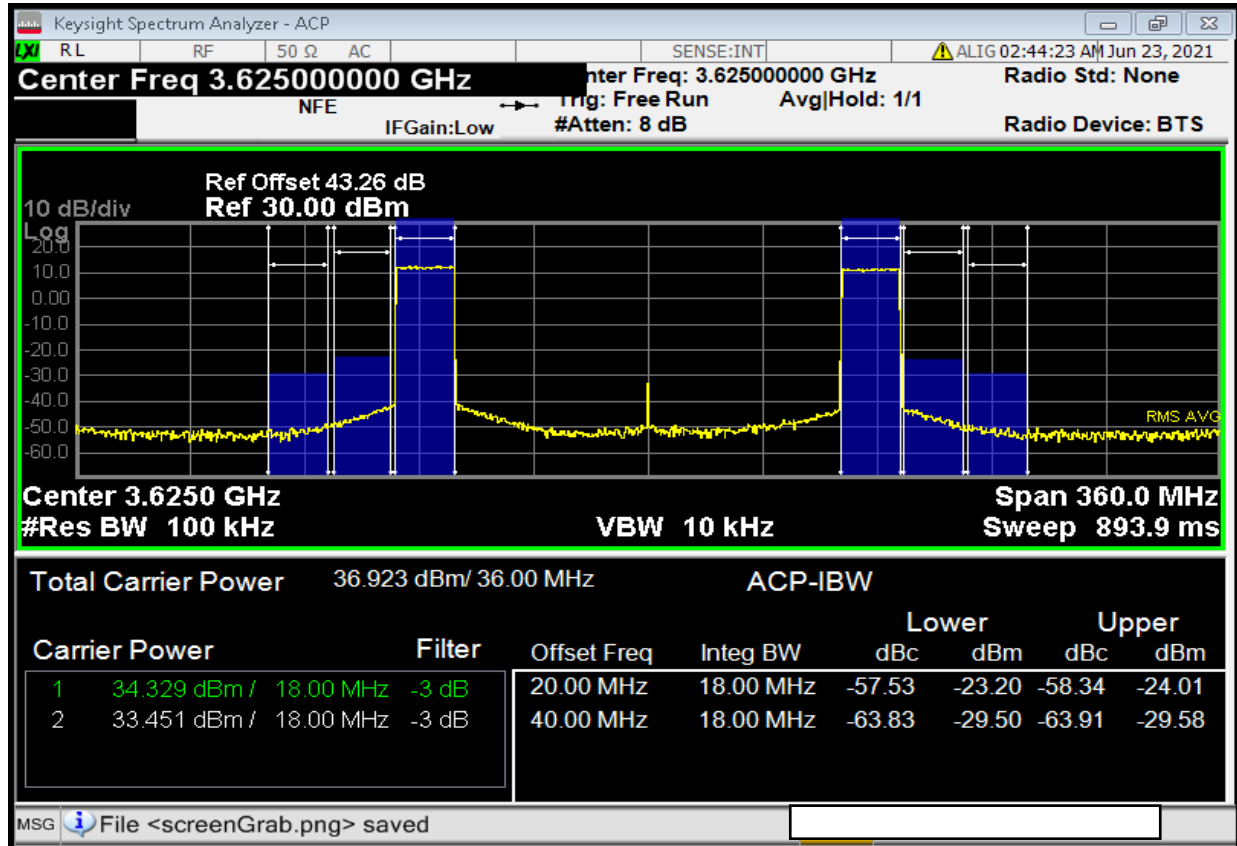


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq:	Pout	DE	VDD	IDD	ACP_Lo	ACP_Hi	ALT1_lo	ALT1_hi	ACP_LO	ACP_HI	ALT1_lo	ALT1_hi
MHz	dBm	%	V	I	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]	[dBc]
3625	37	29.7	29.99	0.112	-30.1	-31.1	-54.5	-55.5	-54.1	-55.6	-63.6	-64.3

# ADRV9029- Ampleon PA test report

Case 4: Test Signal: 2x 20MHz 160MHz LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz

## Post DPD results:

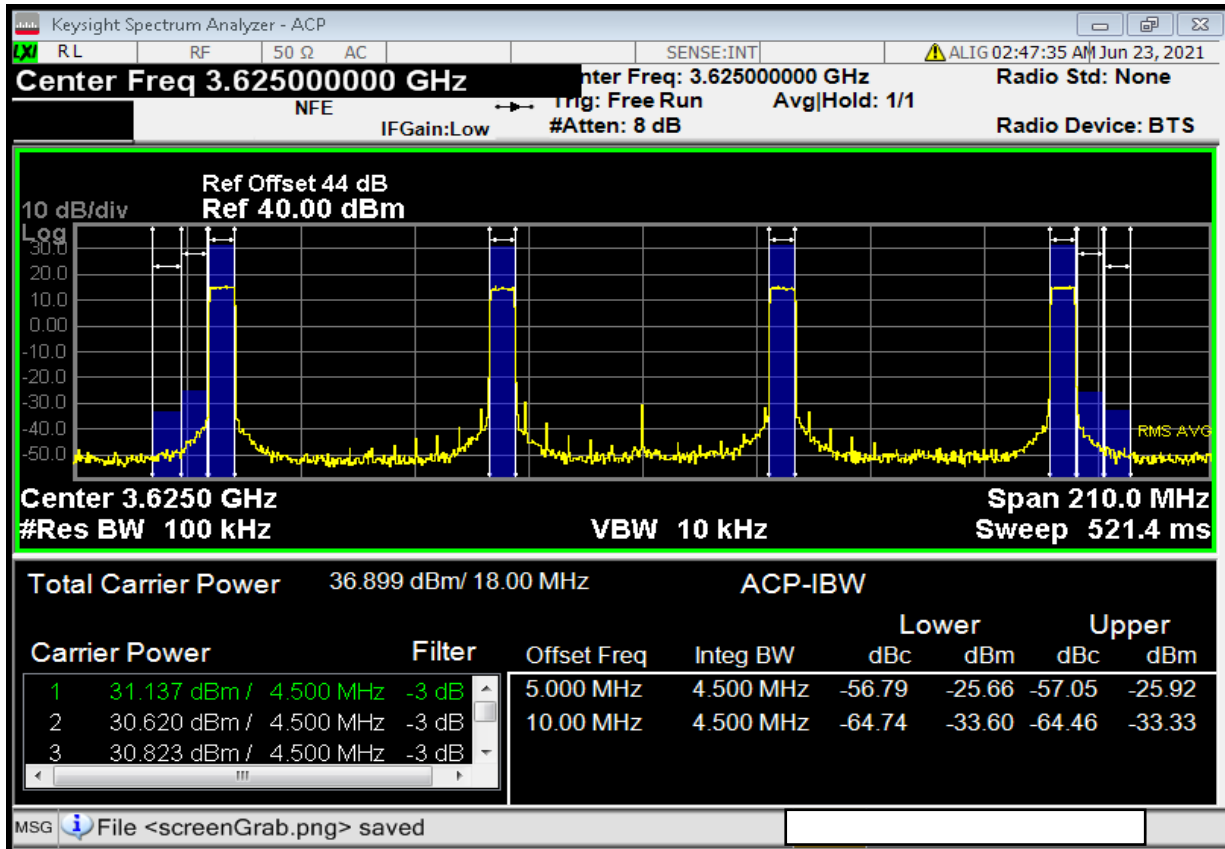


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.113	-30.1	-31.4	-54.2	-56.3	-57.5	-58.3	-63.8	-63.9

# ADRV9029- Ampleon PA test report

Case 5: Test Signal: 4x 5MHz 160MHz LTE (PAR = 8dB), Output Power : 37 dBm, frequency: 3625 MHz

## Post DPD results:



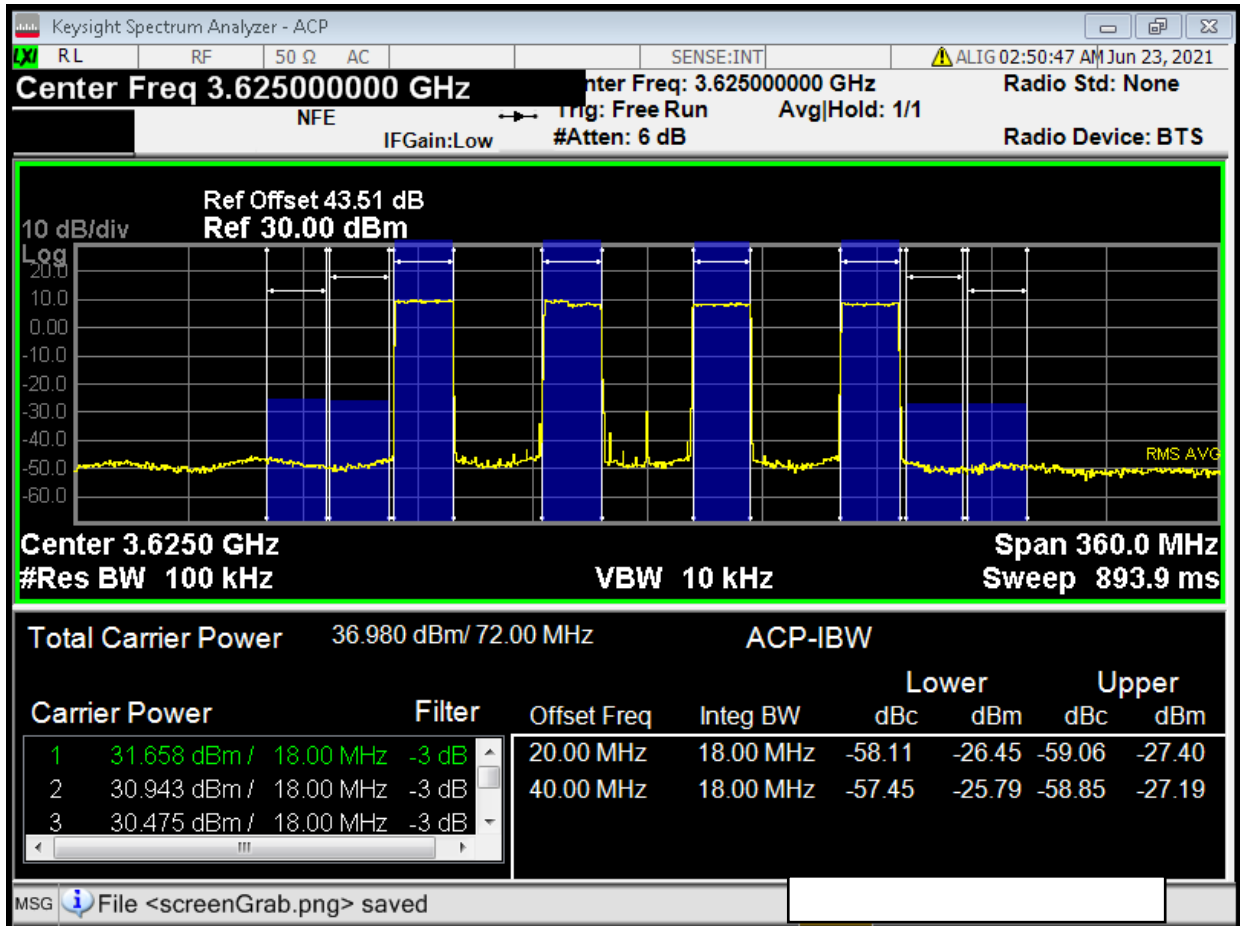
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
					ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.113	-31.2	-31.7	-54.6	-56.2	-56.8	-57.1	-64.7	-64.5



# ADRV9029- Ampleon PA test report

Case 6: Test Signal: 4x 20MHz 160MHz LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz

## Post DPD results:

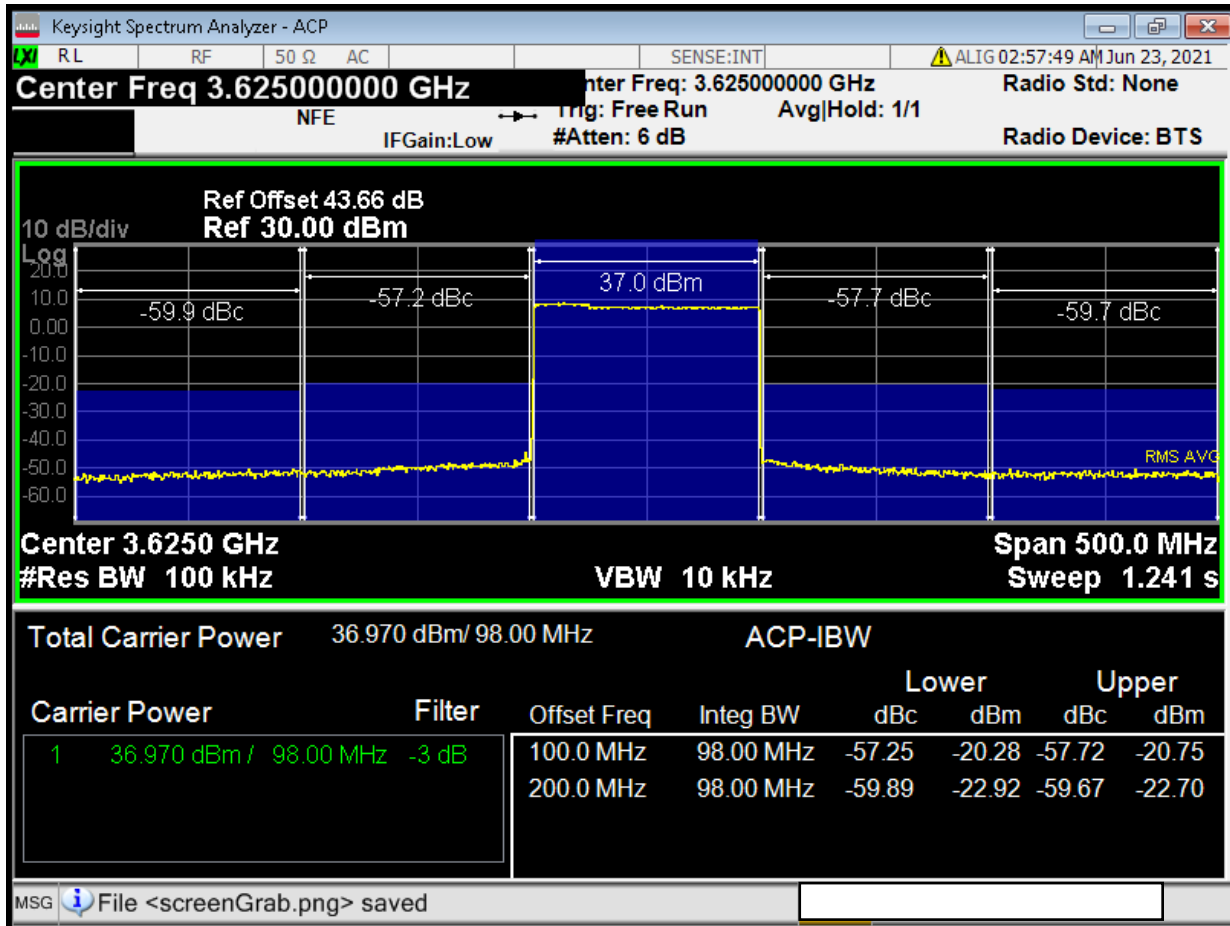


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.113	-30.4	-31.8	-26.7	-28.2	-58.1	-59.1	-57.4	-58.8

# ADRV9029- Ampleon PA test report

Case 7: Test Signal: 1x 100MHz NR LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz

## Post DPD results:

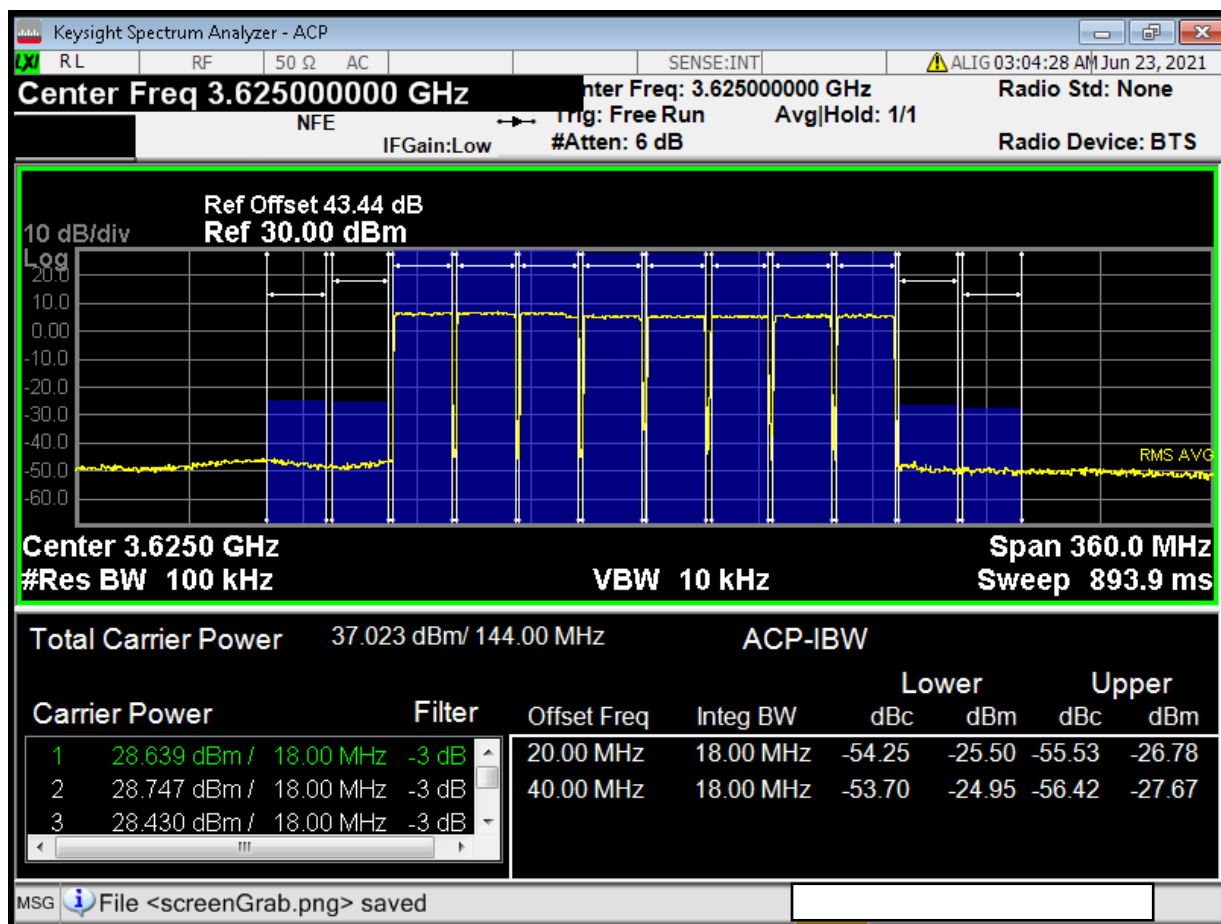


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.112	-27.1	-28.4	-47.0	-50.8	-57.2	-57.7	-59.9	-59.7

# ADRV9029- Ampleon PA test report

Case 8: Test Signal: 8x 20MHz NR LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz

## Post DPD results:

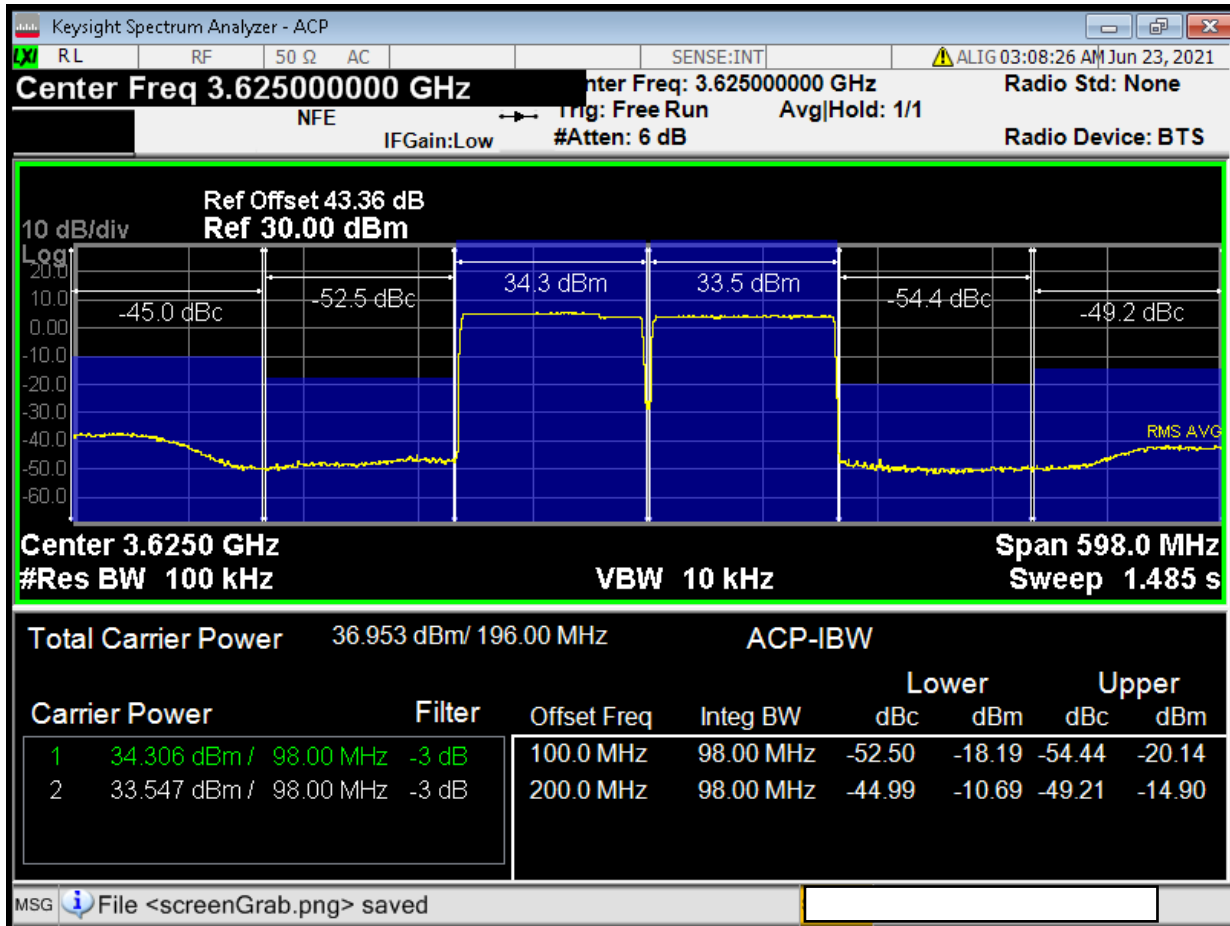


					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.112	-24.1	-25.5	-25.3	-27.0	-54.2	-55.5	-53.7	-56.4

# ADRV9029- Ampleon PA test report

Case 9: Test Signal: 2x 100MHz NR LTE (PAR = 8dB), Output Power: 37 dBm, frequency: 3625 MHz

## Post DPD results:



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3625	37	29.7	29.99	0.113	-24.8	-26.9	-32.3	-35.5	-52.5	-54.4	-45.0	-49.2

## Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.