ADRV9029 DPD results with QORVO PA

Part No: QPA3503

ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

QORVO PA test conditions

Transceiver	ADRV9029
Power Amplifier	QPA3503
Driver Amplifier	MINI Circuits ZVA 183-S+
Application	M-MIMO
Output power	35 dBm (~3.13 Watt)
PA Type	GaN
Frequency Range	3400-3600 MHz
Gain	32.69 dB
Drain Efficiency %	31
P3dB	43.5 dBm
Bandwidth Tested	5*20MHz contiguous 100MHz LTE , non-contiguous 100MHz LTE
ACLR	-51 dBc
Supply Voltage	28V

Test setup

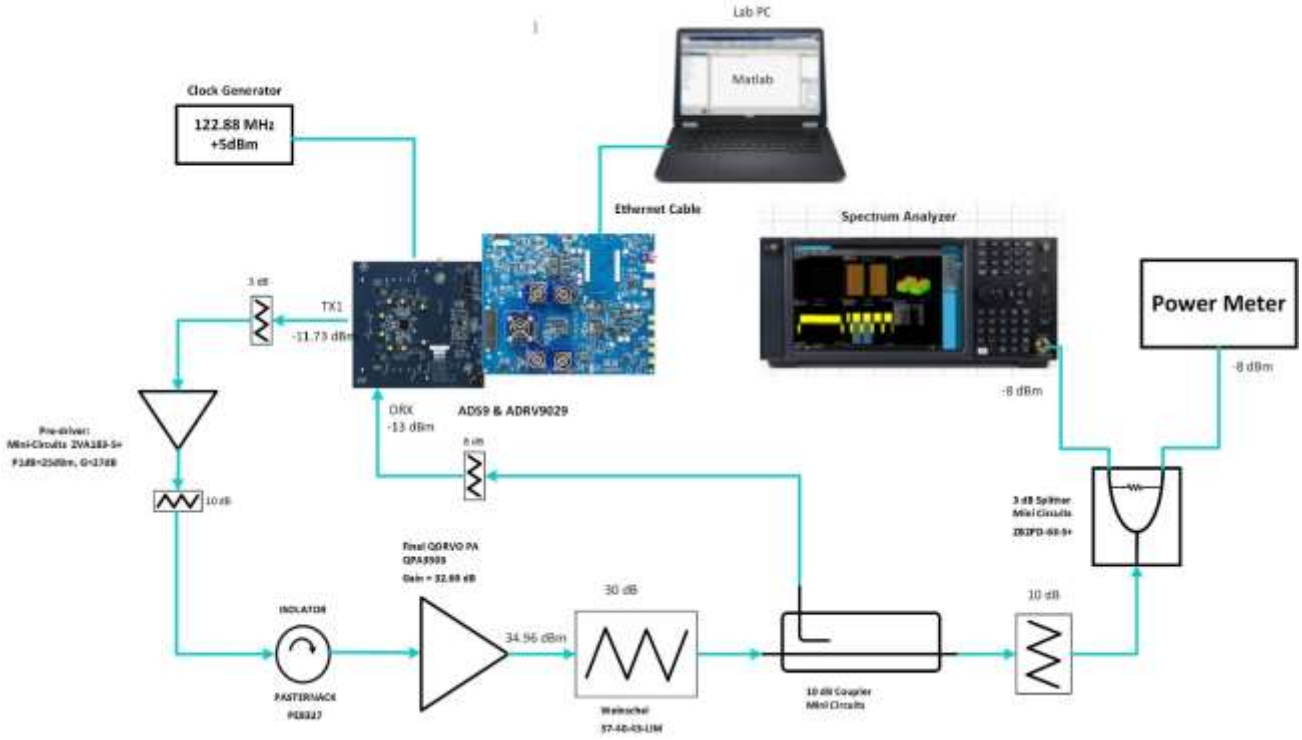


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is broadband QORVO QPA3503. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

In Fig. 1, the GaN Amplifier QPA3503 is loaded with high power attenuator presenting a max VSWR of 1.15 to not detune the PA from its optimum tuning.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design.

Summary

QPA3503 test conditions are:

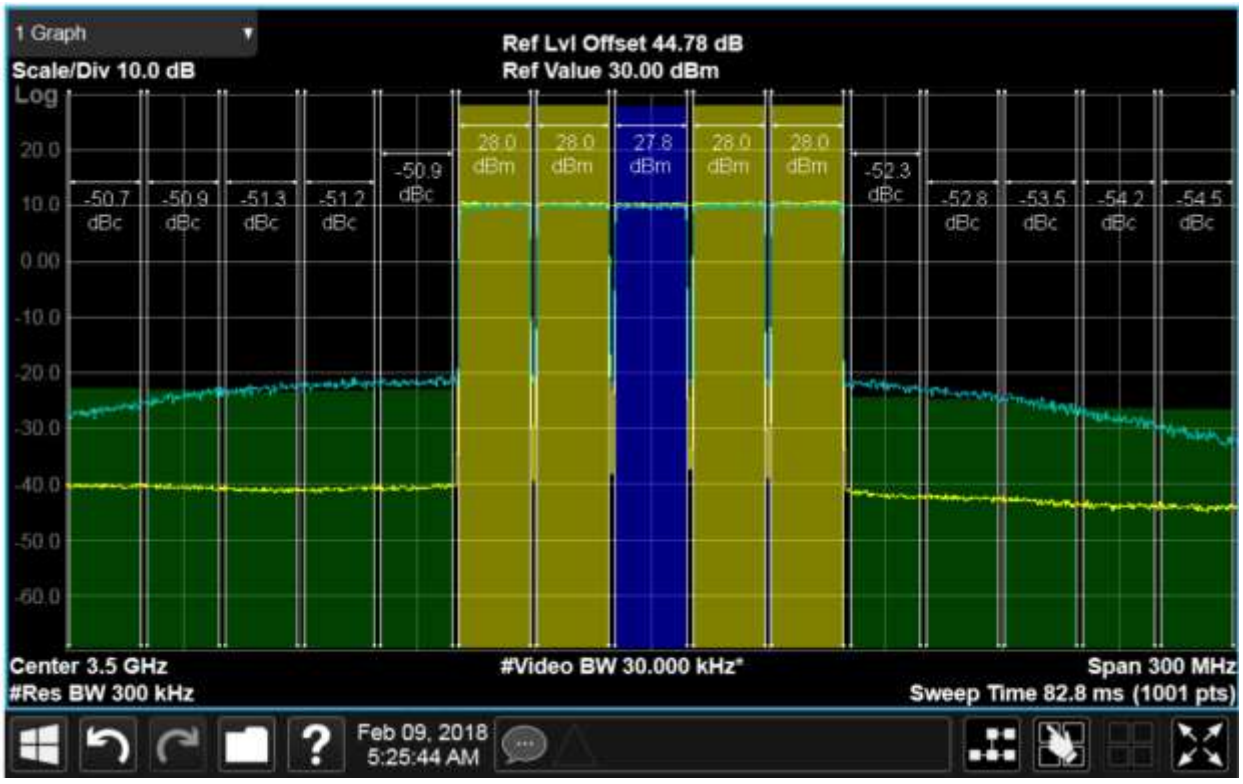
- Center Frequency: 3500 MHz
- Efficiency: 31%
- Average Output Power: 35 dBm (5.13 Watt)
- Test signal: 5*20MHz contiguous 100MHz LTE ,non-contiguous 100MHz LTE

Test Results

Case 1: Test Signal 5*20MHz contiguous 100MHz LTE (PAR = 8dB), Output Power: 35 dBm, Band:3500MHz,

Bias conditions:VDD=28V idq=130mA VgP=-4.5V

Post DPD results:

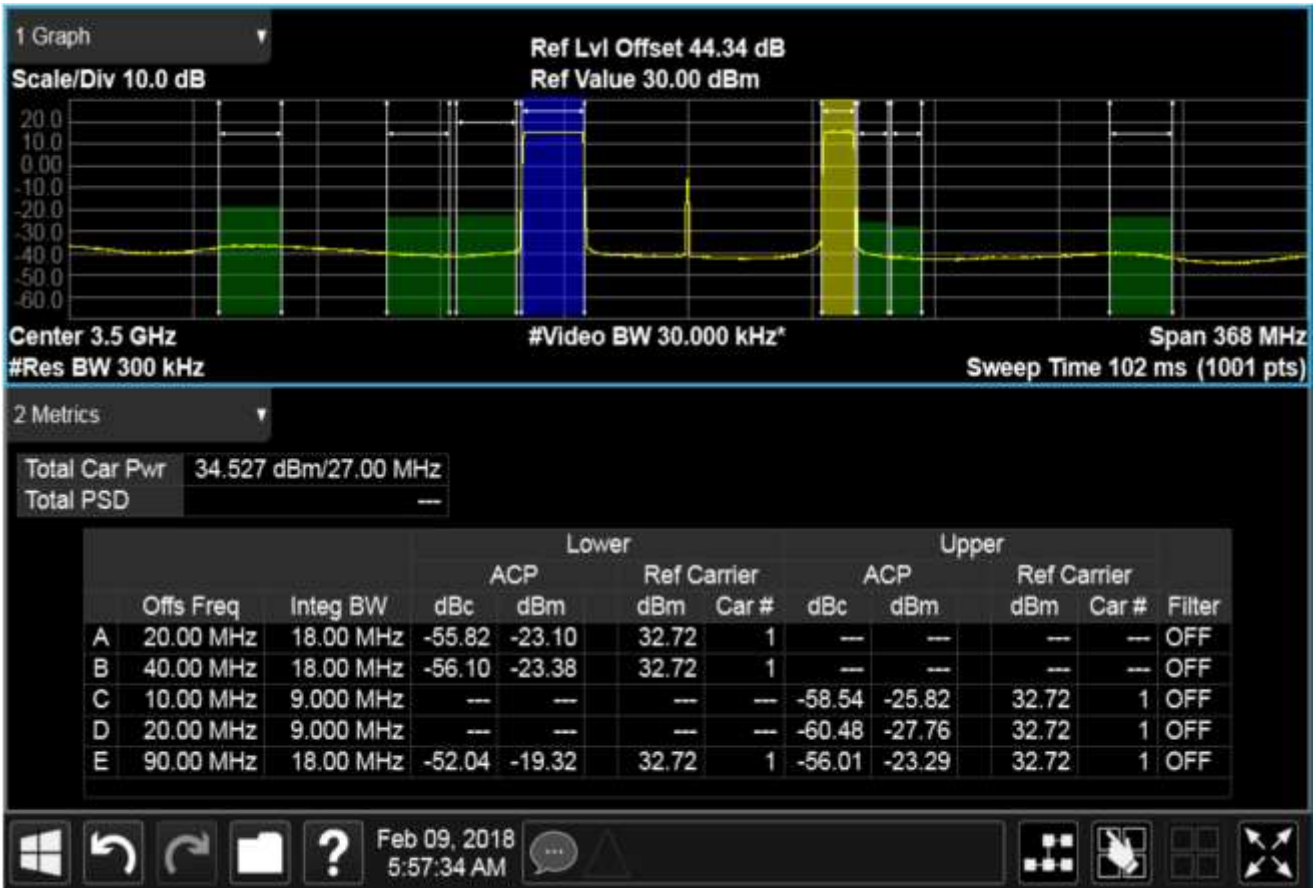


						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3500	35	31	32.69	28	0.36	-32.5	-33	-33	-34.2	-51.3	-52.2	-51.6	-52.5

Case 2: Test Signal non-contiguous 100MHz LTE (PAR = 8dB), Output Power: 35 dBm, Band :3500MHz

Bias conditions:VDD=28V idq=130mA VgP=-4.5V

Post DPD results:



						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3500	34.88	31	32.69	28	0.353	-32.5	-33	-33	-34.2	-55.92	-55.5	-56.15	-57.6

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 5.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.