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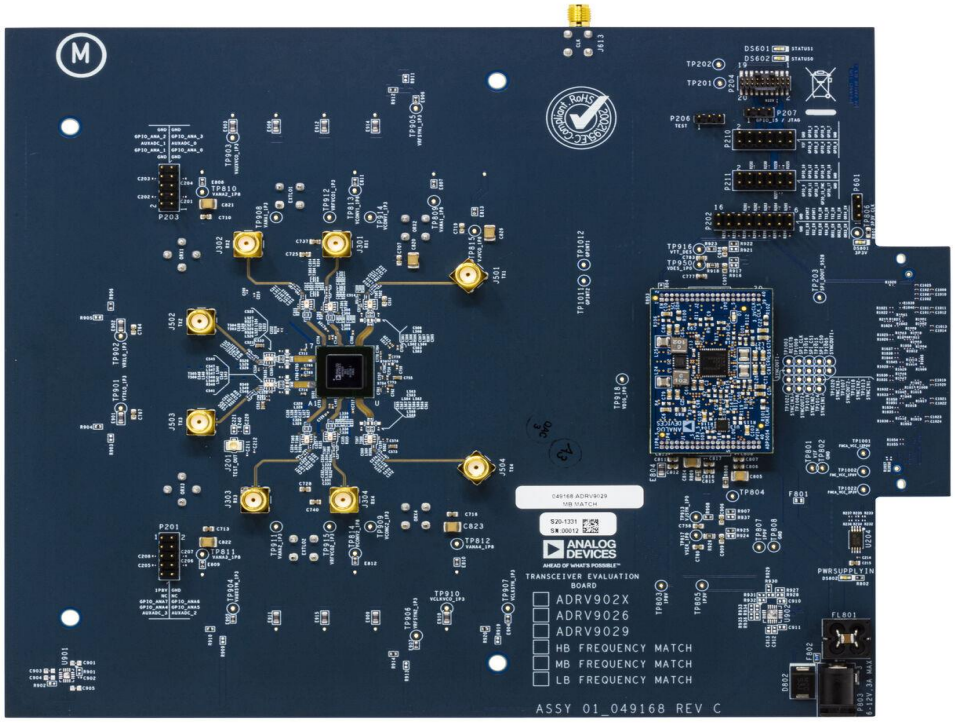
ADRV9029 DPD results with NXP PA

Part No: A2V09H400-04N



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Ampleon PA test conditions

Transceiver	ADRV9029
Power Amplifier	A2V09H400-04N
Driver Amplifier	NXP A2I09VD050GN, Mini-circuit ZVA-183-S+
Application	Macro cell
Output power	47.5 dBm (56 Watt)
PA Type	LDMOS
Frequency Range	780 MHz
Gain	18 dB
Drain Efficiency %	48.61% @47.52dBm
P3dB	57.1 dBm
Bandwidth Tested	10 MHz LTE
ACLR	-51dBc
Supply Voltage	38V,40V,42V

Test setup

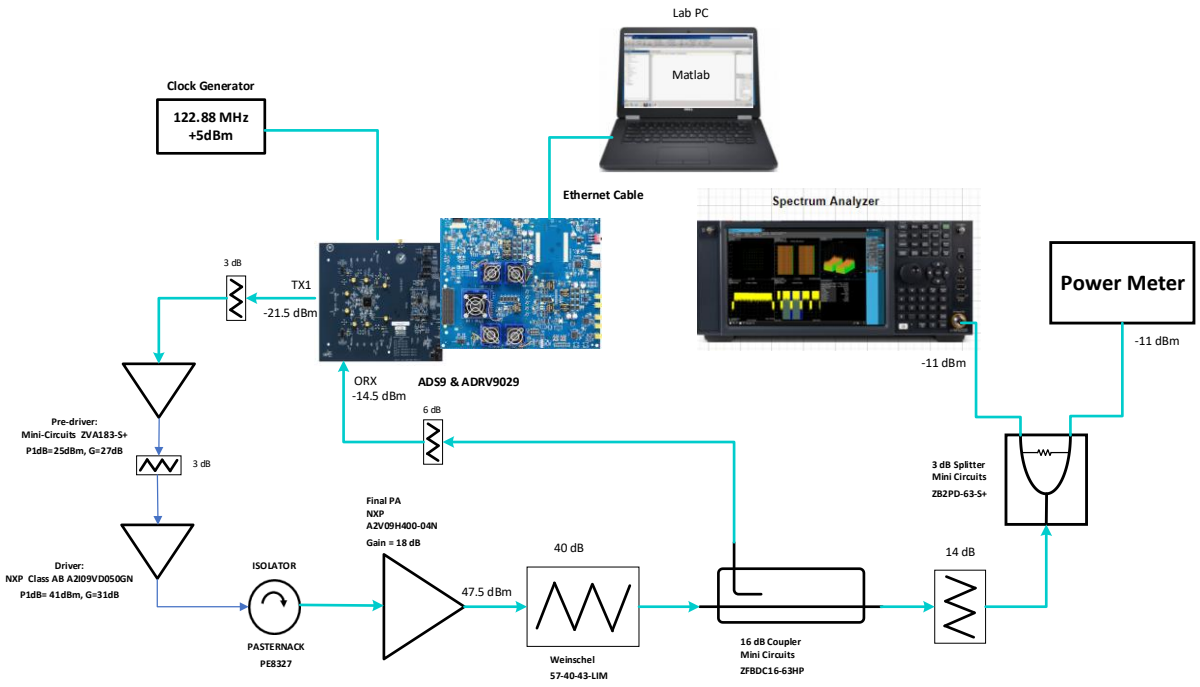


Fig. 1 ADI DPD Test Set up.

Note: The report published is based on measurements done on one PA using ADI test environment. Part-to-part variations might slightly alter the DPD performance. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in slightly different DPD performance.

The Pre-Driver amplifier used is the Mini-circuit ZVA-183-S+ and the driver amplifier used is NXP Class AB A2I09VD050GN. Customers may use different components in their DPD setups. However, careful component selection needs to be performed to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization

Summary

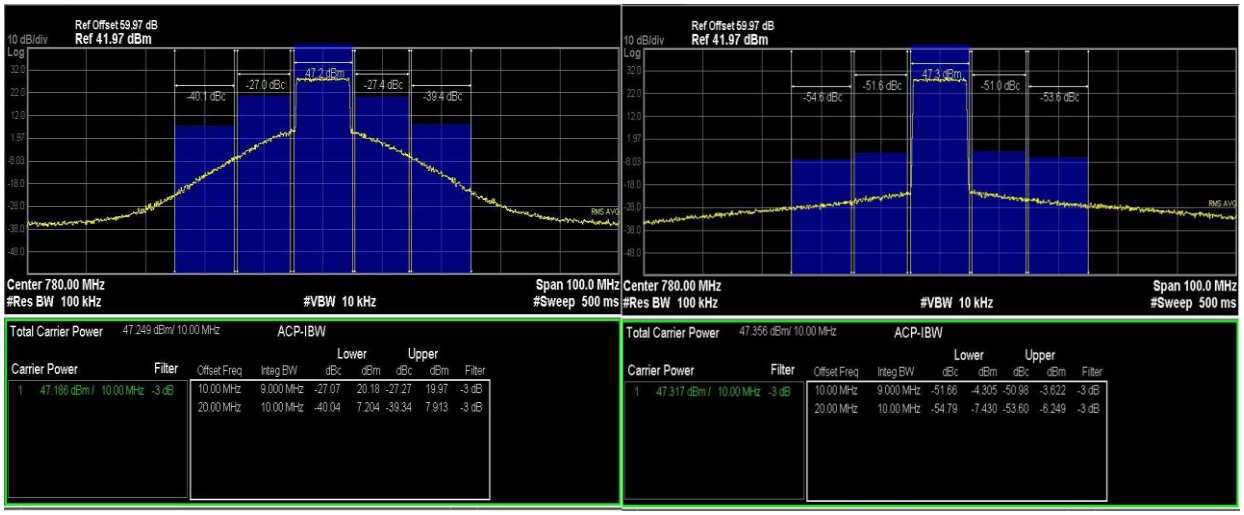
A2V09H400-04N test conditions are:

- Center Frequency: 780 MHz
- Efficiency: 48.6%
- Average Output Power: 47.5 dBm (56 Watt)
- Test signal:10 MHz LTE Signal with 8 dB PAR.
- Bias Conditions: Vdd= 42 V, 40 V and 38 V, VGS1 = 2.39 V, VGS2 = 0.6 V

Test Results

Case 1: Test Signal : 10MHz LTE (PAR = 8dB), Output Power: 47.52 dBm ,VDD=42V,Band 13: 780MHz.

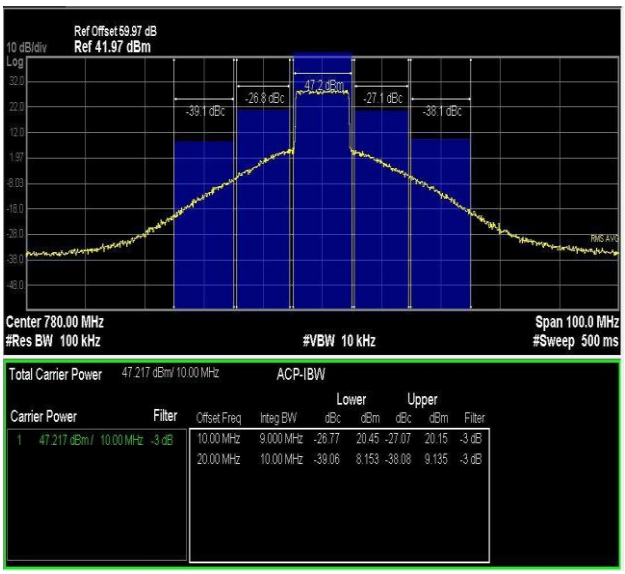
Pre DPD **Post DPD**



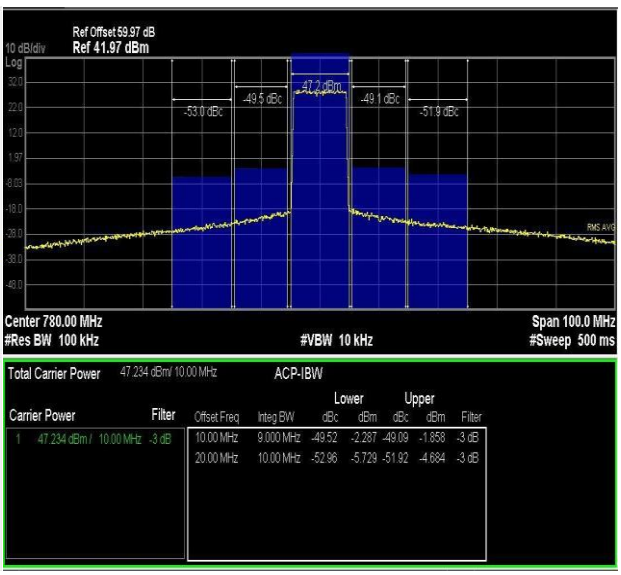
					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
780	47.52	48.6	42	2.76	-27.07	-27.27	-40.04	-39.34	-51.66	-50.98	-54.79	-53.6

Case 2: Test Signal : 10MHz LTE (PAR = 8dB), Output Power: 47.6 dBm , VDD=40V .Band 13: 780MHz.

Pre DPD



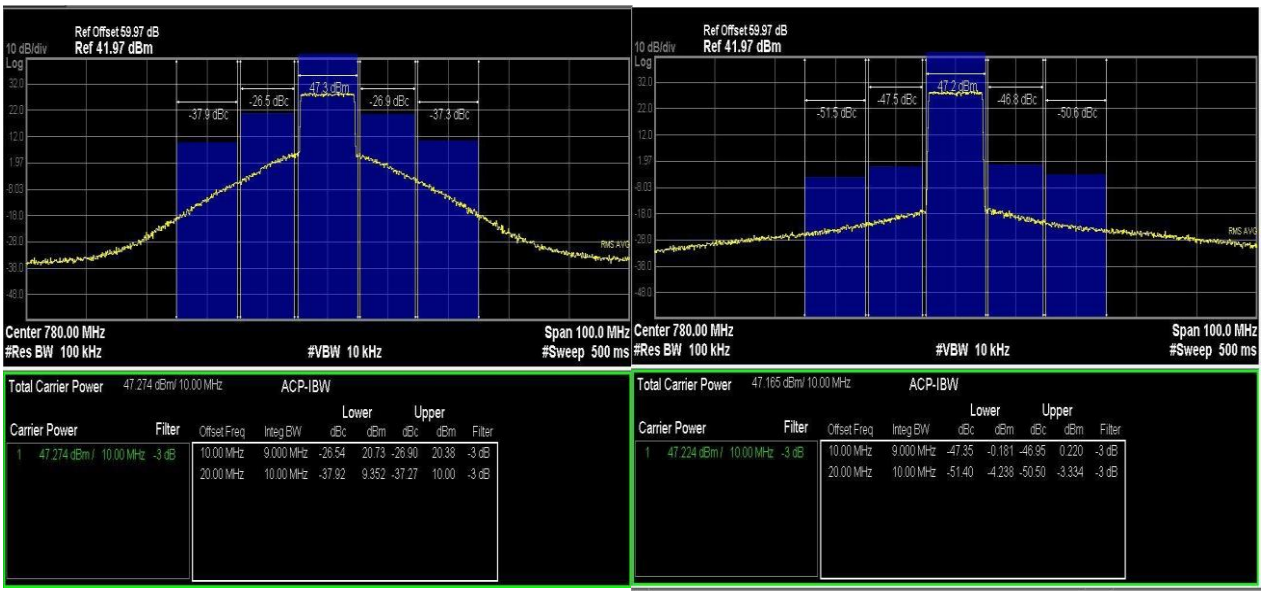
Post DPD



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
780	47.6	49.19	40	2.92	-26.77	-27.07	-39.06	-38.08	-49.52	-49.09	-52.96	-51.92

Case 3: Test Signal : 10MHz LTE (PAR = 8dB), Output Power: 47.59 dBm , VDD=38V, Band13:780MHz.

Pre DPD **Post DPD**



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
780	47.59	49.4	38	3.05	-26.5	-26.9	-37.92	-37.27	-47.35	-46.95	-51.4	-50.5

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.