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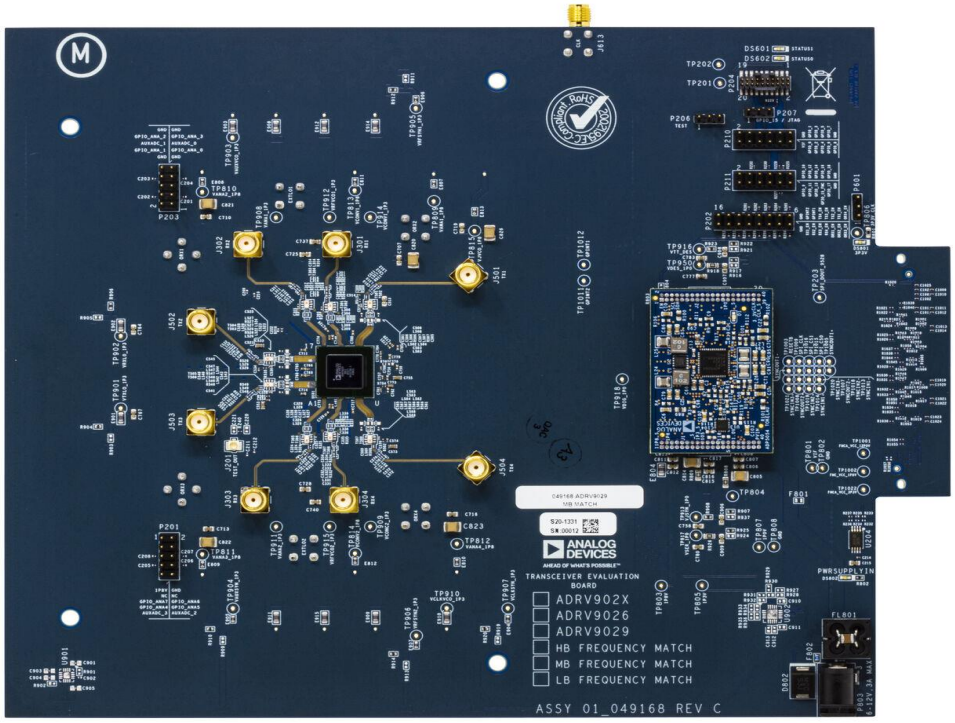
ADRV9029 DPD results with NXP PA

Part No: A3M35TL039



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Ampleon PA test conditions

Transceiver	ADRV9029
Power Amplifier	A3M35TL039
Driver Amplifier	Mini-circuit ZVA-183-S+
Application	M-MIMO
Output power	38.5 dBm (7 Watt)
PA Type	LDMOS
Frequency Range	3500 MHz
Gain	28.3 dB
Drain Efficiency %	39.4% @38.57 dBm
P3dB	47 dBm
Bandwidth Tested	LTE 5*20 100MHz, LTE10*20 200MHz
ACLR	-52 dBc
Supply Voltage	26 V

Test setup

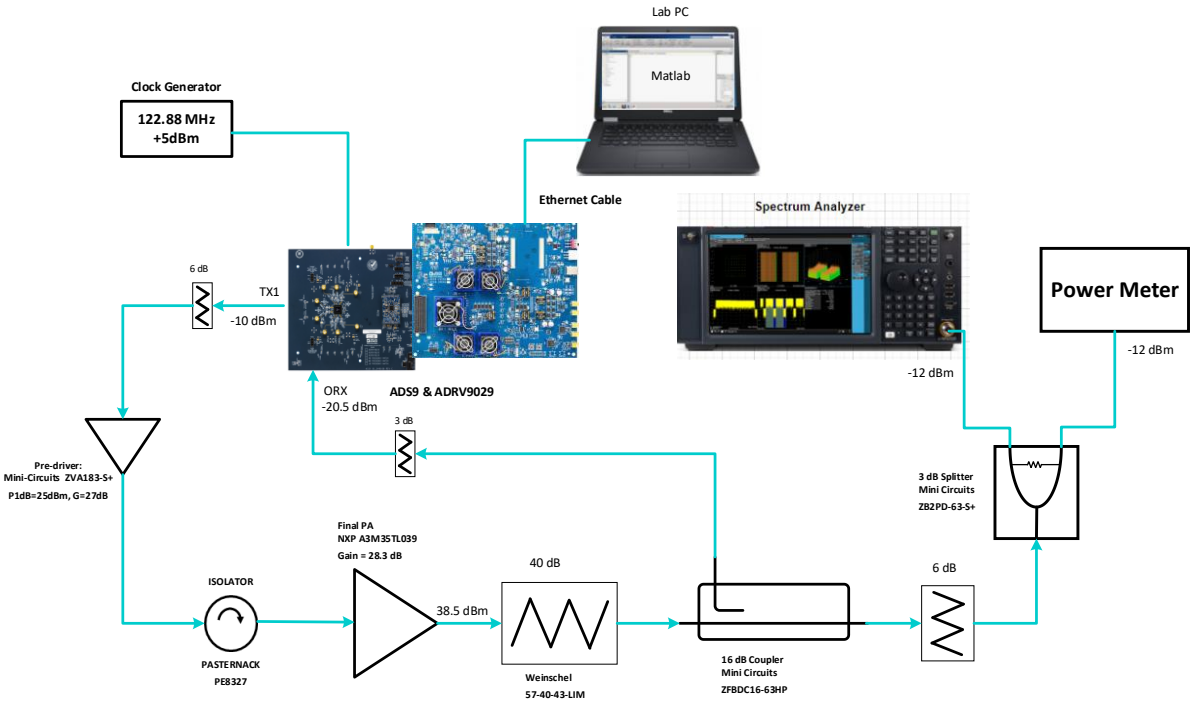


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used is the Mini-circuit ZVA-183-S+. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design. Note that all the performance levels in this report are obtained by running DPD using the model library available in the below link:

https://wiki.analog.com/resources/eval/user-guides/adrv9029/dpd_model_optimization

Summary

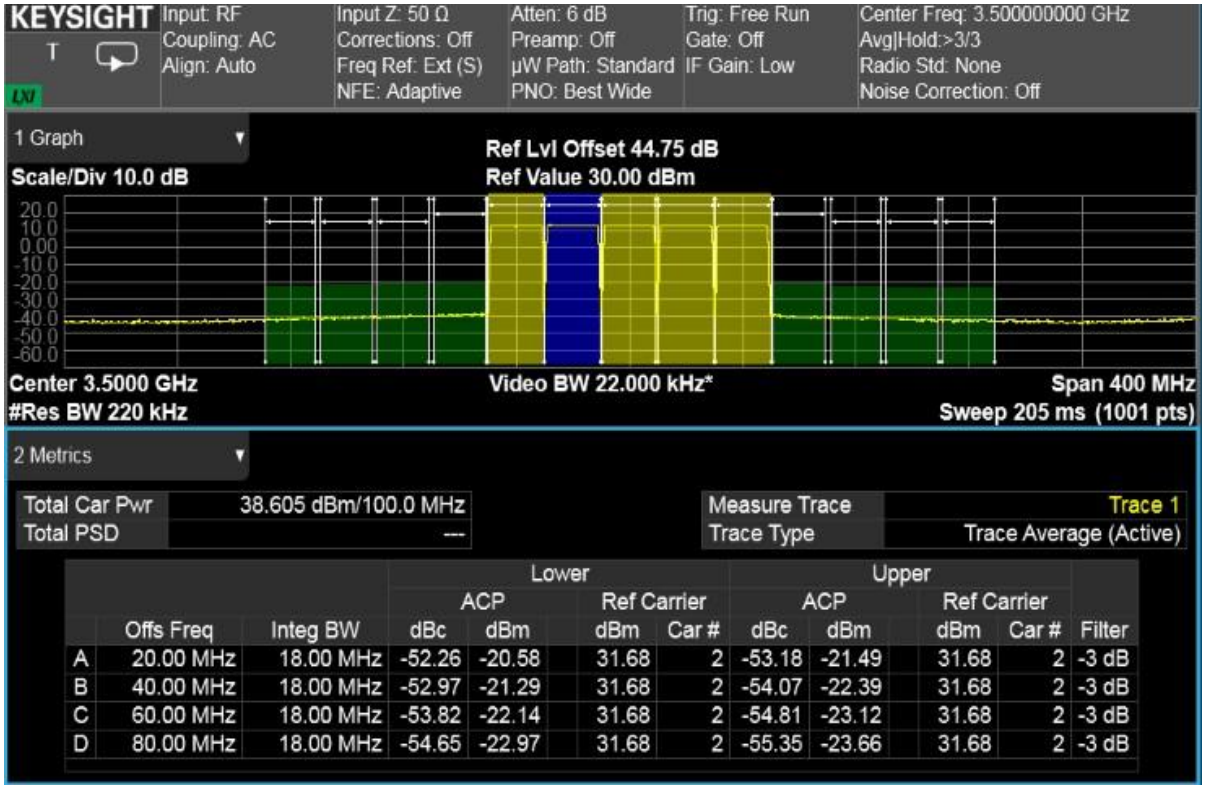
A3M35TL039 test conditions are:

- Center Frequency: 3500 MHz
- Efficiency: 39%%
- Average Output Power: 38.5 dBm (7 Watt)
- Test signal: LTE 5*20 100MHz, 10*20 200MHz with 8 dB PAR.
- Bias Condition: Vdc=VDP = 26V, Idq=97mA, Vg_carr1=5.7V, Vg_carr2=3.3V, Vg_pk1=1.5V,Vg_pk2=1.35V

Test Results

Case 1: Test Signal : 5*20 100MHz LTE (PAR = 8dB), Output Power: 38.57dBm , LTE B42: 3500MHz.

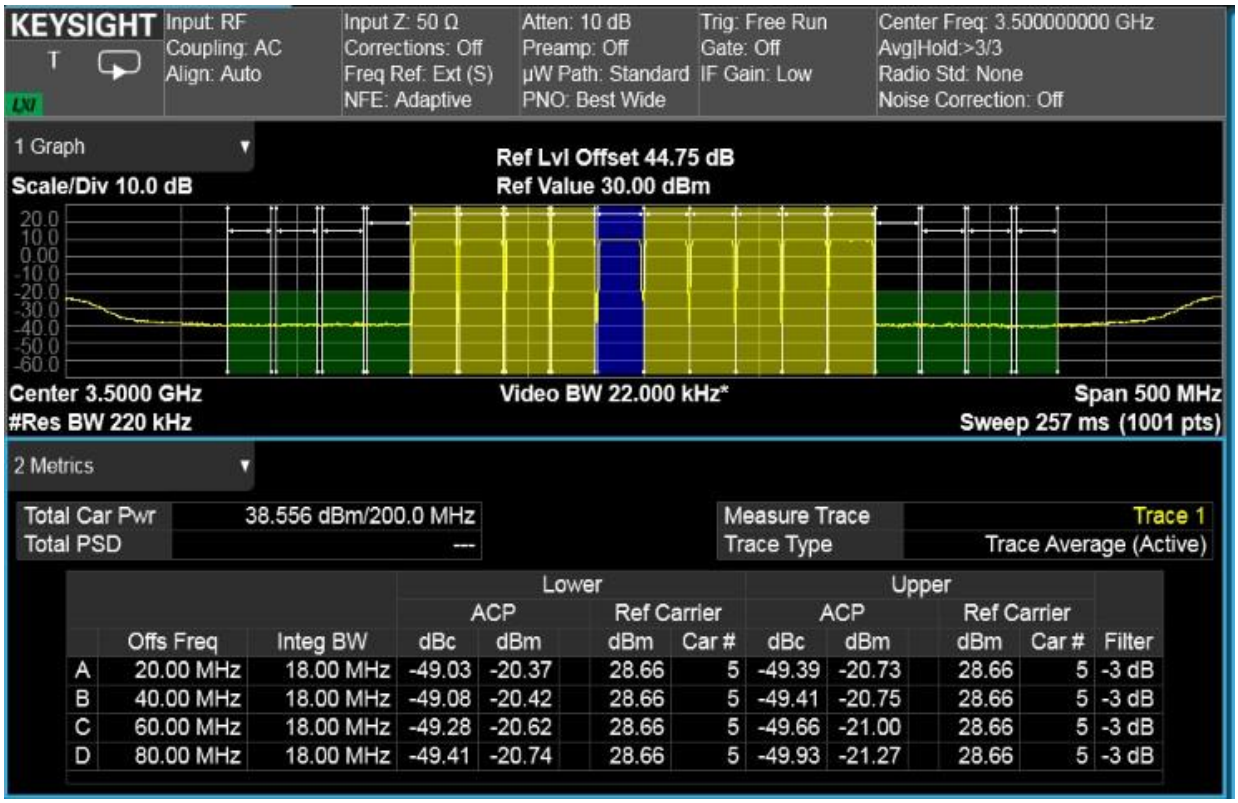
Post DPD results:



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3500	38.57	39.42	26	0.7	-28.6	-27.3	-30.1	-28.6	-52.2	-53.1	-53	-54

Case 2: Test Signal : 10*20 200MHz LTE (PAR = 8dB), Output Power: 38.55dBm , LTE B42: 3500MHz.

Post DPD results:



					Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout dBm	DE %	VDD V	IDD I	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
3500	38.55	38.79	26	0.7	-27.3	-28.7	-28	-28.2	-49	-49.4	-49	-49.4

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.