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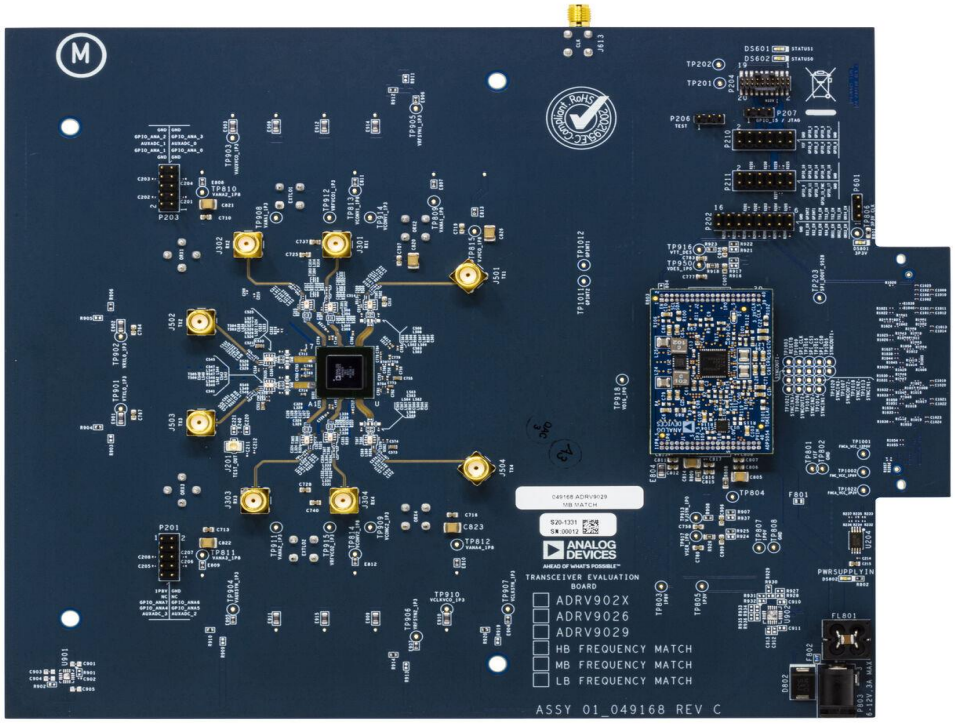
ADRV9029 DPD results with WOLFSPEED PA

Part No: WS1A3940



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Wolfspeed PA test conditions

Transceiver	ADRV9029
Power Amplifier	WS1A3940
Driver Amplifier	Mini Circuits ZVA183-S+
Application	M-MIMO
Output power	39.5 dBm (~9 Watt)
PA Type	LDMOS
Frequency Range	3700-3980 MHz
Gain	14dB
Drain Efficiency %	44.30
P3dB	48 dBm
Bandwidth Tested	1x5MHz LTE, 1x20MHz LTE, 2x20MHz LTE 160MHz, 4x20MHz LTE 160MHz, 1x100MHz NR
ACLR	-49.20 dBc
Supply Voltage	48V

Test setup

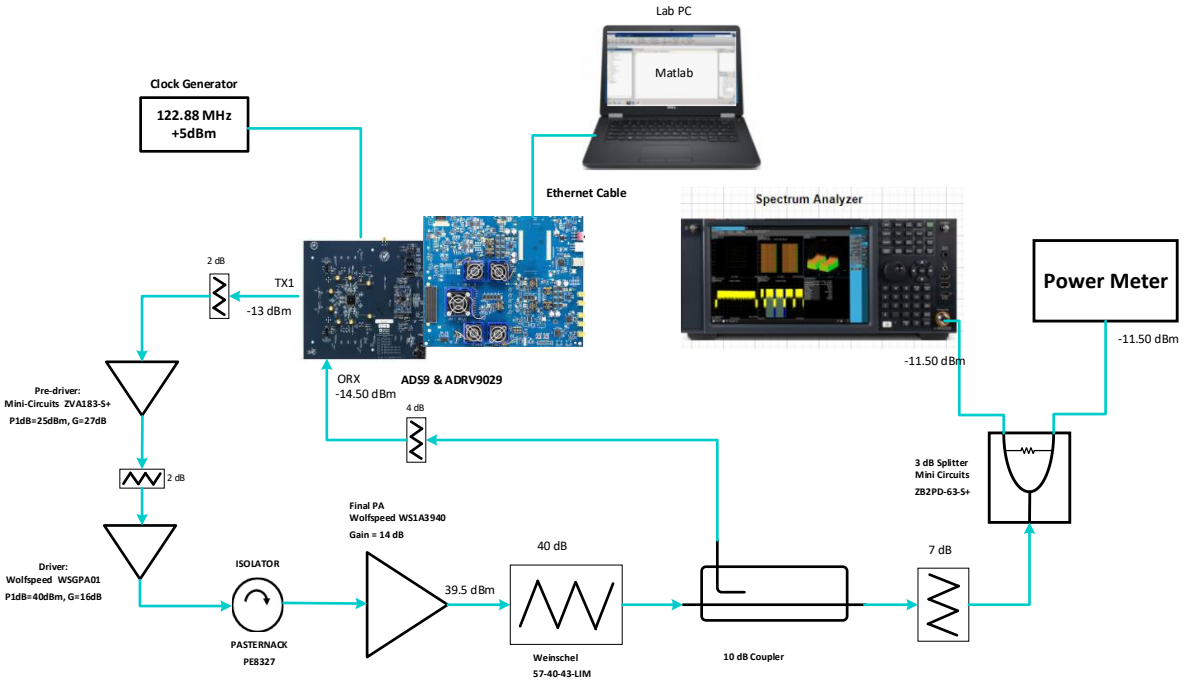


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is broadband Mini circuits ZVA183-S+. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

In Fig. 1, the Doherty Amplifier WS1A3940 is loaded with high power attenuator presenting a max VSWR of 1.15 to not detune the PA from its optimum tuning.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design.

Summary

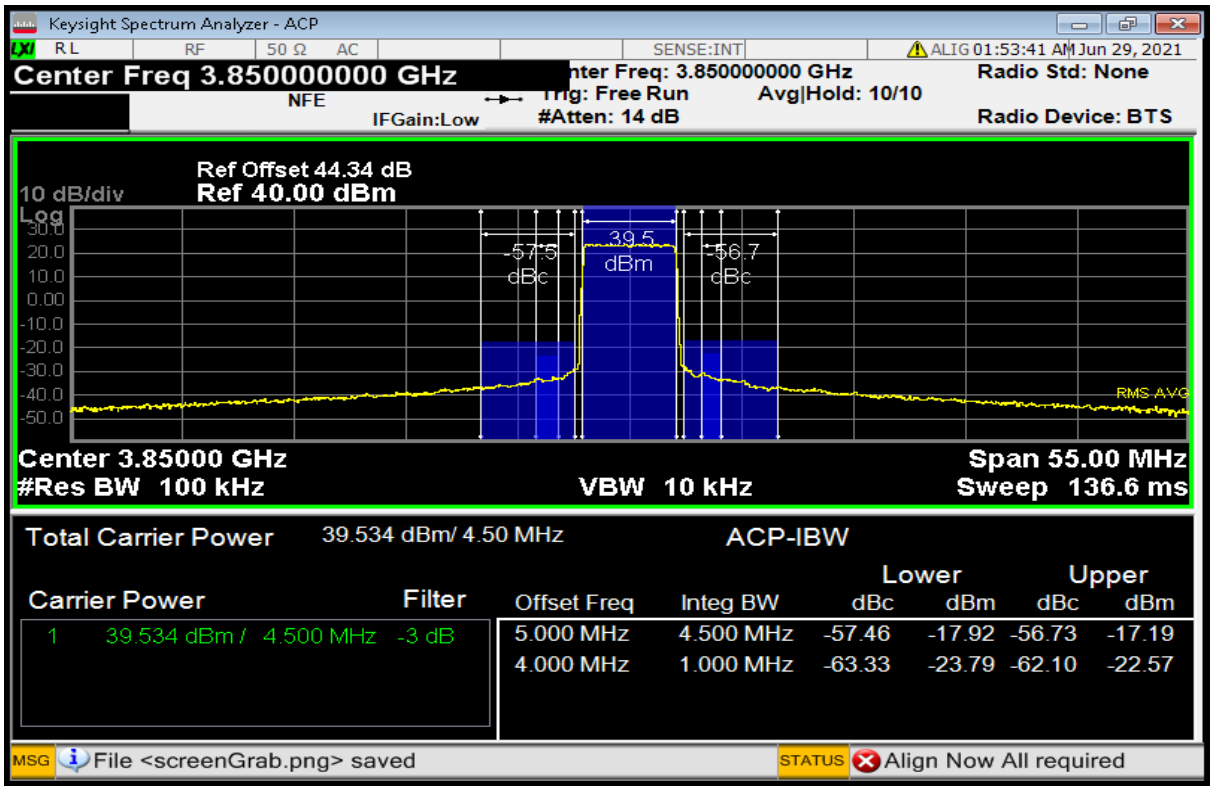
AFSC5G26E37 test conditions are:

- Center Frequency: 3850 MHz
- Efficiency: 44.30%
- Average Output Power: 39.5 dBm (8.91 Watt)
- Test signal: 1x5MHz LTE, 1x20MHz LTE, 2x20MHz LTE 160MHz, 4x20MHz LTE 160MHz & 8x20MHz LTE
- Bias conditions: Vdd: 48.00 V , 69.00 mA, Vgc: 2.84 V , 0.00 mA, Vgp: 5.00 V , 0.00 mA, Vgd: 2.90 V, -0.20 mA

Test Results

Case 1: Test Signal 1x5MHz LTE (PAR = 8dB), Output Power: 39.40 dBm

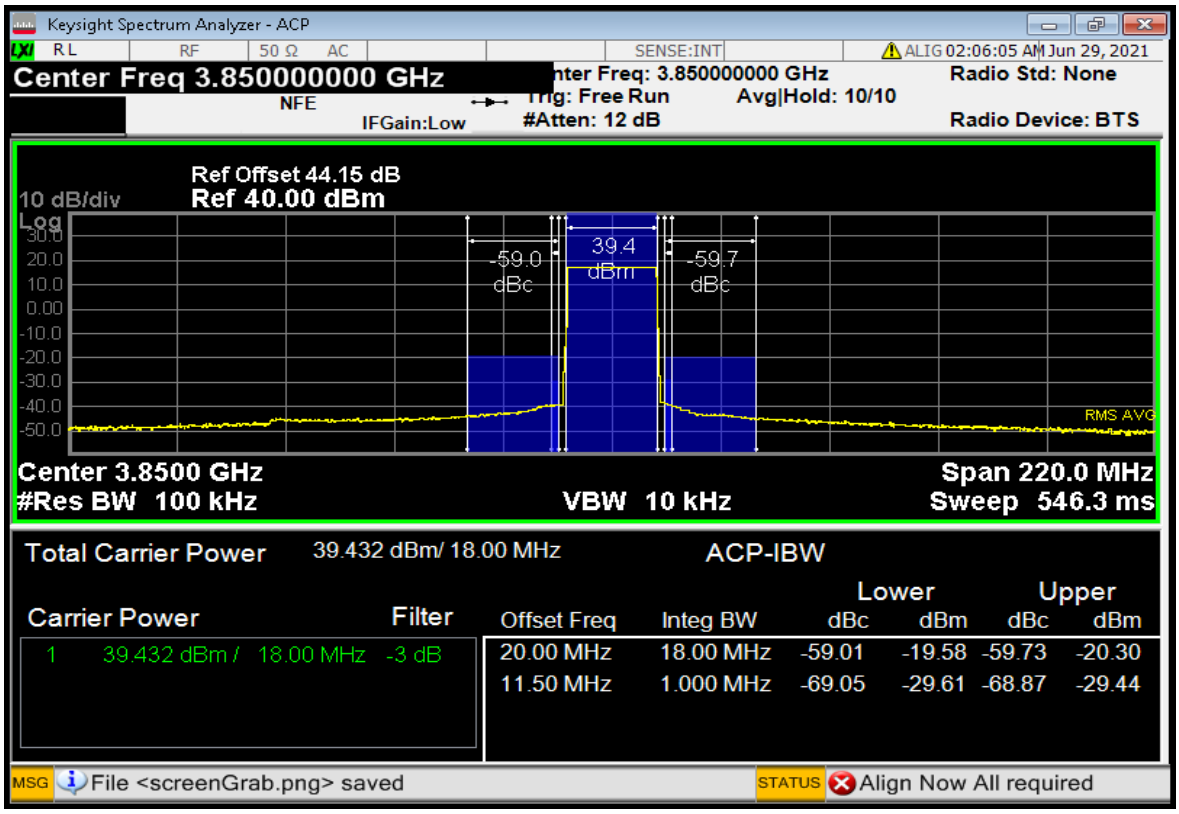
Post DPD results:



						Open Loop [Pre-DPD]		Closed Loop [Post-DPD]	
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]
3850	39.40	43.50	14.00	48	0.42	-28.60	-28.70	-57.50	-56.70

Case 2: Test Signal: Test Signal 1x20MHz LTE (PAR = 8dB), Output Power: 39.50 dBm

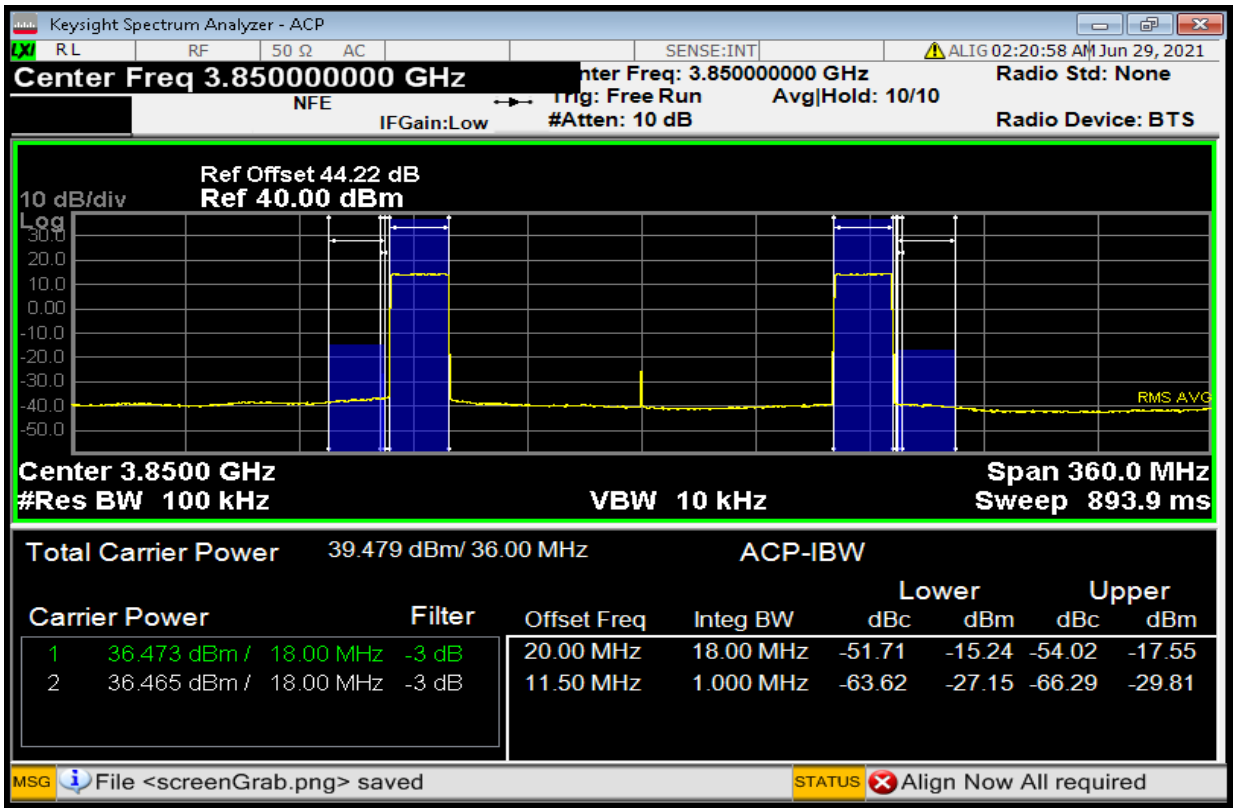
Post DPD results:



						Open Loop [Pre-DPD]		Closed Loop [Post-DPD]	
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]
3850	39.50	43.60	14.00	48	0.42	-28.40	-29.00	-59.00	-59.70

Case 3: Test Signal 2x20MHz LTE 160 MHz (PAR = 8dB), Output Power: 39.50 dBm

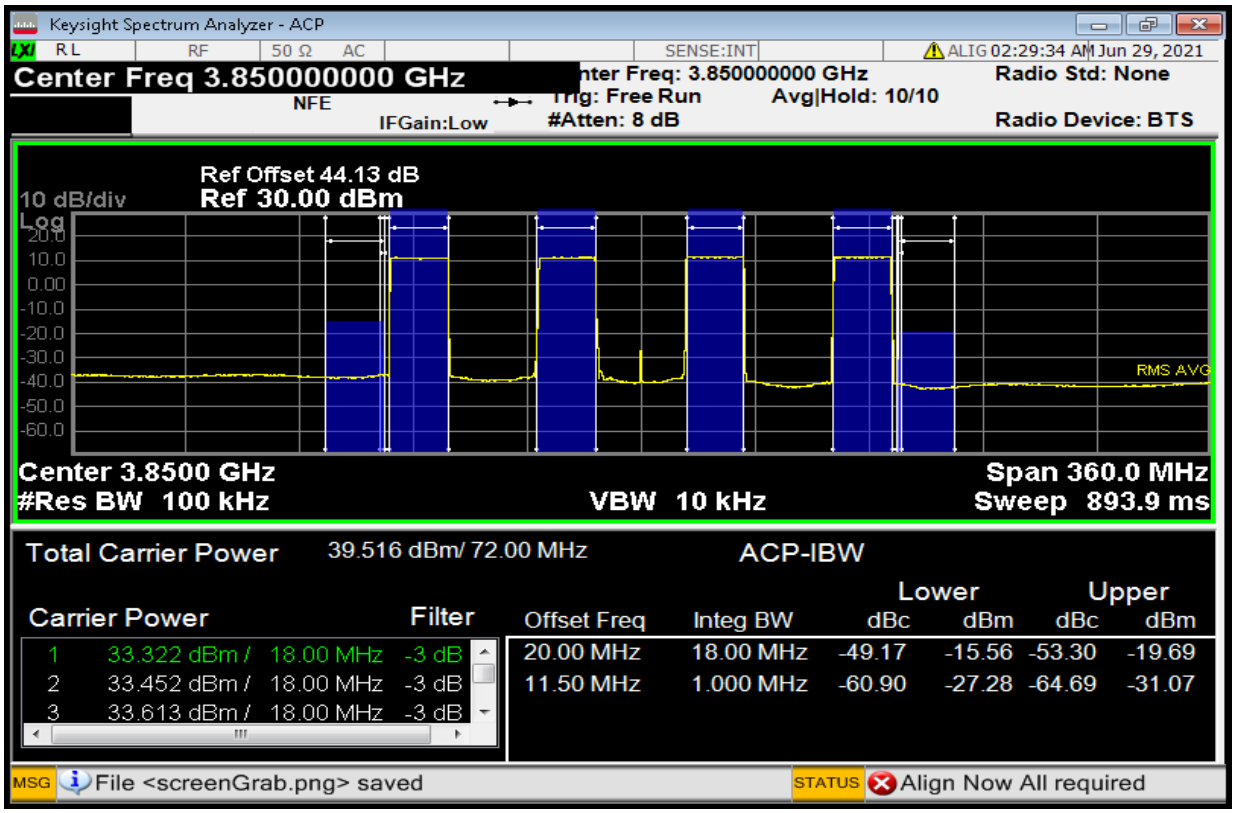
Post DPD results:



						Open Loop [Pre-DPD]		Closed Loop [Post-DPD]	
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]
3850	39.50	43.30	13.00	48	0.43	-29.90	-33.60	-51.70	-54.00

Case 4: Test Signal 4x20MHz LTE 160 MHz (PAR = 8dB), Output Power: 39.50 dBm

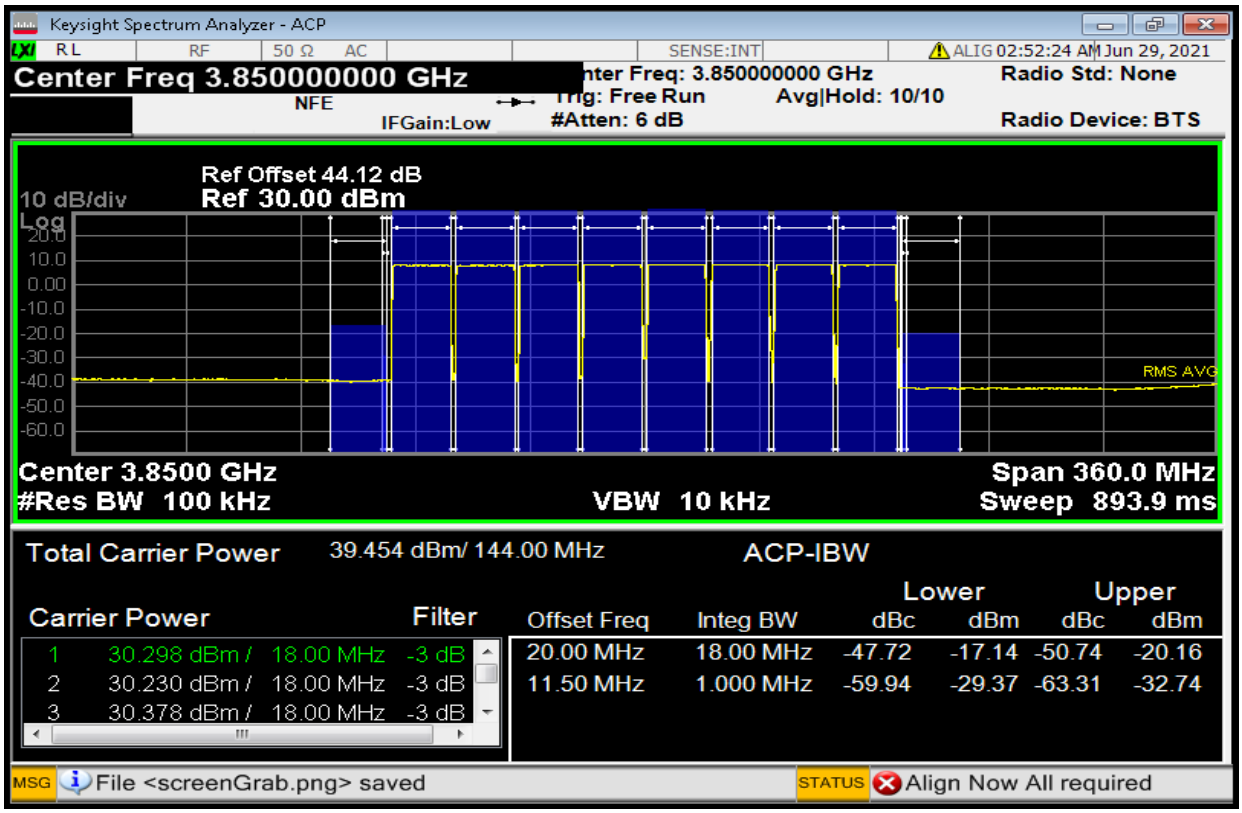
Post DPD results:



						Open Loop [Pre-DPD]		Closed Loop [Post-DPD]	
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]
3850	39.50	43.60	13.00	48	0.43	-29.80	-33.50	-49.20	-53.30

Case 5: Test Signal 8x20MHz LTE (PAR = 8dB), Output Power: 39.50 dBm

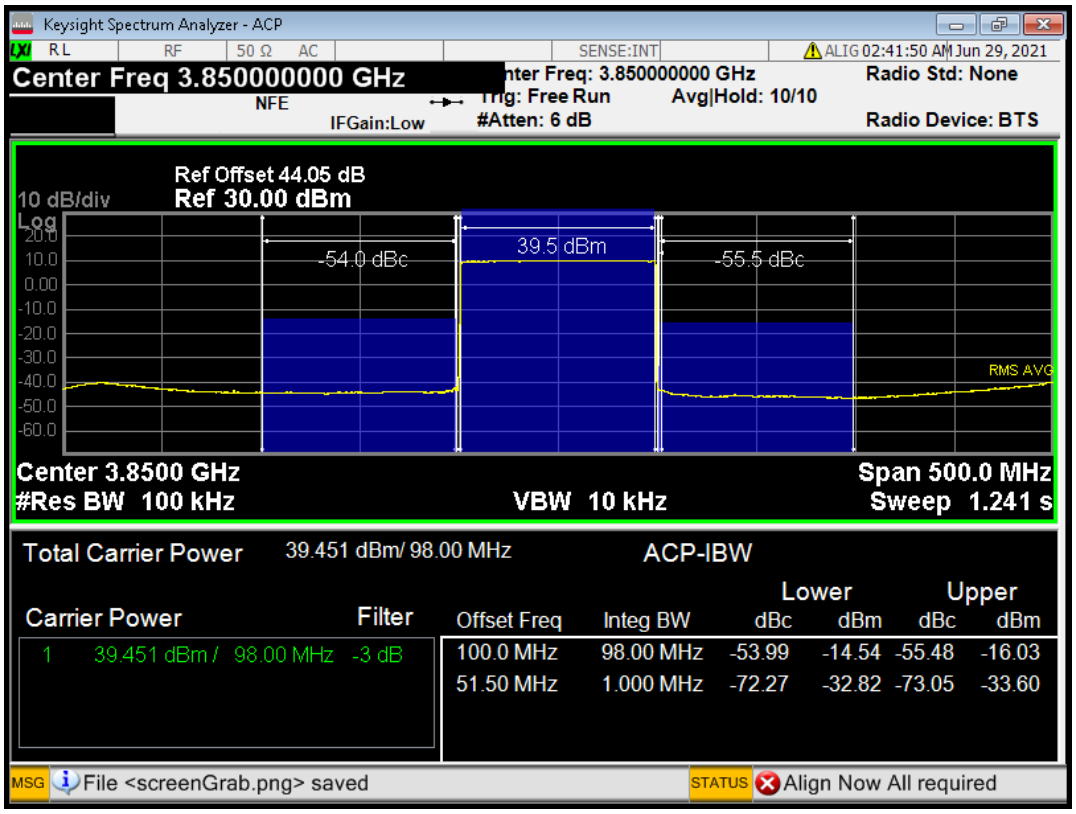
Post DPD results:



						Open Loop [Pre-DPD]		Closed Loop [Post-DPD]	
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]
3850	39.50	43.70	13.00	48	0.42	-23.30	-27.30	-47.70	-50.70

Case 6: Test Signal 1x100MHz NR (PAR = 8dB), Output Power: 39.50 dBm

Post DPD results:



						Open Loop [Pre-DPD]		Closed Loop [Post-DPD]	
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]
3850	39.40	43.70	13.00	48	0.42	-26.60	-30.10	-54.00	-55.50

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.