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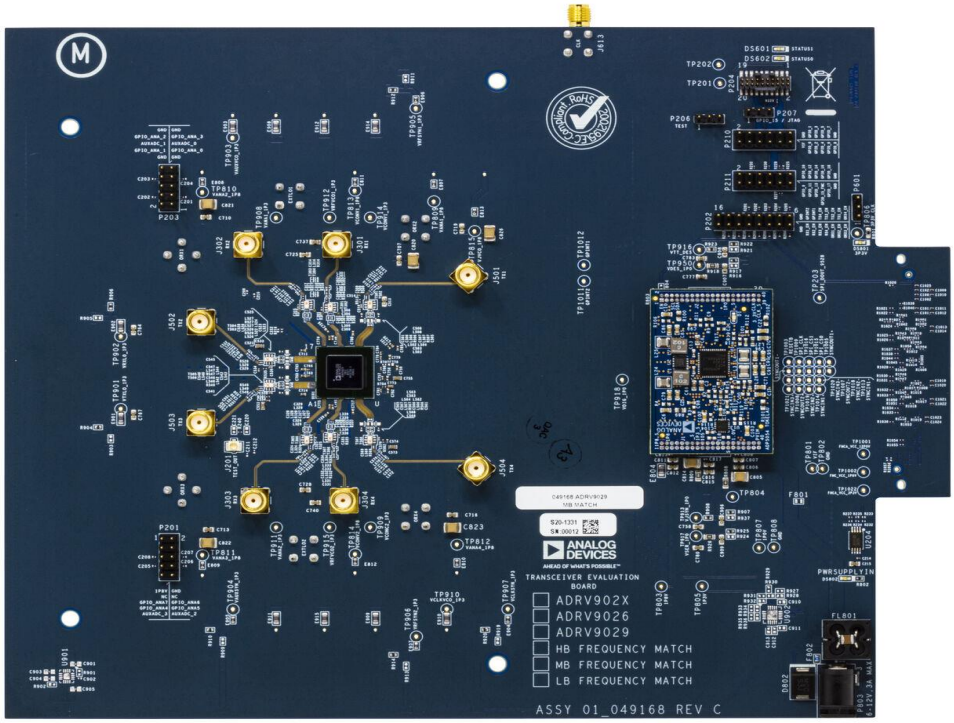
ADRV9029 DPD results with WOLFSPEED PA

Part No: WS1A2639



ADRV9029 Evaluation Board with on-chip Digital Predistortion Solution

Introduction:

In this report, we present DPD results using the ADRV9029 on-chip DPD using the following setup configuration:

User Case: 51C_Non-LinkSharing

Sampling rate: 245.76Msps

JESD Lane rate: 16.22016Gbps

DFE (CFR ,DPD): Enabled

LOL correction: Enabled

Wolfspeed PA test conditions

Transceiver	ADRV9029
Power Amplifier	WS1A2639
Driver Amplifier	WSGPA01
Application	M-MIMO
Output power	38.8 dBm (~7.6 Watt)
PA Type	MMIMO
Frequency Range	2600 MHz
Gain	18.8
Drain Efficiency %	48
P3dB	46.99 dBm
Bandwidth Tested	LTE 100MHz
ACLR	-49.52 dBc
Supply Voltage	48V

Test setup

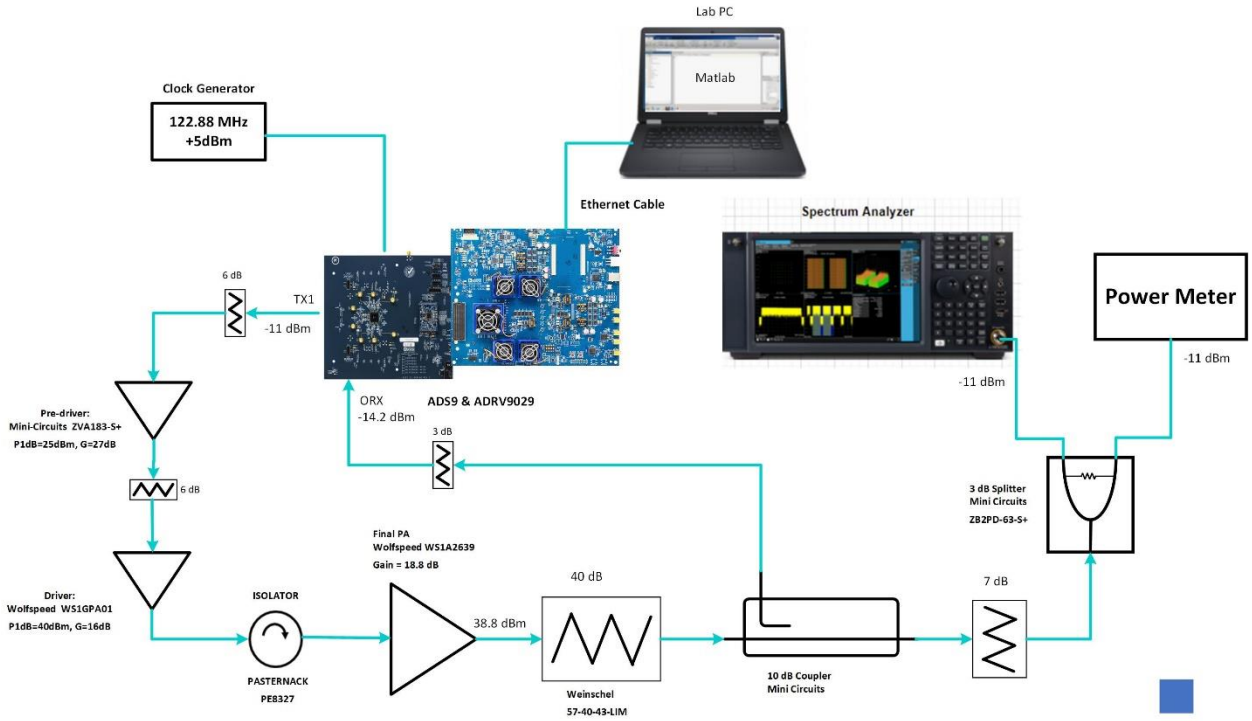


Fig. 1 ADI DPD Test Set up.

Note: The reports published are measurements done on single PA using ADI test environment. that there can be slight DPD performance difference due to part-to-part variations. PA vendors might release other versions of this same EVB with enhanced efficiency and linearity performance. Also, using a custom PA design based on this PA part number may results in different DPD performance.

The Driver amplifier used in Fig. 1 is broadband Wolfspeed WSGPA01. Customers may use different components in their DPD setups. However, careful component selection needs to be performed in order to be able to reproduce the DPD results published in this report.

In Fig. 1, the Doherty Amplifier WS2B2640 is loaded with high power attenuator presenting a max VSWR of 1.15 to not detune the PA from its optimum tuning.

We encourage our customers to evaluate the ADRV9029 DPD performance using evaluation board using the test conditions in this report. It is important to start by testing the evaluation board provided by the PA vendor with the recommended bias values and duplicate the DPD results in this report before proceeding with the custom PA design.

Summary

WS1A2639 test conditions are:

- Center Frequency: 2600 MHz
- Efficiency: 48%
- Average Output Power: 38.8 dBm (7.6 Watt)
- Test signal: LTE 100 MHz
- Bias Conditions: Vdd =48V, Idqc =51mA, Vg,dr = -3.08V, Vg,car = -2.95V, Vg,peak = -5V

Test Results

Case 1: Test Signal: LTE 1x100MHz (PAR = 8dB), Output Power: 38.8 dBm, Band B7:2600MHz

Post DPD results:

						Open Loop [Pre-DPD]				Closed Loop [Post-DPD]			
Freq: MHz	Pout [dBm]	DE [%]	Gain [dB]	VDD [V]	IDD [A]	ACP_Lo [dBc]	ACP_Hi [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]	ACP_LO [dBc]	ACP_HI [dBc]	ALT1_lo [dBc]	ALT1_hi [dBc]
2600	38.79	47.64	18.8	48	0.331	-22.95	-25.09	-24.47	-26.94	-49.62	-49.52	-50.66	-50.02

Conclusion

- The ADRV9029 on-chip, with DPD and CFR engines enabled, power consumption estimate is around 6.8 W in TDD mode. The power consumption can be reduced by lowering the sampling speed and saving JESD resources. Using the Zero IF architecture with an operating bandwidth of 200MHz, the ADRV2029 consumes lower power when compared to RFDAC transceiver architecture solutions.