Precision Technology Learning Module

FAQ: Digital-to-Analog Converters - Basic

– by Ian Vincent Andal & John Carlo Cillion

Introduction

The world we live in now is a world where anything can be controlled by computers. Self-driving cars, aircraft, and automated factories, just to name a few. And in these fields, the role played by precision converters is crucial. The more accurately we can collect and represent data, the more we can do with it and enhance our quality of life.

As discussed in the previous module, ADCs are involved in the acquisition and conversion of real-world analog data into digital form. Please refer to the ADC basic module and have a review of ADCs. DACs, on the other hand, is used in transforming the acquired, processed, transmitted, or stored data back to real-world variables for control, correction, information display, or further analog processing. It is the bridge that allows computer programs to interact with the real world with the use of different kinds of transducers.

A digital-to-analog converter, or DAC, is an electronic device that converts digital input data into analog output signal, as shown in Figure 1. This output signal can be in the form of either voltage or current, depending on the DAC core architecture used, it can be DC or AC, it can be a set of preprogrammed values or calculated steps, frequency, or angle for a sinusoidal output. DAC outputs can be so much more.

Figure 1. Digital-to-Analog Converter (DAC)

In this module series, different architectures, advantages, and disadvantages of DACs will be discussed. What applications do precision DACs fit into, and what key specifications are commonly required from precision DACs. What types of DACs are out there in the market and what are the design considerations for DACs on different applications? First, here's an overview of where DACs are commonly used.

Application

A typical signal chain for a Data Acquisition System, or DAQ, is shown in Figure 2. DACs are responsible for generating the analog signal that controls an output device based on the commands given by the system controller. This signal chain, although at its most basic form, creates the fundamental process of most of the current electronic systems. Aside from data converters, there are also analog and digital signal processing units built by amplifiers, RC, and digital filters, and switch multiplexers for multiple input/output; all playing important roles in the signal chain.

The production of precise voltage or current signals by precision DACs can be used in various types of applications. Listed below are some of them:

- Process and Motion Control (Motor Drivers, Piezoelectric Actuators)
- Bias Generation (LiDAR – Laser MZM drivers, Mems Mirrors)
- Gain and Offset Control (Feedback adjustment for Power Solution)
- Waveform Generation

Analog Devices' portfolio of products covers these applications, and it will be discussed in the upcoming modules in this series. For more information, visit the Precision DACs Hub in this link.

Precision D/A Converters (DAC) | Analog Devices

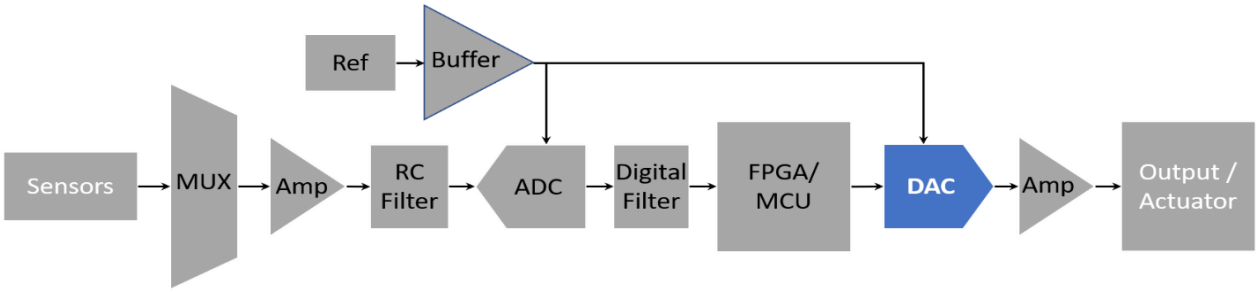
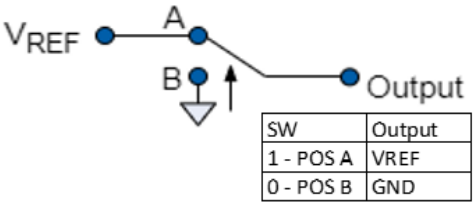


Figure 2. Basic Signal Chain for a DAQ

DAC Basic Operation

In the simplest sense, we can say that DACs are devices with digital code as input and analog voltage or current as its output. However, it must not be overlooked that the analog output is dependent on an analog input known as the **reference**, whose accuracy is almost always the limiting factor on the absolute accuracy of a DAC.



SW	Output
1 - POS A	VREF
0 - POS B	GND

Figure 3. 1-bit DAC

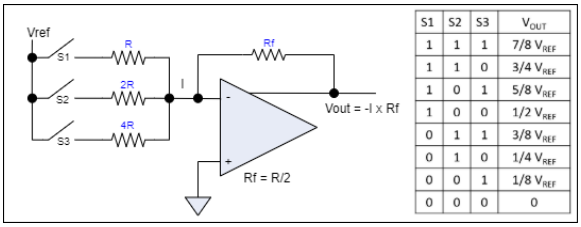
A simple single pole, double throw (SPDT) switch shown in Figure33, is counted as a 1bit DAC. The output switches between the VREF and ground or the positive and negative reference rails. Considering that the switch state reflects the 1bit input code, a truth table may be derived for a code zero input that gives a GND level output while a code one input gives VREF as the output. This has been the basis at which the more complex structures of a DAC operate.

Fundamental DAC Architectures

The topics below discuss the basic architectures used in DAC cores. It is important to learn the basics of each architecture and understand its advantages and disadvantages which is crucial during system design when choosing a suitable DAC core architecture for different applications.

Binary Weighted DAC

The binary-weighted resistor DAC shown in Figure 4 is usually the simplest textbook example of a DAC. An N-bit resolution, only needs N resistors with different values. Each branch consists of weighted current sources which may be simply resistors and a voltage reference, in the ratio of 1:2:4:8…2^{N-1}. The output then can be the sum of the enabled weighted current sources which can be converted to a voltage via the negative feedback amplifier setup.



S1	S2	S3	V_{OUT}
1	1	1	7/8 V_{REF}
1	1	0	3/4 V_{REF}
1	0	1	5/8 V_{REF}
1	0	0	1/2 V_{REF}
0	1	1	3/8 V_{REF}
0	1	0	1/4 V_{REF}
0	0	1	1/8 V_{REF}
0	0	0	0

Figure 4. Binary Weighted Network

The theory of operation is simple but the problems of manufacturing a high-resolution DAC with resistor ratios of even 1:128 for an 8-bit DAC is not as easy at seems, especially as these resistors must have matched temperature coefficients. Additionally, this DAC architecture is not inherently monotonic and achieving monotonicity would require stringent ratio and tolerance matching for all the resistors.

A DAC is said to be monotonic if it can be guaranteed that an increase in input code will result in an increase and never a decrease in the output. In a worst-case scenario, where the resistor errors are at max, the

current of the MSB (S1 branch, code 100) could be smaller than the rest of the combine branch currents (S2 & S3 branch, code 011). This might seem improbable from a 3-bit DAC but for a higher resolution 8-bit DAC, where the LSB value is around 1/256 V_{REF}.

String DAC

One of the earliest and simplest DAC architectures is the voltage output **Kelvin Divider, or String DAC** as shown Figure 5. 2^N equal value resistors in series and 2^N switches (typically CMOS) linked between each node of the resistor string and the output make up an N-bit string DAC. The output is taken from the selected node by closing **just one** of the switches at a time.

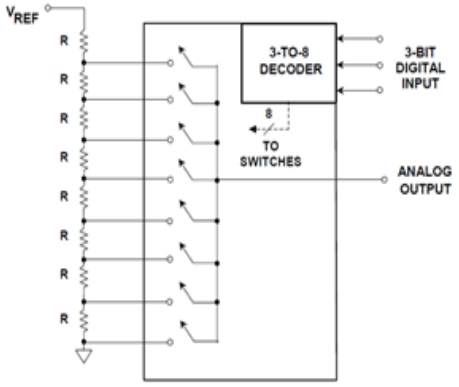


Figure 5. 3bit Voltage Output Kelvin Divider (String) DAC Circuit

Using the same value for all resistors guarantees that each step increase from a given input code, ideally, causes the analog output to also increase by a value equal to 1LSB, in this case, 1/8 V_{REF}. Refer to 1 for the output voltages for different input combinations.

The major drawback of this architecture is the number of resistors and switches required for higher resolution. For a 10bit DAC design, 2^{10} or 1024 switches and resistors will be needed when using the string architecture which makes it impractical in terms of cost and space.

Table 1. Truth table of 3bit Voltage Output Kelvin Divider (String) DAC Circuit

Input	Output
111	7/8 V_{REF}
110	6/8 V_{REF}
101	5/8 V_{REF}
100	4/8 V_{REF}
011	3/8 V_{REF}
010	2/8 V_{REF}
001	1/8 V_{REF}
000	GND

In a worst-case scenario where one resistor on the string is busted short, a code increase that will pass on that node will not increase the output value, but will also not decrease it, just leaving it the same as the previous value. This is the reason why the string DAC is said to be inherently monotonic.

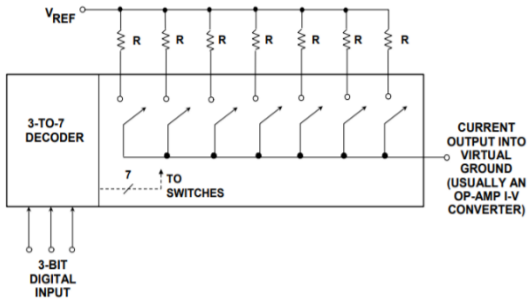


Figure 6. 3bit Current Output Thermometer (Fully-Decoded) DAC

Figure 6 shows a variation of the string DAC which allows for a current output instead of a voltage. This architecture is commonly referred to as "***thermometer***" or "**fully-decoded**" DAC and it contains 2^N-1 switchable current sources which refers to each branch consisting of a resistor and a switch. Another difference from the voltage output string DAC is that the switch decoder allows for multiple switches to be turned on as the digital code is increased, essentially adding each branch current to the total output. 2 shows the output current for different input combinations.

Table 2. Truth Table of 3bit Current Output Thermometer (Fully-Decoded) DAC

Input	Output
111	7/8 V_{REF} / R
110	6/8 V_{REF} / R
101	5/8 V_{REF} / R
100	4/8 V_{REF} / R
011	3/8 V_{REF} / R
010	2/8 V_{REF} / R
001	1/8 V_{REF} / R
000	GND

In comparison, the major drawback of the thermometer DAC and String DAC is numerous elements such as resistors and current sources that are needed to create an n-bit DAC. This drawback makes these architectures impractical to use for DACs that use greater than 8 input bits. Only until the recent introduction of very small IC feature sizes made it possible for these DAC architectures to become widely used for low and medium resolution DACs.

Segmented String DAC

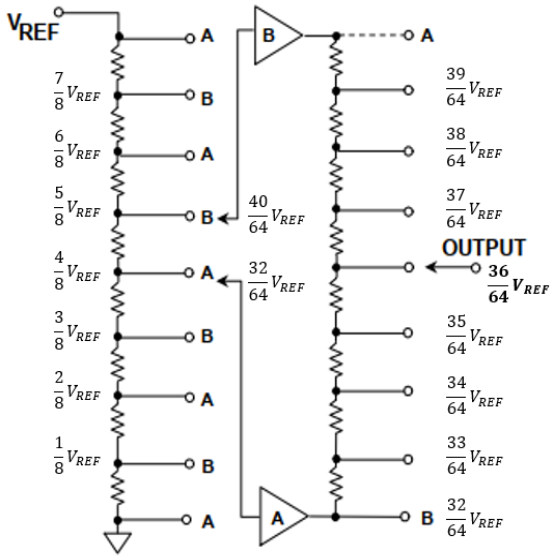


Figure 7. 6bit Segmented String Voltage DAC

In the previous module, it was established that one of the downsides of using a string DAC architecture is that it requires large number of resistors (2^N for an N-bit DAC). To obtain perfect DNL and INL, it is impractical to trim each resistor in the string DAC. The main reason for its impracticality is the cost and another reason is the number of resistors are too many and are too small to trim. In the process of segmentation, a single higher resolution DAC may be achieved by combining two or more DACs. In principle, one DAC handles the MSBs, which we will refer as the first stage with M-bits resolution, then another handles the LSBs, which we will refer to as the second stage with K-bits resolution, and their output are added in some way. The first stage has a string of 2^M equal resistor and a string of 2^N equal resistors in the second stage as shown in Figure 7.

The total number of bits can be given by the equation N = M + K bits. In this structure, the total number of equal value resistors for a 6bit DAC will be $2^3 + 2^3 = 16$, unlike for an ordinary string DAC, $2^6 = 64$. As seen in Figure 7, the segmented string DAC has buffers between the first and second stage. Due to the buffer, the second string does not load the first, and the resistors for the strings do not need to be of the same value. However, all the resistors in each string, need to be equal, or else the DAC will be nonlinear.

Decoding of the first segment is made complex so that buffers A & B can only be connected to their similarly labeled taps. Doing this solves the possibility of the buffers' offset causing non-monotonicity. Of course, the second segment decoding must change direction when one buffer "leapfrogs" the other and the taps "A" and "B" are alternately not used. The logic complexity is trivial since it is justified by the increase in performance. Table 3 shows the truth table of 6-bit segmented string Voltage DAC.

Table 3. Truth Table of 6bit Segmented String Voltage DAC

Input	Output
11111	63/64 V_{REF}
11110	62/64 V_{REF}
11101	61/64 V_{REF}
…	…
00010	2/64 V_{REF}
00001	1/64 V_{REF}
00000	GND

R-2R DACs

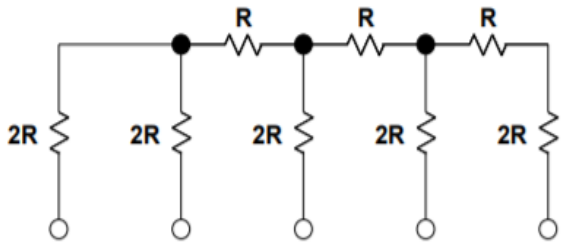


Figure 8. 4 Bit R-2R Ladder Network

Another commonly used DAC building-block structure is the R-2R resistor ladder network shown in Figure 8. This architecture uses a 2:1 value for the resistors. To create an N-bit DAC, the number only of resistors needed is 2*N. This is a significant reduction in the number of resistors for higher resolutions compared to the string DAC. The R-2R ladder network is inherently non-monotonic although trimming and matching the resistor is a required utmost consideration. The R-2R architecture may be used as a DAC in two ways namely: voltage mode and current mode.

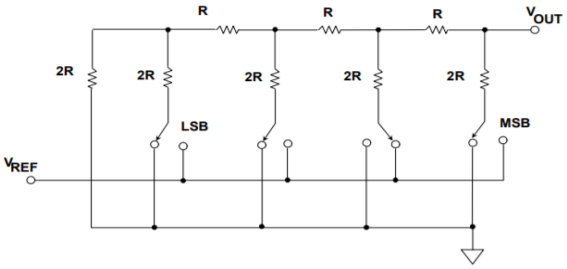


Figure 9. Voltage-mode R-2R Ladder Network DAC

Let us discuss the first way of implementing the R-2R ladder network as a DAC, the voltage mode R-2R ladder network DAC as shown in Figure 9. In this mode, the arms of the ladder or also called "rungs" may either be switched to the ground or VREF. Also, in this mode, the output is taken from the end of the ladder. The output taken is a voltage, however, the impedance and code are independent of one another. As a result, it could be taken as a current output into a virtual ground.

The constant output impedance eases the stabilization of any amplifier connected to the output node. Additionally, the switches switch the arms of the ladder between low impedance nodes VREF and ground, so capacitive glitch currents tend not to flow in the output. The reference input impedance varies widely with code, so the reference input must be driven from a low impedance source.

The V_{REF} and V_{OUT} positions from the voltage mode are interchanged in the current-mode R-2R ladder DAC shown in Figure 10. While the ends of the arms are switched between an output line that must be held at ground potential and the ground, the gain of the DAC can be adjusted using a series resistor at the VREF terminal with its code-independent impedance. With the outputs basically always ground connected, the current at each arm is maintained at either switch state reducing the glitch due to switching states.

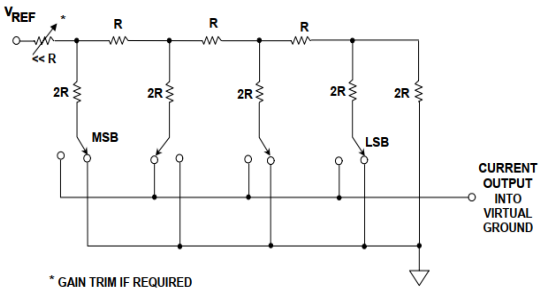


Figure 10. Current-mode R-2R Ladder Network DAC

A current-mode ladder network output is normally connected to an op amp set as a current-to-voltage (I-V) converter. However, the DAC output impedance change with digital coding complicates stability of this op amp. One drawbacks of this architecture to function is its requirement for more external components, op-amp and a resistor network

Current-steering DAC (CMOS Switch current DAC)

High-speed DACs use submicron CMOS technologies as its process for its devices. Switching speeds of submicron MOS transistors have allowed faster sampling rates in hundreds of mega-samples-per-second (MSPS) up to the giga-samples-per-second (GSPS) range.

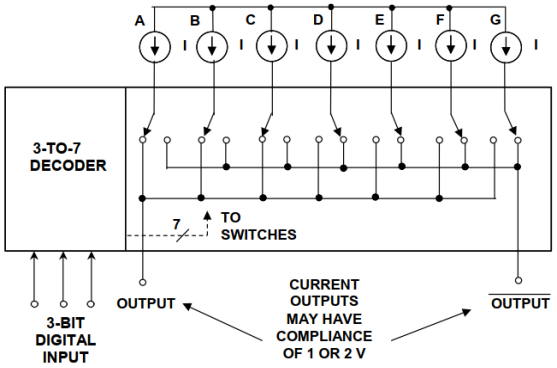


Figure 11. Basic High Speed Current Steering DAC

Having low distortion and glitch at high frequencies if extremely important for high-speed DACs. Thus, they are often built with arrays of fully decoded current sources. Shown in Figure 11 is an example. Current sources are never turned on and off – they are steered to one place or another, depending on the input code. Current steering shortens the time for capacitive loading, and removes significant inductive spikes caused by turning current sources on-off at high speed.

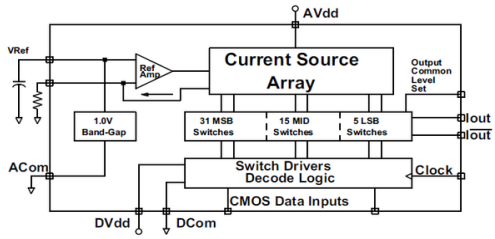


Figure 12. Block Diagram of Typical High-speed CMOS DAC

Current steering DACs with resolution from 8 to 16bits are composed of two or more segments. The MSB segment, which is always made from unit-weighted elements and is thermometer coded, varies from as few as 4 bits up to maximum of 8 bits. The rest of the bits may be binary coded but are segmented further into another segments, the intermediate significant bit (ISB) and the LSB section.

Depicted in Figure 12 below is a basic block diagram of a typical high-speed CMOS DAC. This DAC provides 14 bits of resolution. Five MSBs are composed of 31-unit weighted elements. The remaining 9 bits are split into 4 ISBs and 5 LSBs.

Table 4 shows the summary of different basic DAC architectures and its characteristics.

Terminologies and Key Specifications

This section discusses the different terminologies and key specifications used in DACs.

Offset Error and Gain Error

The output of a DAC may be expressed by the equation A = G*D + K. Where A is the analog output, D is the digital input code, G is the gain error and K is the offset error. The offset error is measured at zero-scale. To get the gain error, we can use the equation knowing that we already have the analog output, digital input code and offset error.

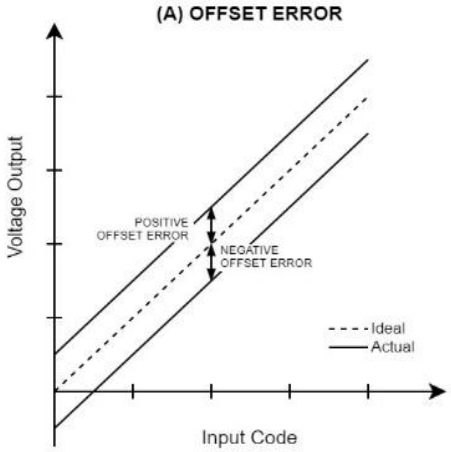


Figure 12. Offset Error

Table 4. Summary of Basic DAC Architectures' Characteristics

DAC Types	# of resistors	Monotonicity	Input Impedance	Output Impedance	Disadvantage	Advantage
String DAC (Kelvin Divider)	2^n	Inherent	Not code dependent	Code dependent	Too many resistors, Noisy	Lower cost
Segmented String DAC	$2^{n/2}+2^{n/2}$	Inherent	Not code dependent	Code dependent	Noisy	Less resistors than Kelvin Divider
Binary weighted DAC	n	Not inherent		Code dependent	Harder to manufacture	Less resistors than segmented string DAC
R-2R	2n	Not inherent	Depends on Operation	Depends on Operation	More expensive, Need extra components	Easier to manufacture, High Accuracy, low noise, highest precision, faster
Current Steering	2^n-1	Inherent	Not Code Dependent	Code Dependent	High element count, output should be at or close to ground, compliance voltage at the output	Less distortion and glitch due to current steering, fast settling time

Offset Error, shown in Figure 12, is a measure of the difference between the actual and ideal output voltage V_{OUT} in the linear region of the transfer function, it is typically expressed in mV or mA. Offset error may either be negative or positive.

Gain Error, on the other hand, is a measure for the DAC's span error. It is the difference between the actual and ideal slope of the DAC transfer characteristic. Gain error is commonly expressed as a percentage of the full-scale range of the instrument (percent FSR). Shown in Figure 13 is the Gain Error while Figure 14 shows the effects of offset and gain error together in actual.

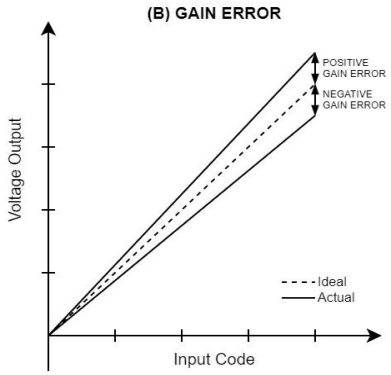


Figure 13. Gain Error

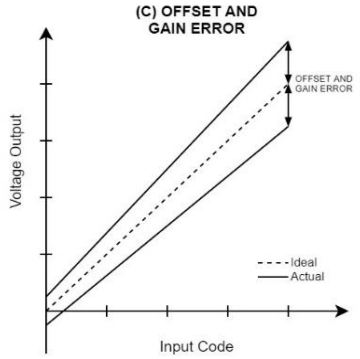


Figure 14. Transfer Function for Ideal 3-bit DAC

Differential Nonlinearity (DNL)

Differential Nonlinearity is the difference between the ideal 1LSB output change and the measured change between two adjacent codes as shown in Figure 15. A specified DNL of ± 1LSB maximum ensures monotonicity.

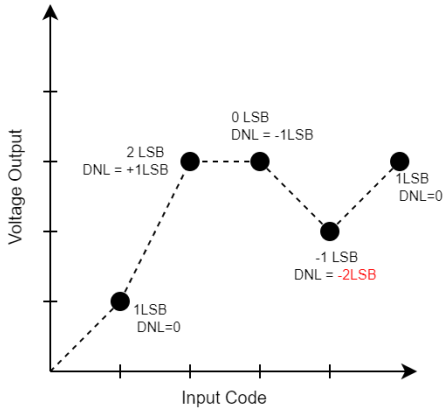


Figure 15. Sample DNL vs Code plot

To give a better visualization of DNL, Figure 16 shows the actual step size and the ideal 1 LSB output. The x-axis is the bits while the y-axis is the digital output in terms of voltage.

Integral Nonlinearity (INL)

Integral non-linearity or Relative Accuracy is a measurement of the maximum deviation, in LSBs, from

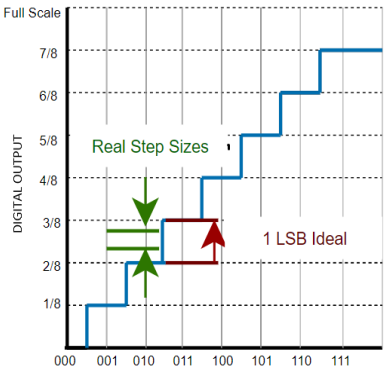


Figure 16. Ideal Step Size vs Real Step Size

the ideal straight line passing through the endpoints of the DAC Transfer function, as shown in Figure 17. INL could also be represented as the cumulative sum of the DNL.

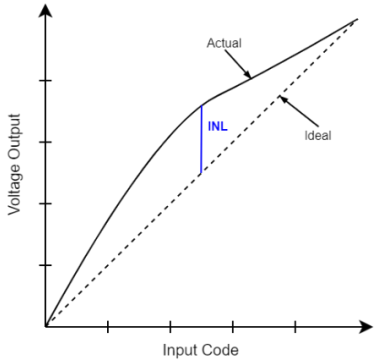


Figure 17. INL or Relative Accuracy

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the amount of noise or impulse injected into the DAC's output when a change is introduced in the DAC register state by a written input code. Measuring glitch as energy is suitable for slow DACs where the output filter spreads the energy over time. The glitch area is expressed in nV•s. Digital-to-analog glitch impulse as shown in Figure 18 is usually measured in major code transitions

since this is where the worst-case impulse is expected due to max. number of internal switches changing state i.e., 0b0111 to 0b1000.

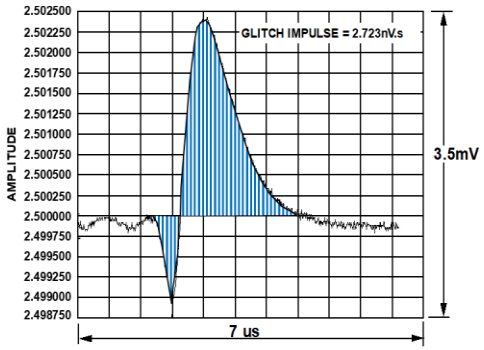


*Figure 18. Glitch Impulse from **AD5680***

Output Voltage Settling Time

The **output voltage settling time** shown in Figure 19 is the amount of time it takes for the DAC output to settle to a specified value normally expressed in terms of us or ns. For accurate output signal representation, the DAC output must settle before another input code triggers an output change. For precision converters, the output is typically expected to settle to values within ±2LSB, ±1LSB or ±0.5LSB.

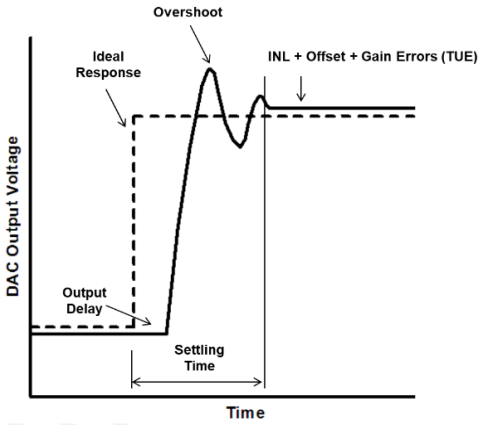


Figure 19. Output Voltage Settling Time

Slew Rate

Slew rate is the rate of how fast the output voltage changes. It is measured in the linear region of the output at the ¼ to ¾ scale step. Typically expressed in V/µS. Figure 20 shows the slew rate.

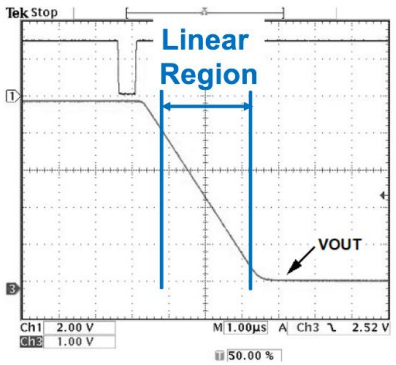


Figure 20. Slew Rate

DAC Noise

In precision DACs datasheet, noise may be specified as Output Voltage Noise and Output Noise Spectral Density.

Output Voltage Noise

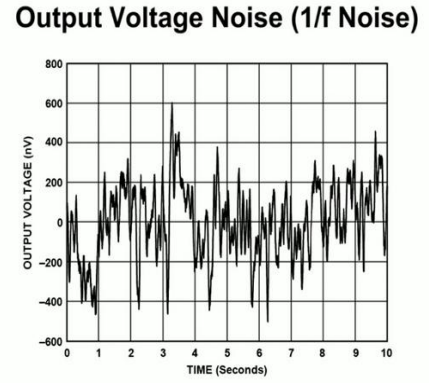


*Figure 21. 1/f Noise from **AD5780***

Output Voltage Noise also known as 1/f noise is captured in time domain. It refers to the voltage peak-to-peak noise that is typically measured between the frequency bandwidth 0.1 Hz – 10 Hz. This noise occurs due to the nature of the component and impurities of

the process what was used. Moreover, there is no general equation to define this type of noise. Figure 21 shows the 1/f noise.

Output Noise Spectral Density

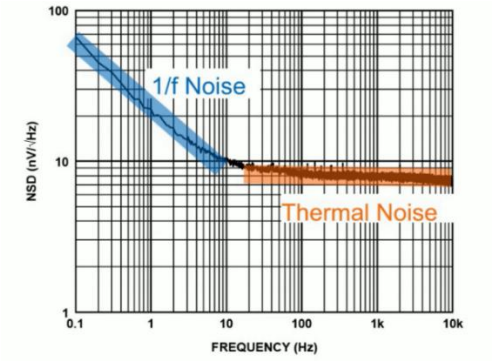


*Figure 22. Output NSD from **AD5780***

Output Noise Spectral Density is the noise energy with respect to frequency. It is typically measured at 1 kHz and 10 kHz or depending on the 1/f corner frequency. It composed of 1/f noise and thermal noise. Thermal noise is produced by thermal electron agitation and proportional to the resistance. Figure 22 shows the 1/f noise and thermal noise in the output noise spectral density diagram

Signal-to-Noise Ratio (SNR)

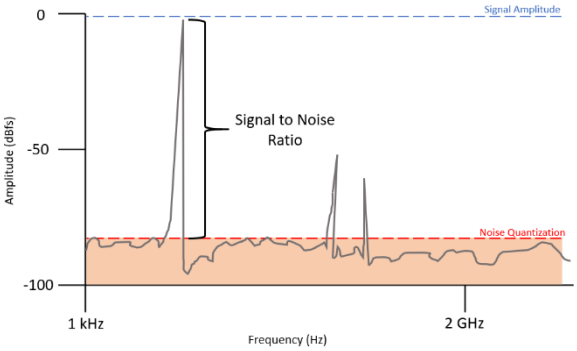


Figure 23. Signal-to-Noise Ratio

SNR is the ratio of the rms signal to the rms noise for sine-wave output signals, excluding the 2nd through 10th harmonics. It is measured in decibels (dB). The measurement is specified for a selected signal amplitude and frequency. The signal amplitude covers the full-scale output range of the DAC and is typically measured up to 20kHz for precision applications. Figure 23 shows the signal-to-noise ratio.

$$SNR = 20log_{10}\left(\frac{rms\ signal}{rms\ noise}\right)$$

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the rms signal power to the rms noise plus distortion for sine-wave output signal of the DAC. SINAD as shown in Figure 24 is the same as SNR, with the addition of harmonic distortion. The measurement is specified for a selected signal amplitude and frequency.

$$SINAD = 20log_{10}\left(\frac{rms\ signal}{rms\ noise\ and\ distortion}\right)$$

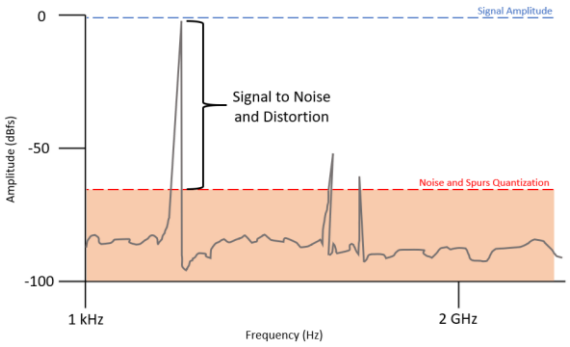


Figure 24. Signal-to-Noise and Distortion

Spurious-free Dynamic Range (SFDR)

SFDR, shown in Figure 25, is the ratio of the rms value of the output signal to the rms value of the highest non-fundamental component of the signal. Same with SNR and SINAR, the amplitude and frequency is specified.

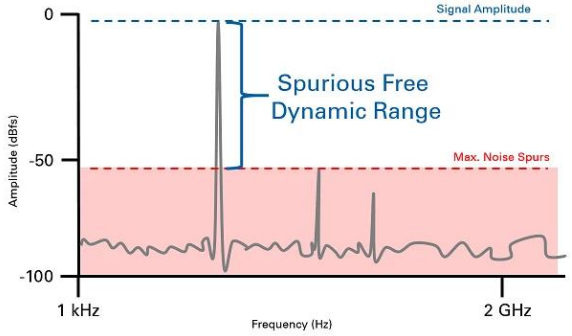


Figure 25. Spurious-free Dynamic Range

Digital Feedthrough

Digital feedthrough is a measure glitch coupled into the output of the DAC by updating the digital inputs. It is measured by sending a digital command to the DAC without update the DAC output itself. The spec is given as nV-sec and is measured with a zero-scale to full-scale code change. Shown in Figure 26 is the digital feedthrough taken from **AD5172/AD5173**.

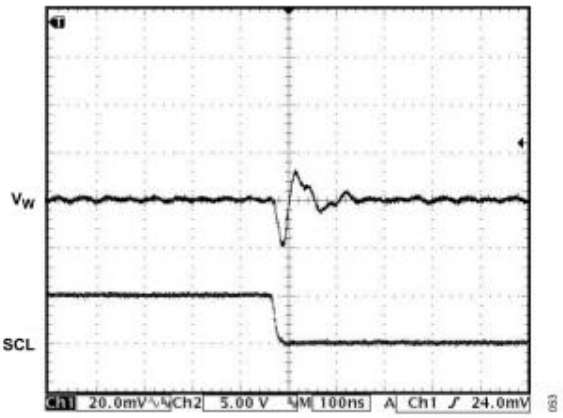


*Figure 26. Digital Feedthrough of **AD5172/AD5173***

Total Harmonic Distortion (THD)

THD is the ratio of the rms DAC output signal to the rms value of the harmonics. Only the 2nd to 5th harmonics are included. Shown in Figure 27 is the THD of **AD5676** measured at 1 kHz.

$$THD = 20log\left(\frac{S}{D}\right)$$

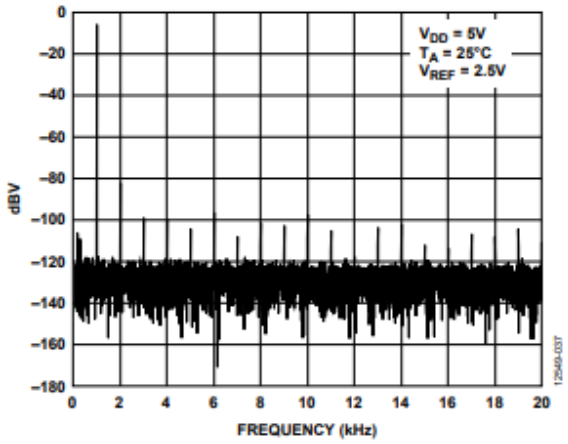


*Figure 27. **AD5676** THD at 1kHz*

DC Power Supply Rejection Ratio (PSRR)

DC PSRR is a measure of the ability of the DAC outputs to reject DC variations in applied in the power supplies of the DAC. It is characterized for a given dc change in power supply voltage and is expressed in μV/V.

AC Power Supply Rejection Ratio (PSRR)

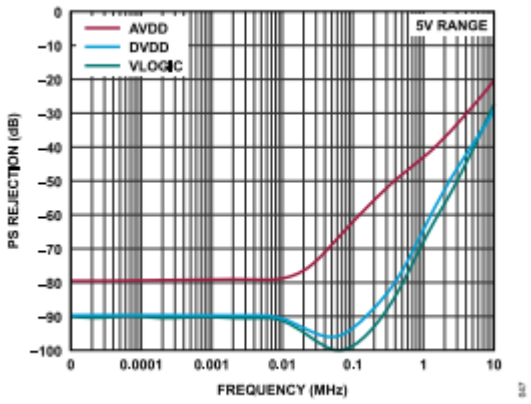


*Figure 28. AC PSRR of **AD3551R***

AC PSRR, on the other hand, is the ability of the DAC outputs to reject AC noise in the DAC's power supplies. It is characterized for a set amplitude and frequency change in power supply and is expressed in decibels. Figure 28 shows the measured AC PSRR of **AD3551R**.

Reference Feedthrough

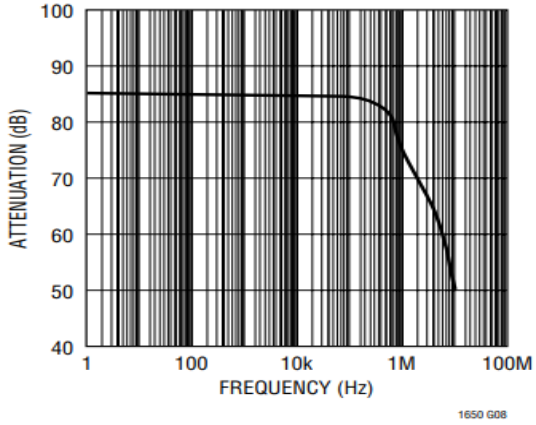


Figure 29. Reference Feedthrough

Reference feedthrough is the measure of feedthrough from the V_{REF} input to the DAC output. It is the ratio of the signal amplitude at the DAC output to the DAC output when the DAC output is not being updated. It is usually expressed in dB as shown in Figure 29.

DC Crosstalk

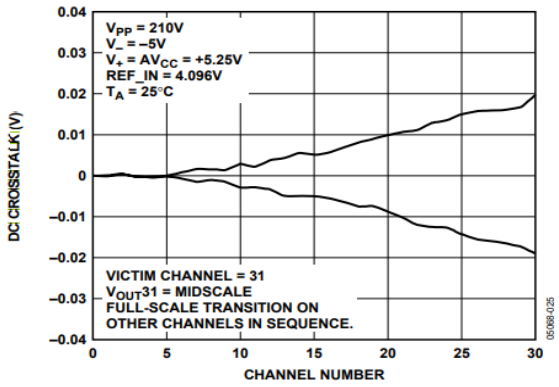


Figure 30. DC Crosstalk

DC crosstalk is the dc change in the output level of a DAC when a change in the output of another DAC occurs. To measure the DC crosstalk of a DAC, the DAC being tested must be kept at mid-scale while the output of the other DAC changes in full-scale. DC crosstalk is expressed in µV. It is also common to express it in uV/V if the DAC has several ranges. Figure 30 shows the Cumulative DC Crosstalk Effects on a Single-Channel Output, switching ll Other Channels in Sequence

Digital Crosstalk

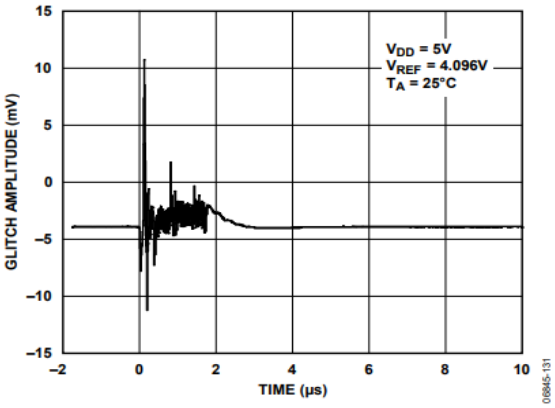


*Figure 31. Digital Crosstalk of **AD5066***

Digital crosstalk shown in Figure 31 is the signal coupled to the output of a DAC due to changing digital input from an adjacent DAC that is being updated.

Analog Crosstalk

When a DAC's output changes it causes a glitch impulse known as analog crosstalk which is transferred to another DAC. It is expressed in nV-sec and measured by loading one of the input registers to a full-scale code change. The output of the DAC whose digital code was not changed is monitored through a software LDAC. Shown in Figure 32 is the analog crosstalk.

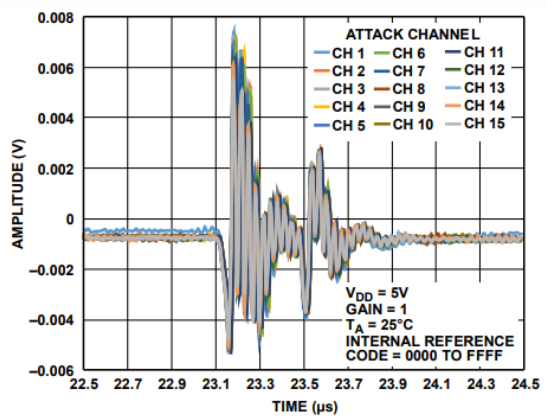


Figure 32. Analog Crosstalk of ***AD5674/AD5674R/AD5679/AD5679R***

DAC-to-DAC Crosstalk

Changes in digital code and subsequent analog output change from a DAC, results to a glitch impulse that is transferred to the output of another DAC. DAC-to-DAC glitch energy is usually expressed in nV•s and it is measured by loading all 0s to all 1s and vice versa, using the write to and update commands when monitoring the output of the affected DAC channel with a full-scale code change. Figure 33 shows the DAC-to-DAC crosstalk.

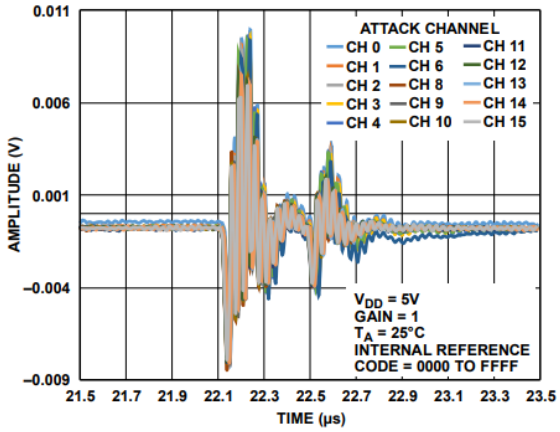


Figure 33. DAC-to DAC Crosstalk of
AD5674/AD5674R/AD5679/AD5679R

Multiplying Bandwidth

Multiplying bandwidth as shown in Figure 34 is actually the transfer function from VREF to VOUT. It is a measurement of the bandwidth of the complete DAC, not just the amplifier.

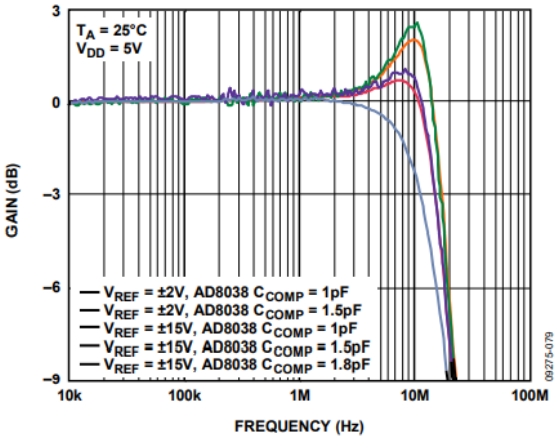


Figure 34. Multiplying Bandwidth of ***AD5544*** *and* ***AD5554***

Voltage Reference TC

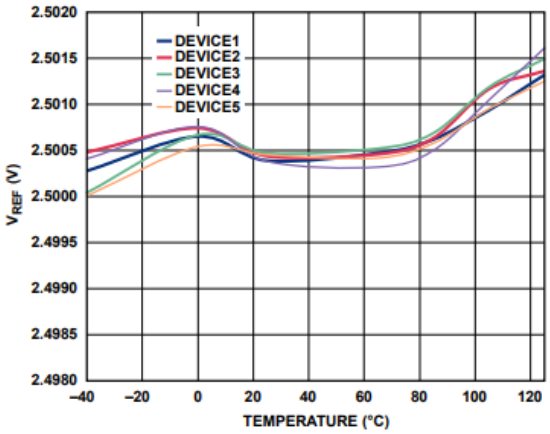


Figure 35. V_{REF} vs. Temperature of ***AD5674/AD5674R/AD5679/AD5679R***

Voltage reference TC is the maximum change in reference output voltage for a given temperature range and it usually expressed in ppm/°C. The equation below shows how to calculate the voltage reference TC.

Shown in Figure 35 is a graph of the reference voltage vs. temperature.

$$TC = \frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temperature\ Range} \times 10^6$$

where:

$V_{REF(MAX)}$ is the maximum reference output measured over the total temperature range.

$V_{REF(MAX)}$ is the minimum reference output measured over the total temperature range.

$V_{REF(NOM)}$ is the nominal reference output voltage, 2.5 V. Temperature Range is the specified temperature range of −40°C to +125°C

Terminologies

Resolution – DAC resolution represents the analog output at number of discrete levels or steps. The smallest resolvable signal is 1 Least Significant Bit (LSB) which is the smallest possible step of the output with a change of 1bit in the input code. The key specification related to resolution is DNL.

Accuracy – refers to how close the output of the DAC is to the ideal value given a digital code input. The key specification for accuracy is the INL.

Monotonicity – a DAC is said to be monotonic if its output increases or remains the same for an increment in the digital code. Conversely, a DAC is non monotonic if the output decreases for an increment in digital code.

Noise – In precision DACs, noise is any signal superimposed to an ideal DC output.

RMS – root mean square, arithmetic average of the squares of a set of numbers.

Decibel (dB) – unit of measurement for intensity or power level of an electric signal on a logarithmic scale.

Harmonics – frequencies that are integer multiples of the fundamental frequency.

Self - Check Questions

Q: It was said that for a DAC to be monotonic, the DNL should be > -1 LSB. Can we also guarantee monotonic behavior when INL > -1 LSB?

Q: I have a 14-bit DAC, B Grade +/-4 LSB INL and an output requirement of 14-bit accurate voltage signal. Can I use this DAC to meet the output requirement? Determine the number of bits with accurate output.

Q: What is the maximum update rate, or time from the signal entry to signal output of the AD5676R? Ignore interface speed.

Q: I need a DAC with low noise, high accuracy and precision. Which DAC Architecture fits my needs?

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Revision History

05/19/2022—Rev 0 Release