ANALOG DEVICES

FAQ

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Migrating to the AD7606C-18 from the AD7608 and AD7609

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INTRODUCTION

The AD7606C-18 is an enhanced version of both the AD7608 and AD7609 analog-to-digital, data acquisition systems (DAS). The AD7606C-18 is a pin for pin replacement for either the AD7608 or the AD7609 with no hardware modifications required to the existing designs, with the following improved features:

- Faster throughput rate of up to 1000 kSPS.
- Extended operating temperature range up to 125°C.
- Lower digital supply (V_{DRIVE}) range down to 1.71 V.
- Higher clamp voltage up to ±21 V.

This document describes the differences between the hardware mode of the AD7606C-18 and the AD7608/AD7609.

For full details on the AD7606C-18, the AD7608 and the AD7609, see the corresponding data sheet, which should be consulted in conjunction with this document.

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HARDWARE COMPATIBILITY

The AD7606C-18 is a pin for pin replacement for both the AD7608 and the AD7609, with no hardware modifications required on existing designs. The functionality of some of the pins have changed to enable the software mode capability on the AD7606C-18. The pin functionality differences are detailed in Table 1.

Table 1. Pin Mnemonic Differences Between the AD7608/AD7609 and the AD7606C-18

Pin No.	AD7608/9 Mnemonic	AD7606C Mnemonic
3	OS 0	OS0[1]
4	OS 1	OS1[1]
5	OS 2	OS2[1]
10	CONVST B	$\overline{WR}$[2]
19	DB3	DB3/$D_{OUT}E$[2]
20	DB4	DB4/$D_{OUT}F$[2]
21	DB5	DB5/$D_{OUT}G$[2]
22	DB6	DB6/$D_{OUT}H$[2]
27	DB9	DB9/$D_{OUT}C$[2]
28	DB10	DB10/$D_{OUT}D$[2]
29	DB11	DB11/SDI[2]

[1] Pulling the OS0, OS1, and OS2 pins high sets the AD7606C to software mode. This combination is invalid on the AD7608/AD7609.
[2] Only applicable when using software mode.

PIN 10 AND PIN 9 DIFFERENCES

Pin 10 (CONVST B) in the AD7608/AD7609 is the CONVSTB input that initiates conversions on Channel 5 to Channel 8, and Pin 9 (CONVST A) in the AD7608/AD7609 is the CONVST A input that initiates conversions on Channel 1 to Channel 4. In the AD7606C-18, Pin 9 (CONVST) is the CONVST input for all eight channels. In the AD7606C-18, Pin 10 ($\overline{WR}$) is the write input for writing registers to software parallel mode. When not using software parallel mode for the AD7606C-18, tie $\overline{WR}$ high, low, or to the CONVST pin.

PIN 19 TO 22 AND PIN 27 TO 29 DIFFERENCES

In the AD7608/AD7609, Pin 19 (DB3), Pin 20 (DB4), Pin 21 (DB5), Pin 22 (DB6), Pin 27 (DB9), Pin 28 (DB10), and Pin 29 (DB11) are parallel data output lines. When using hardware mode for the AD7606C-18, these pins are also the parallel data output lines.

When using software mode for the AD7606C-18, the serial interface can be configured to have four or eight output data lines. Therefore, up to six extra serial data outputs, $D_{OUT}C$ to $D_{OUT}H$, can be enabled on Pin 19 to 22, Pin 27 and Pin 28 of the AD7606C-18.

In software mode, Pin 29 of the AD7606C-18 is the serial data input (SDI) used to write registers in the memory map. See Table 3 for the pin functionality for each device and operating mode.

POWER SUPPLIES

The analog power supply voltage range (AV_{CC}) in the AD7606C-18 is the same as the AD7608/AD7609 (4.75 V to 5.25 V). The logic supply voltage range (V_{DRIVE}) in the AD7608/AD7609 is 2.3 V to 5.25 V, whereas the logic supply voltage range in the AD7606C-18 is 1.71 V to 3.6 V.

The REGCAP pins (Pin 36 and Pin 39) are outputs from the analog and digital low dropout (LDO) regulators, which is in the range of 2.5 V to 2.7 V for the AD7608/AD7609 and in the range of 1.875 V to 1.93 V for the AD7606C-18.

Table 2. Power Supplies for the AD7608/AD7609 and the AD7606C-18

Device	AV_{CC}	V_{DRIVE}
AD7608/AD7609	4.75 V to 5.25 V	2.3 V to 5.25 V
AD7606C-18	4.75 V to 5.25 V	1.71 V to 3.6 V

Table 3. Pin 27 to Pin 29 Pin Function for the AD7608/AD7609 and the AD7606C-18

Data Interface	Device	Mode	Pin 19	Pin 20	Pin 21	Pin 22	Pin 27	Pin 28	Pin 29
Parallel	AD7608/AD7609	Not applicable	DB3	DB4	DB5	DB6	DB9	DB10	DB11
	AD7606C-18	Hardware or software	DB3	DB4	DB5	DB6	DB9	DB10	DB11
Serial	AD7608/AD7609	Not applicable	Unused[1]	Unused[1]	Unused[1]	Unused[1]	Unused[1]	Unused[1]	Unused[1]
	AD7606C-18	Hardware	Unused[1]	Unused[1]	Unused[1]	Unused[1]	Unused[1]	Unused[1]	Unused[1]
	AD7606C-18	Software	$D_{OUT}E$[2]	$D_{OUT}F$[2]	$D_{OUT}G$[2]	$D_{OUT}H$[2]	$D_{OUT}C$[2]	$D_{OUT}D$[2]	SDI

[1] Tie unused pins to AGND.
[2] If serial data output is selected to have four lines through the memory map.

RESET

The AD7608/AD7609 has a single reset mode that resets the entire device by a applying a short pulse (50 ns minimum pulse width) in the RESET pin.

The AD7606C-18 has a dual reset mode (full reset and partial reset) as described in Table 4. There is a minimum delay, called t_{DEVICE_SETUP} in the data sheet, after a reset that must elapse before starting the first conversion.

After issuing a partial reset in AD7606C-18, that is when 50 ns ≤ t_{RESET} < 2 µs, t_{DEVICE_SETUP} (t_7) is 25 ns as per AD7606.

After issuing a full reset, that is when t_{RESET} > 3 µs, t_{DEVICE_SETUP} is 253 µs in AD7606C-18. Take this longer t_{DEVICE_SETUP} into account for software back compatibility when t_{RESET} is longer than 3 µs on existing designs.

REFERENCE BUFFER OUTPUT

The AD7606C-18 reference buffer output is typically 4.4 V and is available on Pin 44 (REFCAPA) and Pin 45 (REFCAPB), whereas in the AD7608/AD7609, the reference buffer output is 4.5 V on these same pins.

Table 4. Reset Line Functionality Differences Between the AD7608/AD7609 and the AD7606C-18

t_{RESET} Pulse Width	AD7608/AD7609	AD7606C-18
<50 ns	No effect	No effect
50 ns ≤ t_{RESET} < 2 µs	Power-on reset, resets entire device[2]	Resets ADC state machine and data interface[1]
≥3 µs	Power-on reset, resets entire device[2]	Power-on reset, resets entire device[2]

[1] 50 ns must elapse before initiating next conversion.
[2] 253 µs must elapse before initiating next conversion.

PERFORMANCE IMPROVEMENTS

Directly replacing the AD7608/AD7609 with the AD7606C-18 results in straight forward benefits due to its higher throughput rate and wider temperature range. However, switching to software mode delivers the best system level benefits, see the

THROUGHPUT RATE

The AD7606C-18 can sample as fast as 1000 kSPS, whereas the maximum throughput rate for the AD7608/AD7609 is 200 kSPS.

TEMPERATURE RANGE

The operating temperature range for the AD7608/AD7609 is −40°C to +85°C, whereas the operating temperature range for the AD7606C-18 is extended from −40°C to +125°C. All specifications stand across the whole temperature range, unless otherwise noted on the AD7608/AD7609 or the AD7606C-18 data sheet.

SOFTWARE MODE

When the software mode of the AD7606C-18 is enabled (see the Migrating to the AD7606C-18 Using Software Mode section) rather than the legacy hardware mode, the following advanced features are available:

- Independent, per channel basis range selection, including both differential and single ended range options.
- System gain, phase, and offset on-chip compensation.
- Analog Input Open circuit detection.
- Additional oversampling ratios (OSR): 128 and 256.
- Optional 1, 2, 4 or 8 serial data output configurations.
- Diagnostics.

These features are only available within the software mode of the AD7606C-18, which can be configured by writing to the register map.

Table 5. Summary of the Differences Between the AD7608/AD7609 and the AD7606C-18

		AD7606C-18	
Parameter	**AD7608/AD7609**	**Hardware Mode**	**Software Mode**
Maximum Throughput Rate	200 kSPS	1000 kSPS	1000 kSPS
Temperature Range	−40°C to +85°C	−40°C to +125°C	−40°C to +125°C
V_{DRIVE} Range	2.3 V to 5.25 V	1.71 V to 3.6 V	1.71 V to 3.6 V
Absolute Maximum Input Voltage	±16.5 V	±21 V	±21 V
Analog Input Range	±10 V or ±5 V[1]	±10 V or ±5 V[1]	See Table 6
System Gain, Phase, and Offset On-Chip Compensation	Not applicable	Not accessible	Available**Error! Bookmark not defined.**
Oversampling Ratio (OS)	From no OS to OSR = 64	From no OS to OSR = 64	From no OS to OSR = 256
Analog Input Open Circuit Detection	Not applicable	Not accessible	Available**Error! Bookmark not defined.**
Serial Data Output Lines	2	2	Selectable: 1, 2, 4 or 8
Diagnostics	Not applicable	Not accessible	Available

[1] Not on a per channel basis.

Table 6. Analog Input Ranges available in AD7606C-18's software mode

Analog Input Type	Unipolar/Bipolar Input	Analog Input Range
Single Ended	Bipolar	±12.5V, ±10V, ±6.25V, ±5V and ±2.5V
Single Ended	Unipolar	0-12.5V, 0-10V and 0-12.5V
Differential	Bipolar	±20V, ±12.5V, ±10 V and ±5V

MIGRATING TO THE NEW GENERATION AD7606C-18

Migrating from the AD7608/AD7609 to the AD7606C-18 offers multiple advantages. All features available in the AD7608/AD7609 are also available in the AD7606C-18. There is no need to change the layout or evaluation setup when migrating to the new generation of the product (AD7606C-18), as long as the digital supply is below 3.3 V.

MIGRATING TO THE AD7606C-18 USING HARDWARE MODE

Using the Parallel Interface

To migrate to the AD7606C-18 in hardware mode using the parallel interface, ensure that the following are done:

- Avoid tying the OS2, OS1, and OS0 pins high because the AD7606C-18 enters software mode if this is done (as shown in Table 7). Note that this combination of the OS x pins is also invalid on the AD7608/AD7609.
- Tie the PAR/SER SEL pin to AGND to select the parallel interface.
- After power-up, 253 µs (t_{DEVICE_SETUP}) must elapse before initiating the first conversion. See Reset section for details on initiating subsequent resets.

Using Serial Interface

To migrate to the AD7606C-18 in hardware mode using the serial interface, ensure that the following are done:

- Avoid tying OS2, OS1, and OS0 high simultaneously because the AD7606C-18 enters software mode if this is done (as shown in Table 7). Note that the combination of the OS x pins is also invalid on the AD7608/AD7609.
- Tie the PAR/SER SEL pin to V_{DRIVE} to select the serial interface.
- Tie unused DBx pins to AGND.
- After power-up, 253 µs (t_{DEVICE_SETUP}) must elapse before initiating the first conversion. See Reset section for details on initiating subsequent resets.

Note that the OSx pins are latched on the falling edge of RESET.

Table 7. Oversample Bit Decoding

OS 2 to OS 0	AD7608/AD7609	AD7606C-18
000	No OS x	No OSx
001	2	2
010	4	4
011	8	8
100	16	16
101	32	32
110	64	64
111	Invalid	Enters software mode

MIGRATING TO THE AD7606C-18 USING SOFTWARE MODE

To migrate to the AD7606C-18 and take advantage of the advanced features only available in software mode, ensure that the following are done:

- Tie all of the OS x pins high to access software mode. The oversampling ratio is set through the corresponding register instead of through the pins.
- To access the AD7606C-18 memory map using the serial interface, use Pin 29 (DB11/SDI) as the serial data input of the SPI interface. If Pin 29 is tied to AGND as recommended in the AD7608/AD7609, no memory map write or read operation can be performed.
- To access the AD7606C-18 memory map using the parallel interface, use Pin 10 (WR) for write operations. In the AD7608/AD7609, Pin 10 (CONVST B) initiates conversions on Channel 5 to Channel 8. Tying Pin 10 of the AD7608/AD7609 to CONVST A results in all eight channels sampling simultaneously. In the AD7606C-18, the WR pin must be available for the memory map to be accessed. If Pin 10 (WR) of the AD7606C-18 is tied to Pin 9 (CONVST), a memory map write or read operation cannot be performed.

SOFTWARE COMPATIBILITY

The microcontroller code and its protocol, developed for the AD7608/AD7609products work with the AD7606C-18 without requiring any modifications to be made as long as the device is used in hardware mode and the timing differences stated in the Reset section are respected. To take advantage of the features available in software mode, adapt the code to add writing capabilities to access the memory map in either the serial interface or the parallel interface (see the Migrating to the AD7606C-18 Using Hardware Mode section and the Migrating to the AD7606C-18 Using Software Mode section for additional information).

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