Precision Technology Learning Modules
Switches and Multiplexers - Advanced

– by Mar Christian Lacida

Introduction

Harsh environments in the automotive, military, and avionic applications drive the integrated circuit to their performance limits, forcing them to withstand high voltage and current, temperature, humidity, vibration, radiation, and other stresses. System engineers are developing high-performance electronics to provide suitable features in different applications such as safety, entertainment, telematics, control, and human-machine interfaces.

In addition, manufacturers specify absolute maximum ratings for every integrated circuit; these ratings must be observed to maintain reliable operation and meet published specifications. If the maximum ratings are exceeded, the operational performance is not guaranteed to result in device damage or failure.

This module will discuss the architecture and different parameters of analog switches and multiplexers.

Switch Architecture

To fully understand the functionality of an analog switch, we must first look at its internal structure and operational limits.

Standard Switch Architecture

A standard CMOS switch shown in Figure 1 uses both N- and P-channel MOSFETS for the switch element, digital control logic, and driver circuitry. Connecting the N- and P-channel MOSFETs in parallel permits bidirectional operation, allowing the analog input voltage to extend to supply rails while maintaining almost constant on-resistance over the signal range.

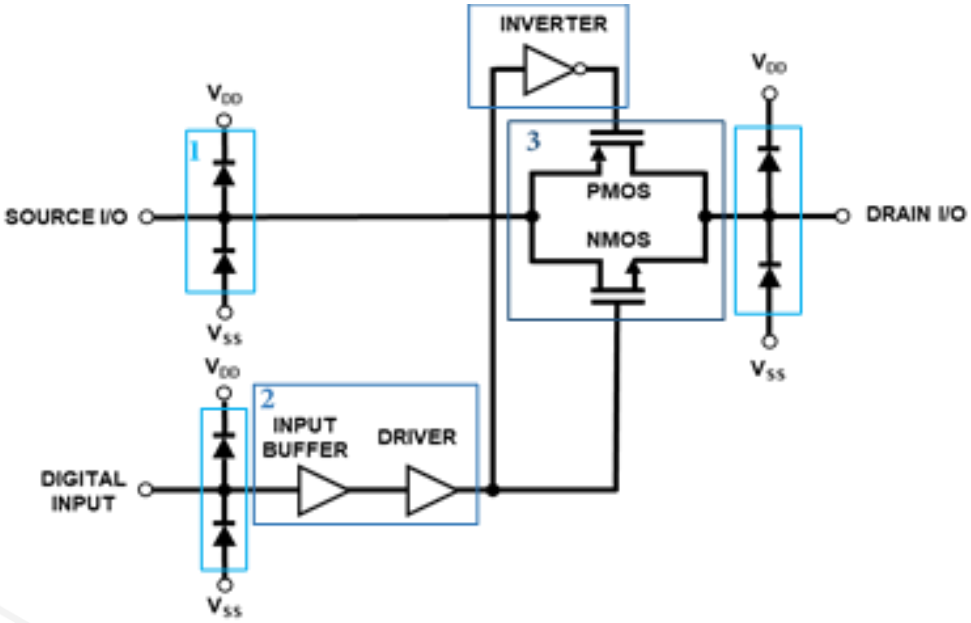

Figure 1. Standard Switch Architecture

Protection Diodes

The source, drain, and digital logic terminals include clamping diodes to the supplies to provide electrostatic discharge (ESD) protection illustrated in Figure 1, Lebel 1. Reversed-biased in standard operation and do not pass current unless the signal exceeds the supply voltage. The diodes vary in size depending on the process, but they are kept small to minimize the leakage current.

Digital Block

It is composed of an input buffer, driver, and inverter as shown in Figure 1, Label 2. The input buffer and inverter provide the logic to the gate of the transistors. The driver is used to provide sufficient drive capability to pass the signals along the succeeding stage and to set the turn on and off time of the PMOS and NMOS transistors.

T-Gate Switch

The T-Gate Switch is the parallel combination of the PMOS and NMOS transistors that operates in a non-saturated region as shown in Figure 1, Label 3. The N-channel device is on for the positive gate-to-source voltage, V_{GS}, and off for negative V_{GS}. The opposite is true for the P-channel device.

NMOS-only Switch Architecture

Another switch architecture is composed of a bidirectional NMOS transistor and a digital control input block on its gate shown in Figure 2.

The on-resistance is dependent on the voltage difference between the gate and the source of the switch. Some of its advantages are its simplicity and faster switching times. One of its disadvantages is, as the input/output signal increases toward the supply voltage, the on-resistance increases due to lower V_{GS}

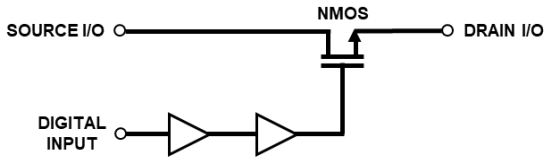

Figure 2. NMOS Switch

Key Specifications and Error Sources

The key specification is the detailed description of the switches and multiplexers parameters and performance for a given test conditions across the voltage supplies and temperature ranges.

Figure 4 shows the detailed key specifications of the ADG141x. The ADG141x series are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an industrial CMOS, iCMOS process.

In designing a system, it is important to understand the error sources in analog switches and multiplexers. Many affect the AC and DC performance, while others only affect AC. These error sources are also specified in the datasheet key specifications. Figure 3 shows the equivalent circuit of two adjacent CMOS switches.

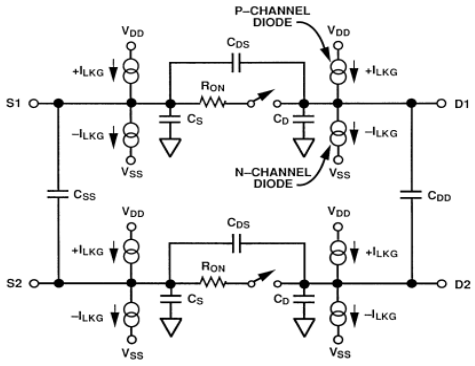

Figure 3. Equivalent Circuit of Two Adjacent CMOS Switches

Data Sheet ADG1411/ADG1412/ADG1413

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	1.5			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 23
	1.8	2.3	2.6	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.3			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.03			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 24
	±0.55	±2	±12.5	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
Drain Off Leakage, I_D (Off)	±0.03			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 24
	±0.55	±2	±12.5	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
Channel On Leakage, I_D, I_S (On)	±0.15			nA typ	V_S = V_D = ±10 V; see Figure 25
	±2	±4	±30	nA max	
ADG1411WBCPZ-REEL Only	±3		±40	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	

Figure 4. Equivalent Circuit of Two Adjacent CMOS Switches

Voltage Supply Levels

The ADG141x is specified at different supply voltage levels. As shown in the Figure 4, it is specified at ±15 V dual supply operation. The positive supply voltage, V_{DD} level is +15 V, the negative supply voltage, V_{SS} level is -15 V, and the analog signal range on either source or drain input output, V_D or V_S is from V_{DD} to V_{SS} range.

On Resistance

Figure 5 shows the on-resistance performance of both N-type and P-type devices with changing applied signal. These non-linear resistances can cause errors in DC accuracy as well as AC distortion. The T-Gate CMOS switch solves this problem. The on-resistance is minimized, and linearity is also improved.

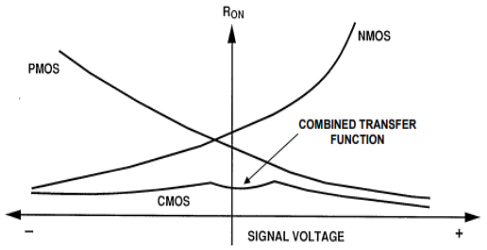

Figure 5. CMOS Switch On-Resistance vs. Signal Range

Figure 4 shows the on-resistance curve that is flat over the full analog input signal range. It ensures the excellent linearity and low distortion when switching signals. Figure 6 shows the on-resistance curve at different supply level of the ADG141x family.

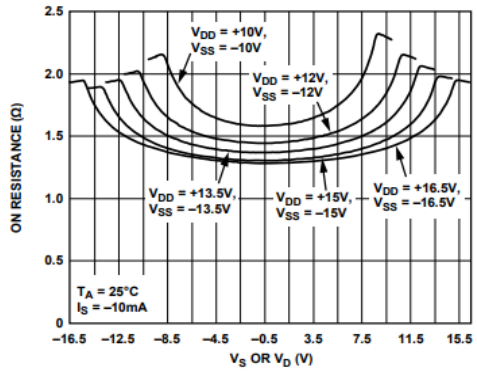

Figure 6. On Resistance vs. V_S or V_D Dual Supply

To measure the on-resistance of a switch, it is tested using the setup shown in Figure 7. The test conditions used is also specified on the ADG141x datasheet.

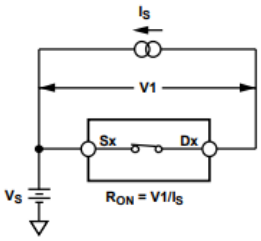

Figure 7. On Resistance Test Circuit

Leakage Current

The leakage currents are current measured at the source and drain when the switch is on or off. It is measure using the test setup shown in Figures 8 and 9. Datasheet parameters are specified as the following:

Source Off Leakage, $I_{S(OFF)}$

It is the algebraic sum of the leakage currents in or out of an OFF channel, source input, predominantly caused by parasitic reverse-biased diode junctions. Note that the channel is switched off using the digital control logic.

Drain Off Leakage, $I_{D(OFF)}$

The algebraic sum of the leakage currents in or out of an OFF channel, drain input, mainly due to the parasitic reverse-biased diode junctions. Note that the channel is switched OFF using the digital control signal.

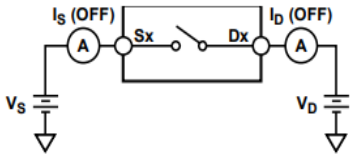

Figure 8. Off Leakage Test Circuit

Source/Drain On Leakage, $I_{D(ON)}$/ $I_{S(ON)}$

The algebraic sum of the leakage currents in or out of an ON channel, predominantly caused by parasitic reverse-biased diode junctions. Note that when the channel is ON, $I_{D(ON)} = I_{S(ON)}$.

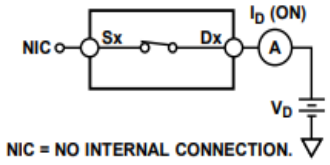

Figure 9. On Leakage Test Circuit

The ADG141x leakage current over temperature range graph is shown in Figure 10.

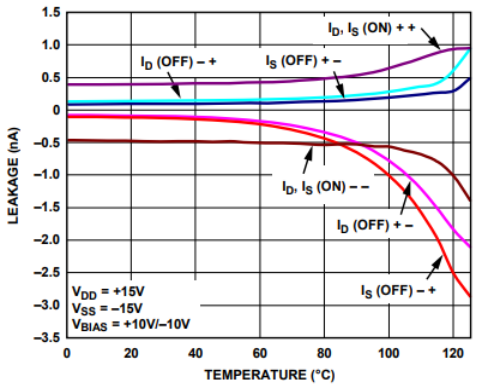

Figure 10. Leakage Current vs. Temperature, ±15 V Dual Supply

Figure 11 shows the DC errors associated with a single CMOS switch in the on-state. The switch DC performance is mainly affected by the on-resistance and leakage current parameters during on state. A resistive path is created by the R_G-R_{ON}-R_{LOAD} combination that produces a gain error. The leakage, I_{LKG} current flows through these resistances.

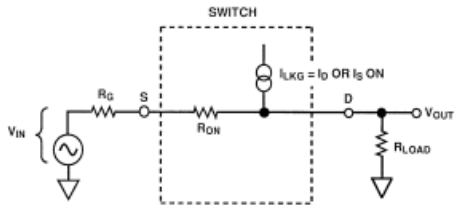

Figure 11. Effects of R_{ON}, R_{LOAD}, I_{LKG}

The gain errors caused by the on-resistance can be calibrated using system gain trim, but variations along with the applied signal voltage can introduce distortion that can't be calibrated. Low resistance circuits are more subject to errors due to R_{ON}, while high resistance circuits are affected by leakage currents. The equations below show how these parameters affect dc performance.

$$\mathbf{V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]}$$

If $R_G = 0$,

$$\mathbf{V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}R_{ON}}{+R_{ON} + R_{LOAD}}\right]}$$

When the switch is off, leakage current can introduce errors as shown in Figure 12. The leakage current flowing through the load resistance develops corresponding voltage error at the output.

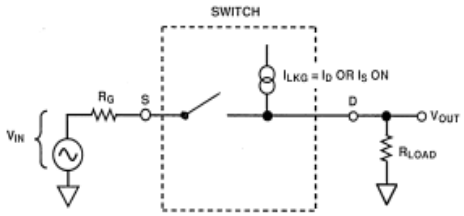

Figure 12. Effects of I_{LKG} and R_{LOAD}

$$\mathbf{V_{OUT} = I_{LKG}\ x\ R_{LOAD}}$$

Digital Input Interface

To understand the compatibility issues relating to interfacing ICs operated at different VDD supplies, it is useful to first look at the structure of a typical CMOS logic stage as shown in Figure 13.

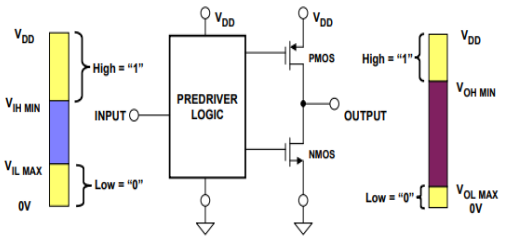

Figure 13. Typical CMOS IC Output Driver Configuration

Input High Voltage, V_{INH}

It is the minimum voltage level required by the buffer to recognize a logic high.

Input Low Voltage, V_{INH}

It is the maximum voltage level required by the input buffer to recognize a logic low.

Input Low and High Current, I_{INL} and I_{INH}

It is the input current of the digital input when high or when low.

A summary of the existing logic standards using these definitions is shown in Figure 14. This chart helps connect two integrated circuits (ICs) operating on different logic level standards and avoids possible interface problems.

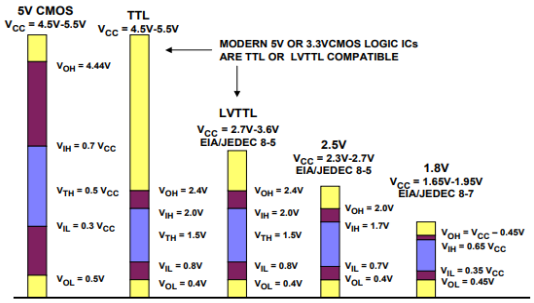

Figure 14. Standard Logic Levels

Digital Input Capacitance, C_{IN}

It is the digital input capacitance which is measured between the digital input and ground shown in Figure 15.

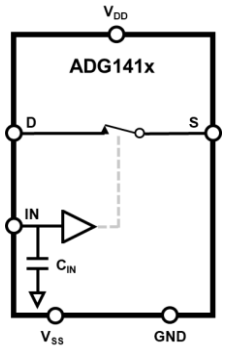

Figure 15. Digital Input Capacitance

The lower part of the ADG141x datasheet contains the dynamic characteristics section of the switch. It consists of the timing, charge injection, off isolation, crosstalk, total harmonic distortion plus noise (THD+N), bandwidth, insertion loss, and pin capacitances.

	DYNAMIC CHARACTERISTICS[1]					
5	t_{ON}	100			ns typ	R_L = 300 Ω, C_L = 35 pF
		150	170	190	ns max	V_S = 10 V; see Figure 30
	t_{OFF}	90			ns typ	R_L = 300 Ω, C_L = 35 pF
		120	140	160	ns max	V_S = 10 V; see Figure 30
	Break-Before-Make Time Delay, t_D (ADG1413 Only)	25			ns typ	R_L = 300 Ω, C_L = 35 pF
				10	ns min	V_{S1} = V_{S2} = 10 V; see Figure 31
6	Charge Injection, Q_{INJ}	−20			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
7	Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
8	Channel-to-Channel Crosstalk	−100			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
9	Total Harmonic Distortion + Noise	0.014			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 29
10	−3 dB Bandwidth	170			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
11	Insertion Loss	−0.35			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
12	C_S (Off)	23			pF typ	V_S = 0 V, f = 1 MHz
	C_D (Off)	23			pF typ	V_S = 0 V, f = 1 MHz
	C_D, C_S (On)	116			pF typ	V_S = 0 V, f = 1 MHz

Figure 16. Dynamic Characteristics

Timing Characteristics

The timing specifications of the switch determine the amount of time it takes for it to change its state. Timing parameters are measured using the test circuits shown in Figure 17, Figure 20, Figure 21, and Figure 22.

On Time, T_{ON}

The delay between the 50% level of the digital control (IN) and the 90% of the output switching on as shown in Figure 17.

Off Time, T_{OFF}

The delay between the 50% level of the digital control (IN) and the 10% or 90% of the output switching off as shown in Figure 17.

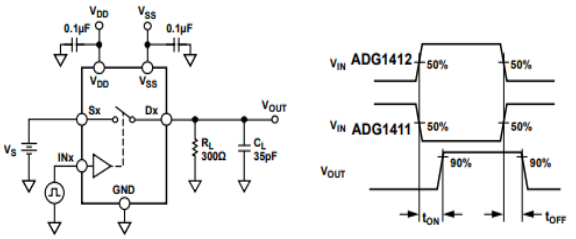

Figure 17. Switching Time Test Circuit

For SPDT and MUX, the on and off time are measured between the enable digital input and switch output. Transition and break-before-make time delays are also specified.

Transition Time, T_{TRANS}

The delay between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another. TTRANSITION is measured using the test circuit shown in Figure 18.

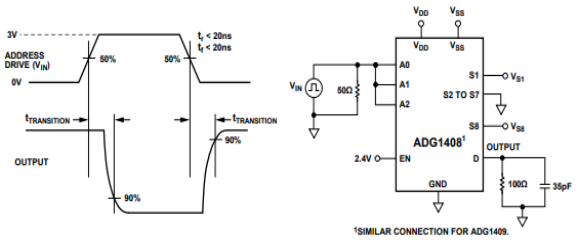

Figure 18. Transition Time Test Circuit

Enable On Time, T_{ON} (EN)

The delay between the 50% level of the enable digital input (EN) and the 90% of the output switching on as shown in Figure 19.

Enable Off Time, T_{ON} (EN)

The delay between the 50% level of the enable digital input (EN) and the 10% or 90% of the output switching on as shown in Figure 19.

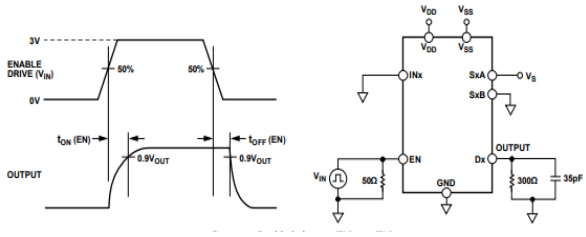

Figure 19. Enable Time Test Circuit

Break-before-Make Time, T_{BBM}

The off time measured between the 80% point of both switches when switching from one address state to another as shown in the test circuit of Figure 20.

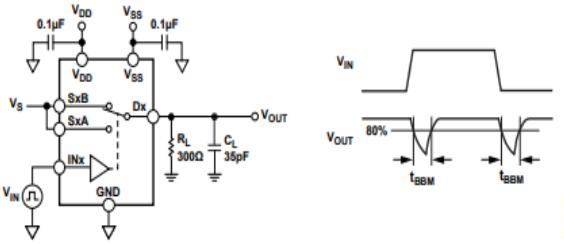

Figure 20. Break-before-Make Time Test Circuit

Charge Injection

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from V_{DD} to V_{SS}, or vise versa) at the gate of the CMOS switch. The fast change in voltage injects a charge into the switch output through the gate-drain capacitance, C_Q as shown in Figure 21.

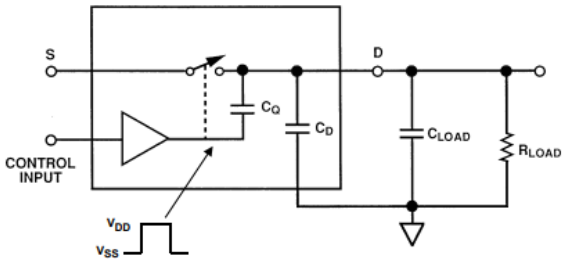

Figure 21. Charge Injection Model

The charge injection introduces a step change in output voltage when switching as shown in Figure 22 test circuit. The change in output voltage ΔV_{OUT}, is a function of the amount of charge injected, Q_{INJ} (which is in turn a function of the gate-drain capacitance, C_Q) and the load capacitance, C_L.

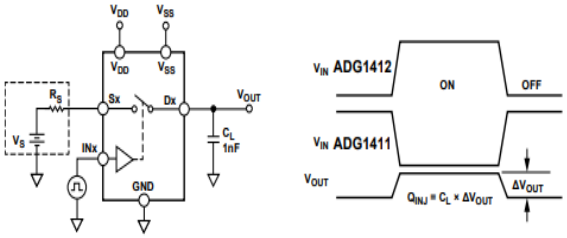

Figure 22. Charge Injection Test Circuit

The charge injection parameter is measured with respect with the source voltage as shown in Figure 23.

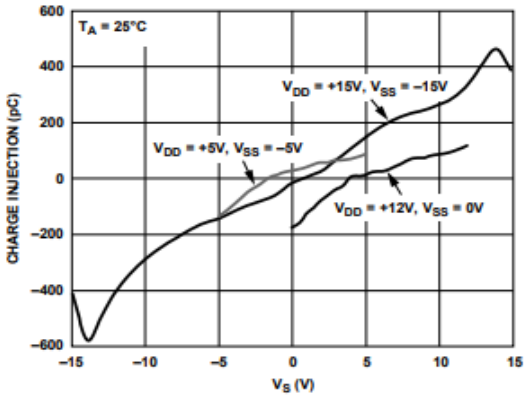

Figure 23. Charge Injection vs. Source Voltage

Off Isolation

The off isolation is a measure of unwanted signal coupling in an off switch through the drain to source capacitance, C_{DS}. It is a parameter affected by the degradation of the AC performance of CMOS switches due to parasitic capacitances. In the circuit representation shown in Figure 24, the C_{DS} not only creates a zero in the response in the on-state, but it also degrades the feedthrough performance of the switch during the off-state.

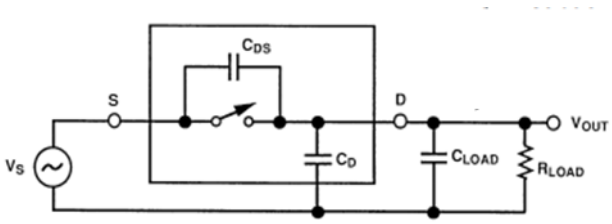

Figure 24. Off Isolation Model

The off isolation is measured using the test circuit shown in Figure 25.

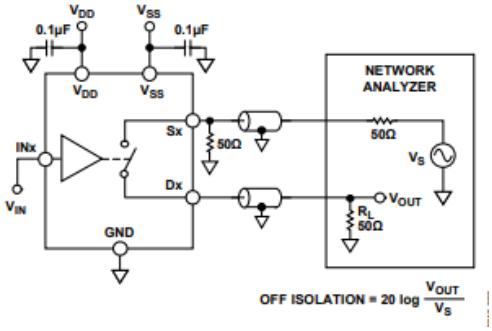

Figure 25. Off Isolation Test Circuit

The ADG141x has an off-isolation response as a function of frequency shown in Figure 26.

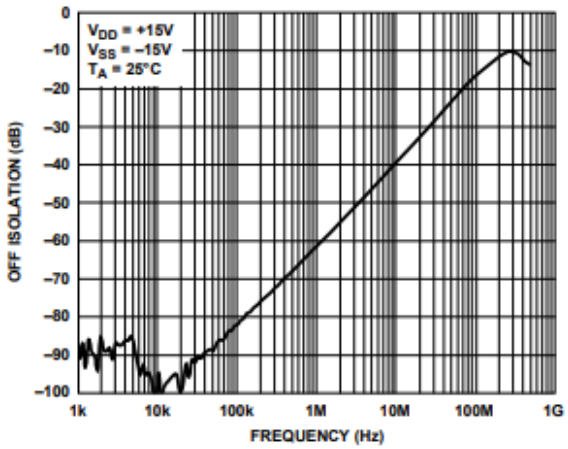

Figure 26. Off Isolation vs. Frequency, ±15 V Dual Supply

Crosstalk

When switching channels, another problem arises as the switch capacitances retained charge. This charge can cause transients in the switch output, as shown in Figure 27. When S2 is initially closed and S1 is open, CS1 and CS2 are charged. As S2 opens, the charge remains on CS1 and CS2 as S1 closes. The output will not stabilize until the CS1 and CS2 fully discharges and settles to 0 V.

Crosstalk is related to the capacitances between two switches. It is modeled as the C_{SS} capacitance as shown in Figure 27.

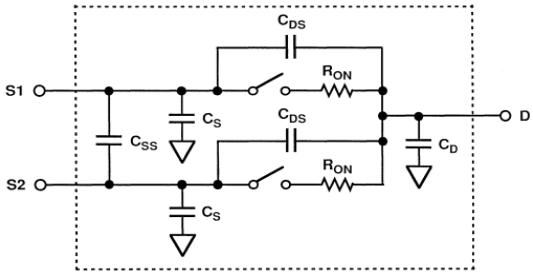

Figure 27. Crosstalk Model

The crosstalk parameter is measured using the test circuit shown in Figure 28.

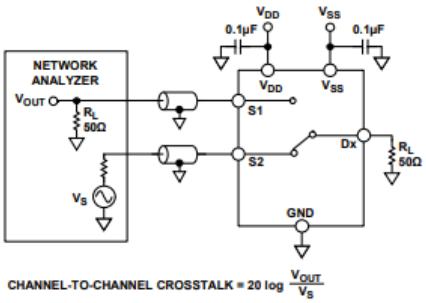

Figure 28. Crosstalk Test Circuit

The ADG141x has a crosstalk response as a function of frequency shown in Figure 29.

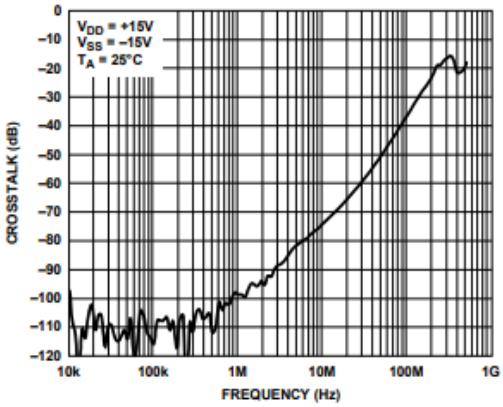

Figure 29. Crosstalk vs. Frequency, ±15 V Dual Supply

Total Harmonic Distortion plus Noise (THD+N)

The total harmonic distortion plus noise, THD+N, is the ratio of the signal power at the fundamental frequency to the signal power of all other harmonics observed at the switch output, V_D with a pure sinusoid applied to the switch input, V_S. The best THD+N values are obtained by using very low R_{ON} switch that also exhibits good R_{ON} flatness. It is measured using the test setup shown in Figure 30.

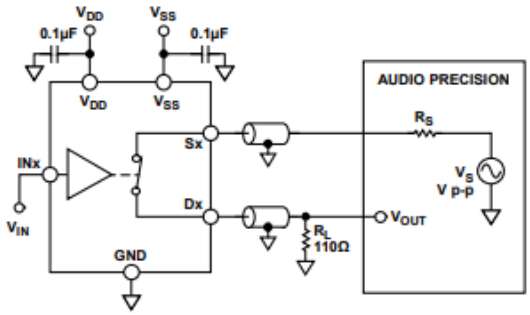

Figure 30. THD+N Test Circuit

The ADG141x has a THD+N response as a function of frequency shown in Figure 31.

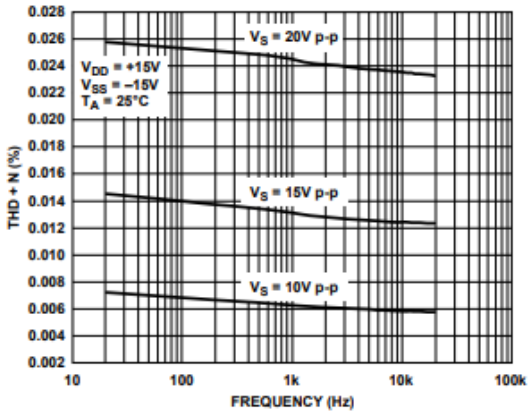

Figure 31. THD+N vs. Frequency, ±15 V Dual Supply

Bandwidth

The bandwidth is the frequency range, when the switch is on, measured from 0 Hz to a frequency where small signals pass through switch and attenuated by -3 dB. It is also called half-power point of the switch. It is measured using the test circuit shown in Figure 32.

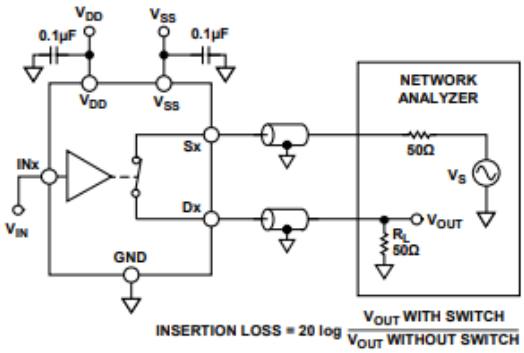

Figure 32. Bandwidth Test Circuit

Insertion Loss

The insertion loss is the measure of the small signal attenuation caused by loss of transferable power due to reflections at the input of the switch channel which is on. Reflections are caused by mismatch of load due to RON. Insertion loss is measured in the passband and with a test circuit shown in Figure 32.

The ADG141x has an insertion loss response as a function of frequency shown in Figure 33.

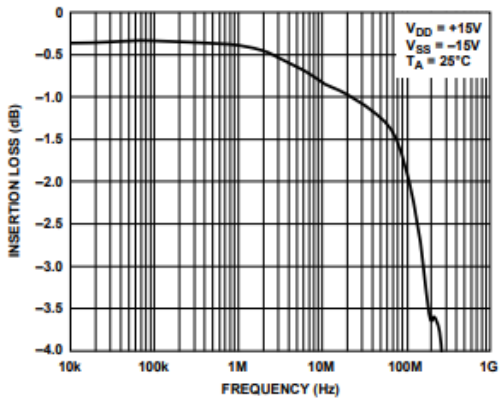

Figure 33. On Response vs. Frequency, ±15 V Dual Supply

Pin Capacitance

The pin capacitances are the capacitances measured at the source and drain of the switch in an on and off condition.

Off Source Capacitance, $C_{S(OFF)}$

It is the off-switch source capacitance which is measured with reference to ground as shown in Figure 34.

Off Drain Capacitance, $C_{S(OFF)}$

It is the off switch drain capacitance which is measured with reference to ground as shown in Figure 34.

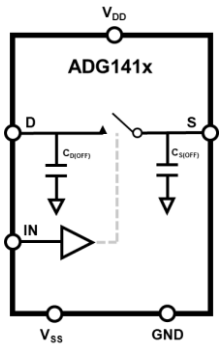

Figure 34. Off Source and Drain Capacitance

On Source and Drain Capacitance, $C_{S(ON)}$/ $C_{D(ON)}$

It is the on-switch drain capacitance which is measured with reference to ground as shown in Figure 35.

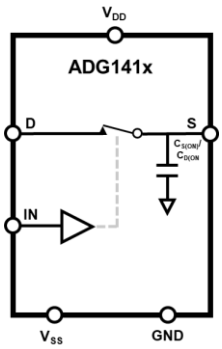

Figure 35. On Source and Drain Capacitance

Choosing the Correct Switch for Applications

There are a large range of switches and multiplexers based on different technology strands that are available in the market that has single and multiple switch elements with various signals ranges, variety of packages to suit the breath off application needs. Deciding on the best switch or multiplexer for your application can be a difficult task.

As an individual switch cannot be optimized on every vector, Analog Devices offers a large and varied portfolio that is classified into families based on the technology choice, supply voltage, precision, robustness, and overvoltage fault detection and protection that come in industry-leading package sizes. To select the correct switch for your application, the following are the key specifications to consider:

Supply Voltage

Analog Devices offers high-performance switches and multiplexers across voltage supply ranges suitable for different applications. It has high and low-voltage options that have their performance advantages. It consists of traditional supplies, low voltage levels, and single and dual supply options.

Specifications

The portfolio offers a breadth of precision performance capability. Across applications there will be differences in the key performance specification requirements and priorities for the switch. This table summarizes key switch performance specifications and a general indicator of performance targets.

Table 1: Switch Specification Summary

Parameter	Definition	Recommendations
Supply Voltage	Voltage of the analog switch	Must cover the desired analog input signal range
On Resistance, R_{ON}	Resistance of the closed switch path	Lower is better (precision application)
On Leakage	Leakage currents into/out of the switch channel	Lower is better
Charge Injection, Q_{INJ}	Disturbance to the signal from the control input	Lower is better
Bandwidth	Frequency range of the switch in the on state and where the switch attenuates the input signal by 3 dB	Higher is better
Off Isolation	Measure of the signal coupling through a switch in the off state	Higher is better
Insertion Loss	Measure of the loss when the switch is in the on state	Lower is better
Crosstalk	Measure of signal coupling to the adjacent channel	Higher is better
Timing	Time required for signal to travel through the switch	Lower is better

Configurations

Do you need a switch or multiplexer? For a switch, do you need an SPST? How many channels do you need? Do you need a bus switch or a level translator (for digital signals)? These are guide questions that will help you identify the switch configuration.

Interface

Interface options are as follows:

Inter-Integrated Circuit, I2C

The Inter-Integrated Circuit (I2C) bus is a two-wire serial interface. It is a bi-directional bus with connections minimized using a serial data line (SDA), a serial clock line (SCL), and a common ground to carry all communications.

Serial Peripheral Interface, SPI

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface widely used between the microcontroller and peripheral ICs. It communicates in full-duplex mode using a master-slave architecture.

It has four logic signals: SCLK (Serial Clock), MOSI (Master Out, Slave In), MISO (Master In, Slave Out), and CS (Chip Select).).

Parallel

The parallel interface is a multiline channel that transmits multiple bits of data simultaneously.

Package Type

The ADI switches and multiplexers portfolio offers different package options up to 75% savings on board space compared to the nearest competitors. Details of these package types and information are shown in the table 2 below.

Table 2: Switch Specification Summary

Package Type	Lead Count Options	Example Body by Size (mm)	Sample Board Area (mm^2)	Example Pitch (mm)	Package Code
TSSOP	14/16/20/24/28/38	5 x 4.4 x0.65 (14-lead)	32 (14-lead)	0.65 (14-lead)	RU-X
MSOP	8/10	3 x3 x 1.1 (8-lead)	14.7 (8-lead)	0.65 (8-lead)	RM-X
LFCSP	8/10/12/16/20/24/32/40/48	3 x 3 x 0.9 (8-lead)	9 (8-lead)	0.65 (8-lead)	CP-X
SOT-23	5/6/8	2.9 x 1.6 x 1.175 (5-lead)	8.12 (5-lead)	0.95 (5-lead)	RT/RJ-X
SC70	5/6	1.25 x 2 x 0.65 (5-lead)	4.2 (5-lead)	0.65 (5-lead)	KS-X
Mini LFCSP	10/16	1.4 x 1.6 x 0.6 (10-lead)	2.08 (10-lead)	0.4 (10-lead)	CP-X
WLFCSP	5/6/10/12/16	0.9 x 1.29 x 0.5 (5-ball)	1.16 (5-ball)	0.5 (5-ball)	CB-X

Additional Protection Requirements

Every system requires different protection requirements for optimized robustness and protection. The ADI offers switches and multiplexers with latch-up proof, power-off protection, and overvoltage protection.

iCMOS Switch Alternative

Update the old switches to a new iCMOS switch using the alternatives below. These are available in different packages that give up to 75% space savings compared to other industry-standard solutions.

a. **ADG12xx :** It offers groundbreaking low capacitance per channel and the industry's lowest, most stable charge injection performance over the full signal range with only 1.5 pF off capacitance and >1 pC charge injection.

b. **ADG14xx :** It is a family of ±15 V switches and multplexers that has the industry's lowest on-resistance (5 Ω max) and excellent on-resistance flatness (0.5 Ω).

c. **ADG8xx :** It is a family of low voltage (<5 V) switches and multiplexers and has sub 1 Ω on-resistance that are ideal for precision applications where on-resistance switching is critical.

Latch-up Immune and High ESD Alternative

Utilize the switches below to transition from an iCMOS to a latch-up immune or use a combination of both latch-up and high ESD alternatives. These are pin-to-pin compatible with the iCMOS.

a. **ADG54xx :** Latch-up immune, low R_{ON}, high ESD protected switches and multiplexers.

b. **ADG52xx :** Latch-up immune, low Q_{INJ}, low leakage switches and multiplexers.

Overvoltage Protection and Detection Alternative

Utilize the overvoltage protection and detection alternatives below to transition from iCMOS, latch-up immune, or the former overvoltage protection switch to the new overvoltage protection and detection family. This family also provide latch-up immunity.

a. **ADG54xxF :** Overvoltage protection and detection switches and multiplexers with high ESD protection, optimized for low R_{ON}.

b. **ADG52xxF :** Overvoltage protection and detection switches and multiplexers with high ESD protection, optimized for low leakage, Q_{INJ}, and capacitance.

Self-Check

Circuit Simulation. Plot and measure the following parameters of the switch and multiplexer using the test circuits mentioned in their respective datasheets. Use their LTspice models for the simulation and provide your observations.

1. **ADG1412: 1.5 Ω On Resistance, ±15 V, +12 V, and ±5 V *i*CMOS, Quad SPST Switches**
    a. On-resistance (Plot Only)
    b. On Time, T_{ON}
    c. Off Time, T_{OFF}
    d. Charge Injection
    e. Off Isolation
    f. Crosstalk
    g. Bandwidth

2. **ADG1408: 4 Ω On Resistance, 8-Channel, ±15 V, +12 V, and ±5 V *i*CMOS Multiplexer**
    a. On-resistance (Plot Only)
    b. On Time, T_{ON}
    c. Off Time, T_{OFF}
    d. Charge Injection
    e. Off Isolation
    f. Crosstalk
    g. Bandwidth

References

Analog Devices. 2008. *MT-088 Tutorial: Analog Switches and Multiplexers Basics*. Retrieved from https://www.analog.com/media/en/training-seminars/tutorials/MT-088.pdf

Analog Devices. 2009. *MT-098 Tutorial: Low Voltage Logic Interfacing*. Retrieved from https://www.analog.com/media/en/training-seminars/tutorials/mt-098.pdf

Analog Devices, 1.5 Ω On Resistance, ±15 V/+12 V/±5 V, *i*CMOS, Quad SPST Switches, ADG1412 Datasheet, May 2008 [Revised Jan. 2020]

Analog Devices, 4 Ω R_{ON}, 4-/8-Channel, ±15 V/+12 V/±5 V, *i*CMOS, Multiplexers, ADG1408 Datasheet, Aug. 2006 [Revised June 2016]

Analog Devices. 2011. *Choosing the Correct Switch, Multiplexer, or Protection Product for Your*

Application. Retrieved from https://www.analog.com/media/en/news-marketing-collateral/product-selection-guide/choosing_switches_or_muxes.pdf

Analog Devices. 2019. *Switches and Multiplexers Portfolio*. Retrieved from https://www.analog.com/media/en/news-marketing-collateral/product-selection-guide/Switches_Multiplexers_Product_Selection_Guide.pdf