



# User’s Guide: Configuring the EVAL-AD2428WD1BZ Evaluation Board as a Local Power Slave Node

## Purpose

The purpose of this document is to guide the user to evaluate the EVAL-AD2428WD1BZ board (hereafter referred to as WD1BZ) in the following configurations:

- WD1BZ Master Node <---> WD1BZ Local Powered Slave (LPS) Node using the ADAU1452 SigmaDSP Audio Processor & ADAU1761 SigmaDSP Audio CODEC

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## System and Software Requirements

S. No	Software Component	Version	Comments
1.	A2B Software*	19.4.0*	Copy the DLL's (A2B.DLL, A2BStack.DLL) into SigmaStudio Installation Directory. Refer to the A2B Quick Start Guide for more details (C:\Analog Devices\ADI_A2B_Software-Rel19.4.0\Docs)
2	SigmaStudio	4.6*	SigmaStudio 4.6 product page: <a href="https://www.analog.com/en/design-center/evaluation-hardware-and-software/software/ss_sigst_02.html#software-overview">https://www.analog.com/en/design-center/evaluation-hardware-and-software/software/ss_sigst_02.html#software-overview</a>

\*Please contact A2B SW team for latest updates.

## Hardware Requirements

S. No	Name of Board	Type of Board/ Node	Quantity
1	EVAL-AD2428WD1BZ Rev. 1.1	Master/ Local Powered Slave (LPS)	2
2	Twisted Pair A2B Cable with DuraClik Connectors	-	1
3	12V Power Supply	-	2
4	USBi I2C Adapter	v1.5	1
5	Audio source (non-grounded)	e.g., PC/Mobile phone	2
6	Aux Cable	-	2
7	Audio Sink Devices	3.5mm Jack Headphones	2
8	SPDIF cable		4
9	SPDIF input source like say e.g., AP		1
10	SPDIF output sink e.g., AP		1

## Procedure

WD1BZ Master Node <---> WD1BZ Local Powered Slave (LPS) Node **Using** the ADAU1452 SigmaDSP Audio Processor & ADAU1761 SigmaDSP Audio CODEC

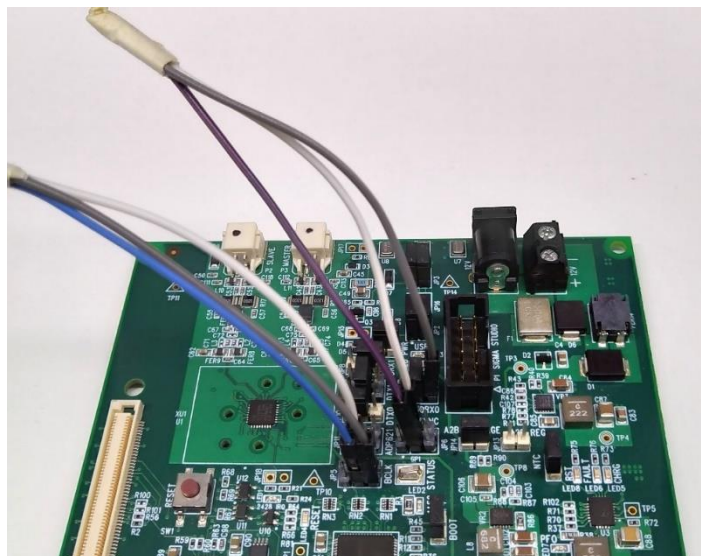
## Jumper Settings

Place the jumpers on WD1BZ **Master** and WD1BZ **LPS** boards as per the tables below.

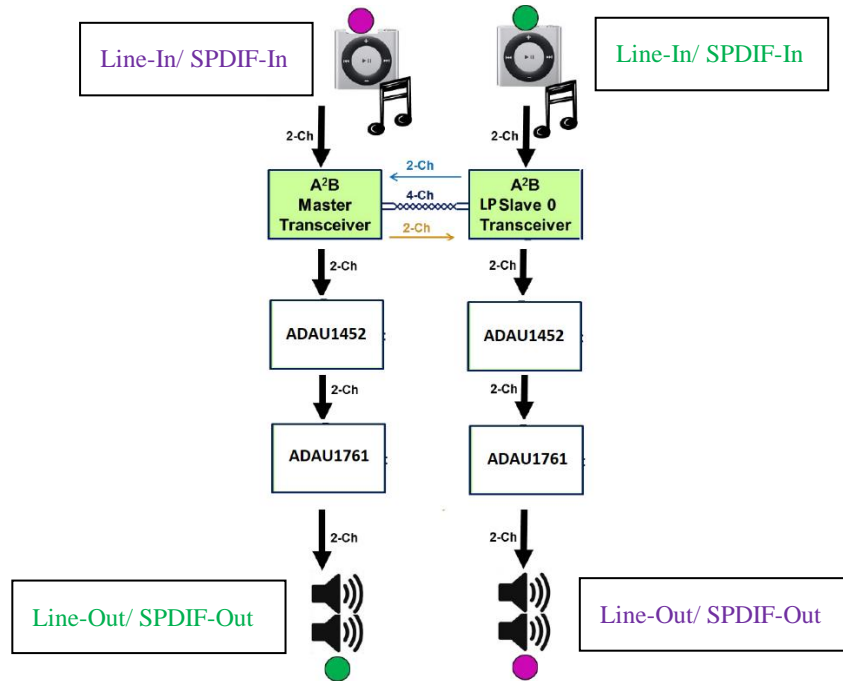
Jumper	Master	Comments
JP1 (A2B power)	Install	-
JP2	Uninstall	Install when phantom power or hybrid power support is required
JP3	Uninstall	
JP4 (BOOT)	Install	Self-Boot option disabled
JP5 (BCLK)	3-4	ADAU1452_BCLK_OUT0 -> AD2428_BCLK
JP6 (SYNC)	3-4	ADAU1452_LRCLK_OUT0 -> AD2428_SYNC
JP7 (DRX0)	3-4	ADAU1452_SDATA_OUT0 -> AD2428_DRX0
JP8 (DRX1)	2-3	ADAU1452_SDATA_OUT1 -> AD2428_DRX1 If Secondary Rx data line DRX1 is desired. Uninstall if only primary data line DRX0 is required.
JP9 (DTX1)	3-4	AD2428_DTX1 -> ADAU1452_SDATA_IN1 If Secondary Tx data line DTX1 is desired. Uninstall if only primary data line DTX0 is required.
JP10 (DTX0)	1-2	AD2428_DTX0 -> ADAU1452_SDATA_IN0
JP11 (ADMP621 CLK)	Uninstall	-
JP12 (NTC)	Install	-
JP13 (A2B_REG)	Uninstall	-
JP14 (VOLTAGE)	Uninstall	Install/ Uninstall depending on VIN requirement. Installed -> VIN = 7V Uninstalled -> VIN = 8V
JP19 (1961 BCLK)	1-2	ADAU1761 MCLK from CLKOUT of ADAU1452

Jumper	LPS	Comments
JP1 (A2B power)	Install	-
JP2	Uninstall	Install when phantom power or hybrid power support is required
JP3	Uninstall	
JP4 (BOOT)	Install	Self-Boot option disabled
JP5 (BCLK)	3-4-5	AD2428_BCLK -> ADAU1452_BCLK_OUT0 & ADAU1452_BCLK_IN0 <b>(Use a three-way wire connector – See picture below)</b>
JP6 (SYNC)	JP5(3-4) & JP7(5)	AD2428_SYNC -> ADAU1452_LRCLK_OUT0 & ADAU1452_LRCLK_IN0
JP7 (DRX0)	3-4	ADAU1452_SDATA_OUT0 -> AD2428_DRX0 JP7.5 should be connected to SYNC signals on JP6.3 & JP6.4 <b>(Use a three-way wire connector – See picture below)</b>
JP8 (DRX1)	2-3	ADAU1452_SDATA_OUT1 -> AD2428_DRX1 If Secondary Rx data line DRX1 is desired. Uninstall if only primary data line DRX0 is required.
JP9 (DTX1)	3-4	AD2428_DTX1 -> ADAU1452_SDATA_IN1 If Secondary Tx data line DTX1 is desired. Uninstall if only primary data line DTX0 is required.
JP10 (DTX0)	1-2	AD2428_DTX0 -> ADAU1452_SDATA_IN0
JP11 (ADMP621 CLK)	Uninstall	-
JP12 (NTC)	Install	-
JP13 (A2B_REG)	Uninstall	-
JP14 (VOLTAGE)	Uninstall	Install depending on VIN requirement. Installed -> VIN = 7V Uninstalled -> VIN = 8V
JP19 (1961 BCLK)	1-2	ADAU1761 MCLK from CLKOUT of ADAU1452

## LPS board Jumper Connections



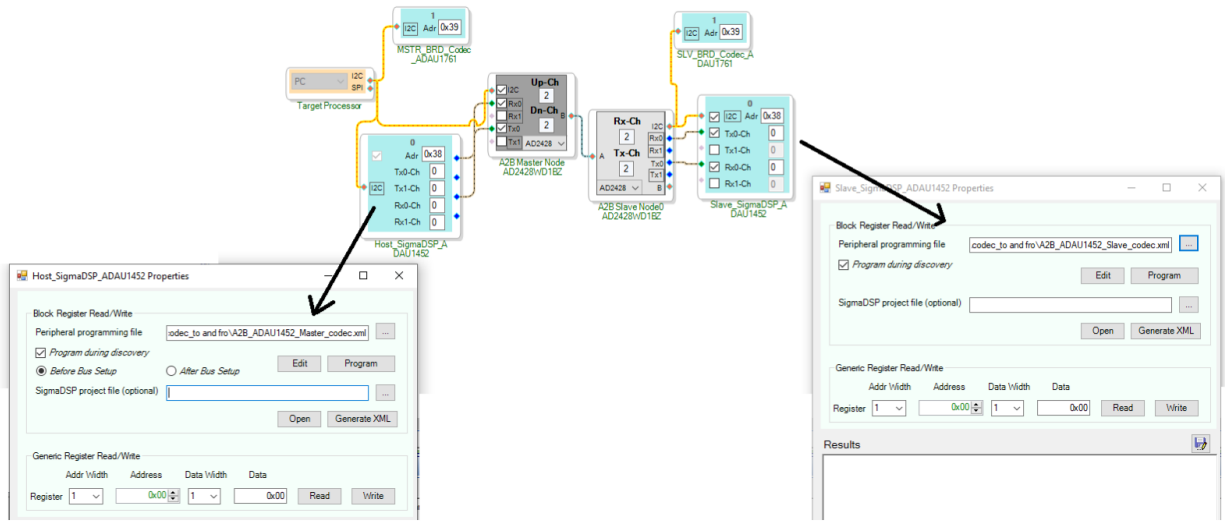
## Audio Routing – Block Diagram



### Instructions

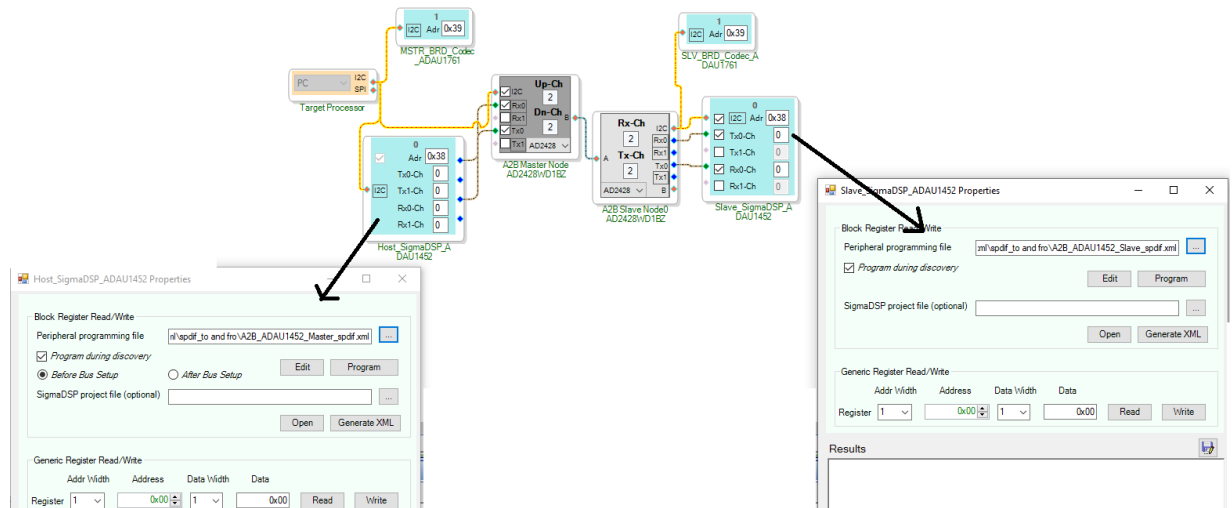
#### A: Routing of analog signals.

1. Connect the A2B Master node to an LPS Slave node using a A2B UTP cable.
2. Make sure the jumpers are configured as per the tables above.
3. Open the A2B schematics `..\A2B_Project.dspproj`.
4. For routing of the analog signals used the `'..\xml\codec_to and fro'` Master and slave .xml files.
5. Link Compile Download the A2B schematics onto the target
6. Feed audio data by connecting the Aux cable to the Line-In connector J3 of the Master, verify the audio on the slave node Line-Out J4 with the help of headphones.
7. Feed audio data by connecting the Aux cable to the Line-In connector J3 of the Slave node, verify the audio on the Master node Line-Out J4 with the help of headphones.



## B: Routing of SPDIF signals.

1. Connect the A2B Master node to an LPS Slave node using a A2B UTP cable.
2. Make sure the jumpers are configured as per the tables above.
3. Open the A2B schematics ..\A2B\_Project.dsproj.
4. For routing of the SPDIF signals used the **'..\xml\ spdif\_to and fro'** Master and slave .xml files.
5. Link Compile Download the A2B schematics onto the target.
6. Feed audio data by connecting the SPDIF cable to the SPDIF-IN J1 of Master node, verify the audio signals from SPDIF-Output J2 using the Analog decoders on the slave node.
7. Feed audio data by connecting the SPDIF cable to the SPDIF-IN J1 of Slave node, verify the audio signals from SPDIF-Output J2 using the Analog decoders on the Master node.



=====END=====