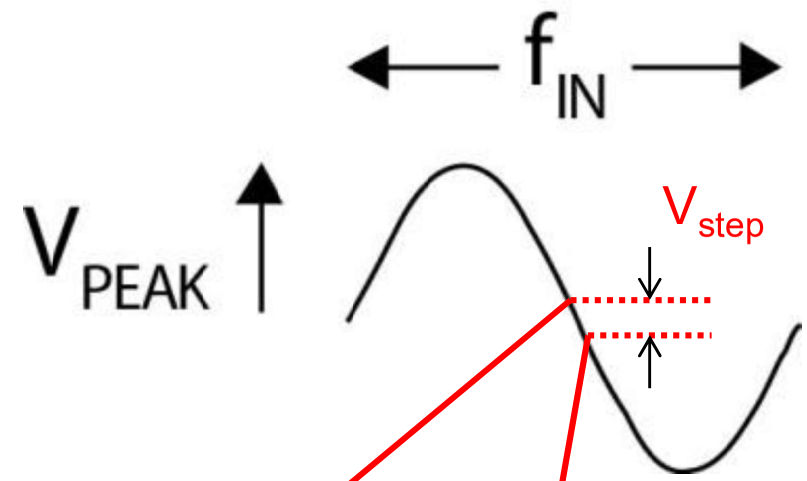
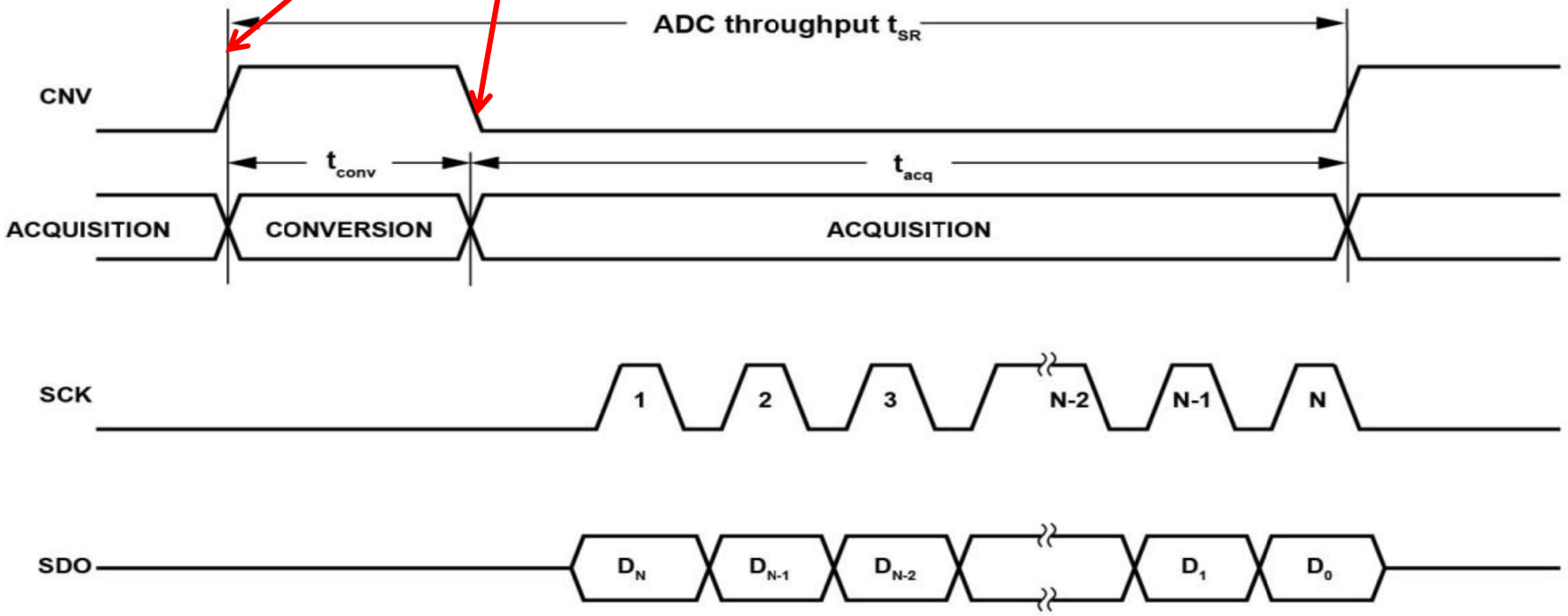
Calculating the RC filter Bandwidth

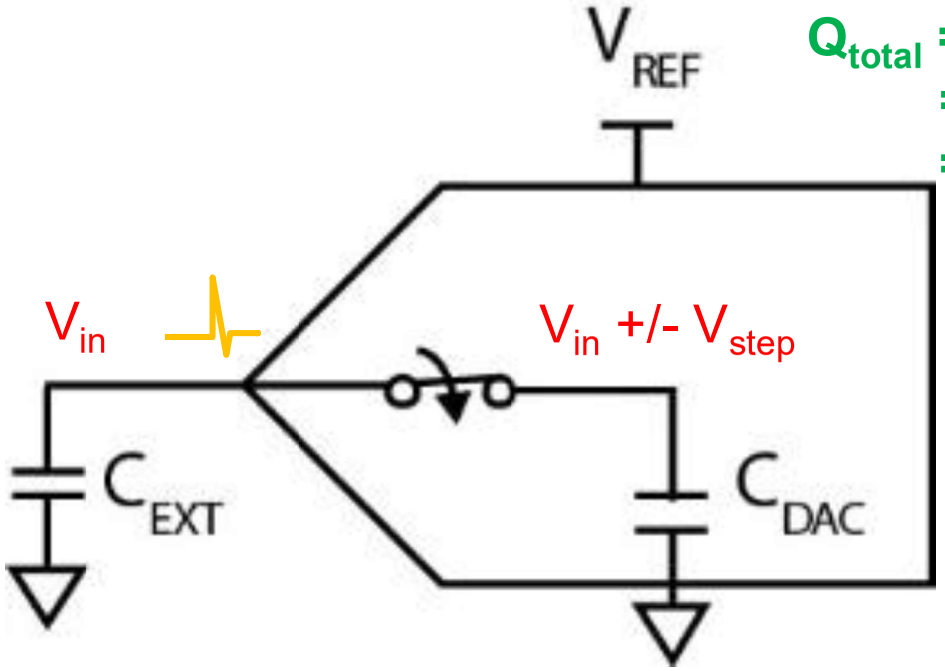
Vin = Vpeak * sin(2*π*f_{in}*t)



- Cap DAC disconnected from input during t_{conv}
- Max rate of change = $2\pi f_{in} V_{peak}$
- Amount signal moves during conversion $V_{step} = 2\pi f_{in} V_{peak} t_{conv}$
- Min step ~100mV



Calculating the RC filter Bandwidth

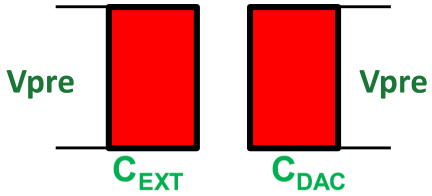


$$Q_{total} = (C_{EXT} + C_{DAC}) \times Vpre + C_{EXT} \times Vstep$$
$$= C_{EXT} \times Vin + C_{DAC} \times Vpre$$
$$= C_{EXT} \times (Vin - \Delta V) + C_{DAC} \times (Vin - \Delta V)$$
$$\Delta V = C_{DAC} / (C_{EXT} + C_{DAC}) * Vstep$$

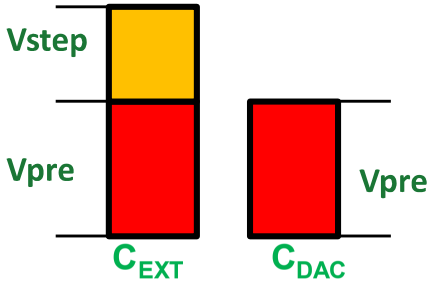
- Charge sharing at beginning of acquire
- C_{EXT} usually >> C_{DAC}, typically ~100 times
- Step is attenuated by $\frac{C_{DAC}}{C_{EXT}+C_{DAC}}$
- Time to settle the remaining step is the reverse settling time

Calculating the RC filter Bandwidth

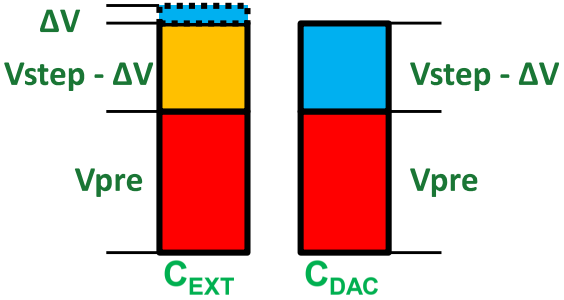
End of Previous Acquisition



Forward Settled



Reverse Settled



$$Q_{total} = (C_{EXT} + C_{DAC}) \times Vpre + C_{EXT} \times Vstep$$
$$= C_{EXT} \times Vin + C_{DAC} \times Vpre$$
$$= C_{EXT} \times (Vin - \Delta V) + C_{DAC} \times (Vin - \Delta V)$$

$$\Delta V = C_{DAC} / (C_{EXT} + C_{DAC}) * Vstep$$

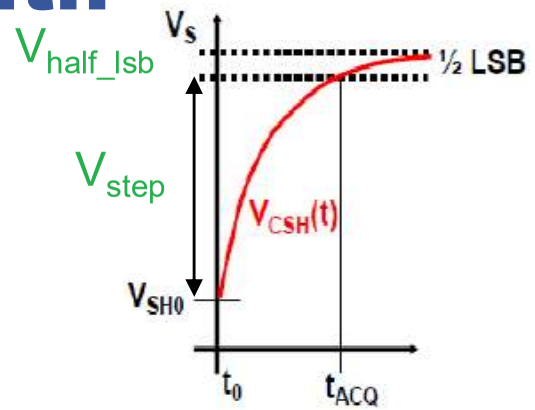
Calculating the RC filter Bandwidth

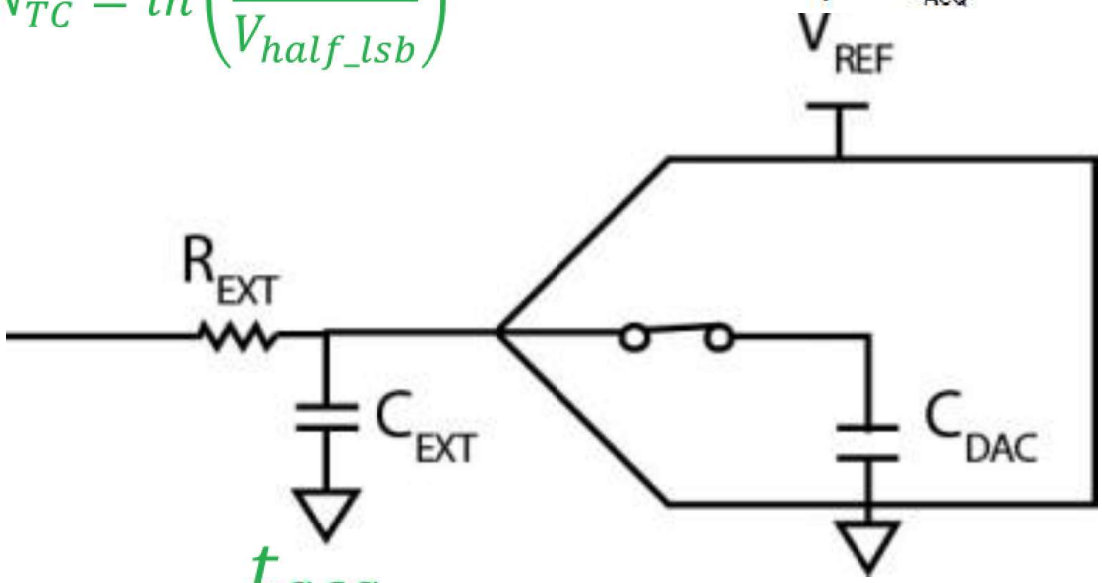
- Need to settle remaining step to a half lsb within t_{acq}
- Number of time constants N_{TC} calculated for exponential settling
- The required RC time constant (τ) is the acquire time divided by number of time constants
- Or RC BW = $\frac{1}{2\pi\tau}$

$$(1 - e^{-t/\tau}) * V_{step} = V_{step} - V_{half\_lsb}$$

$$t = N_{TC} * \tau$$

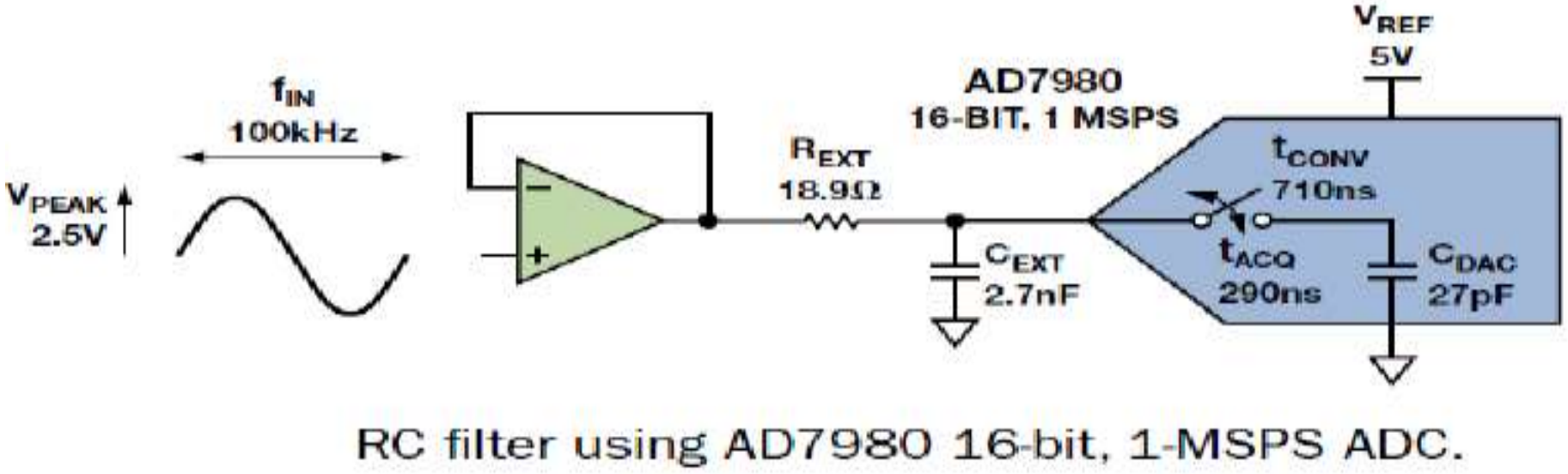
$$N_{TC} = ln\left(\frac{V_{step}}{V_{half\_lsb}}\right)$$





$$\tau = \frac{t_{acq}}{N_{TC}}$$

RC Calculation Example

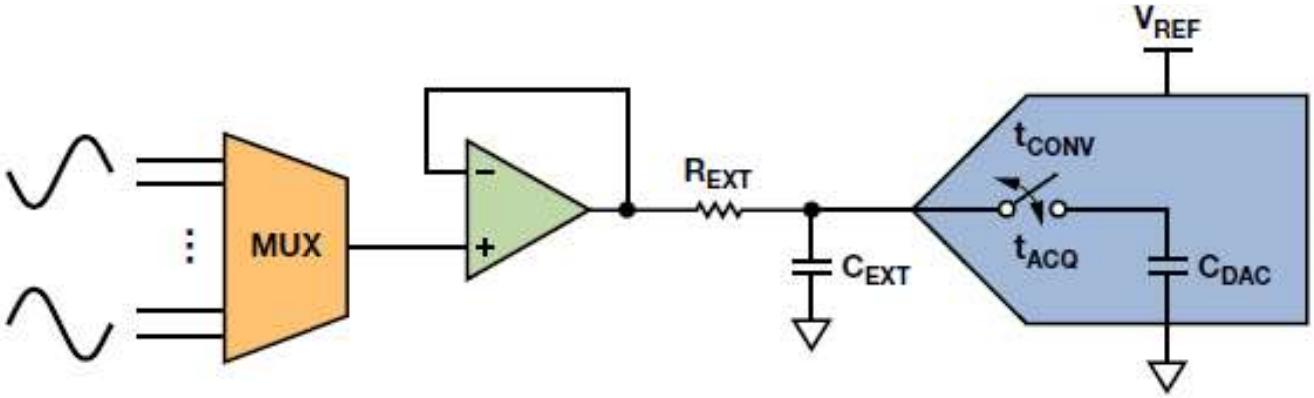


RC filter using AD7980 16-bit, 1-MSPS ADC.

- **Max Voltage step before attenuation =** $2\pi(100KHz)(2.5V)(710nS) = 1.115V$
- **Assume C_{EXT} = 2.7nF. Attenuated V_{step}=** $\frac{1.115V(27\,pF)}{2.7nF + 27\,pF} = 11.042mV$
- **Calculate number of time constants** $N_{TC} = \ln\left(\frac{11.042mV}{\frac{5V}{2^{16+1}}}\right) = 5.668$
- **RC time constant** $\tau = \frac{290nS}{5.668} = 51.16nS$ **=> BW = 3.11 MHz, R_{EXT}=18.9ohm**

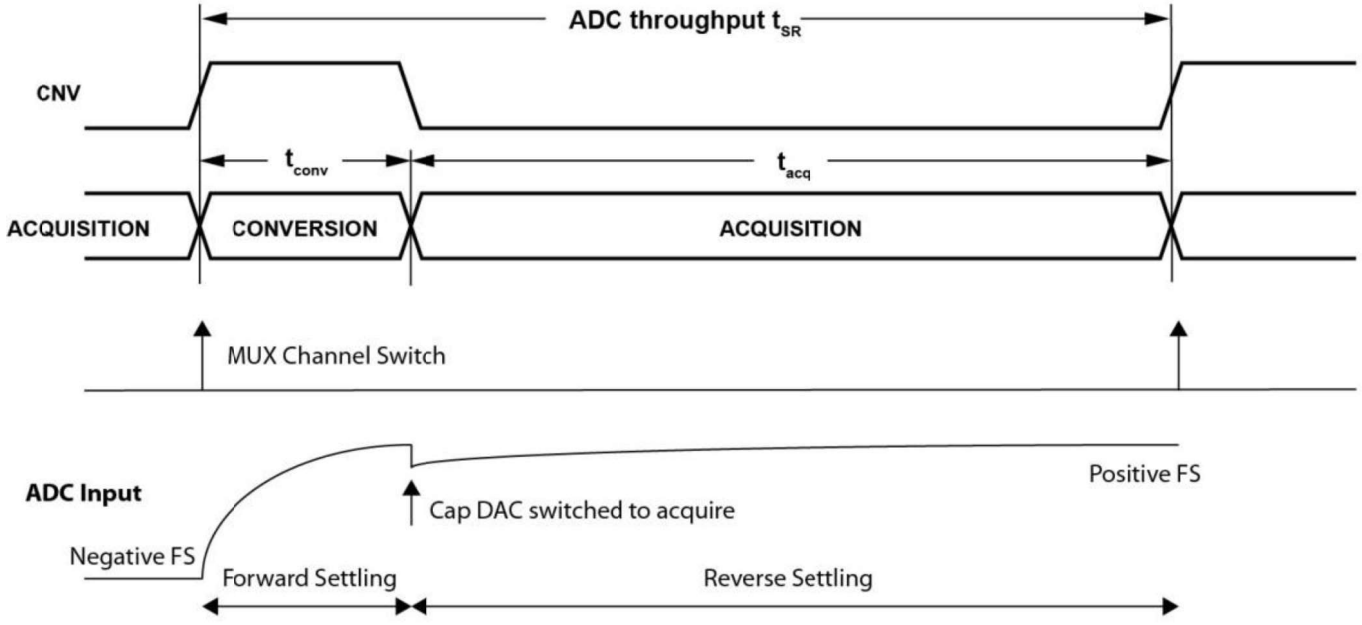
Multiplexed Input Considerations

- Large step (up to full-scale) when switching channels
- Step size is 5V in this case
- RC BW = 3.93 MHz (40.5ns) R=15, C=2.7nF
- Forward settling require 12 TC for 16 bit
- Forward settling = 486ns < t_{conv} (710ns)

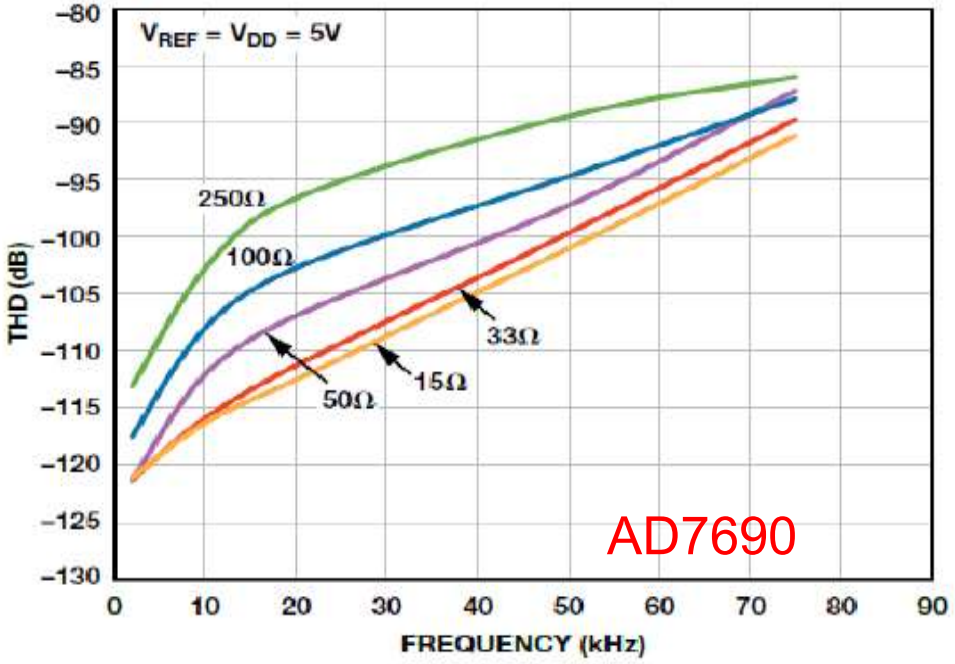


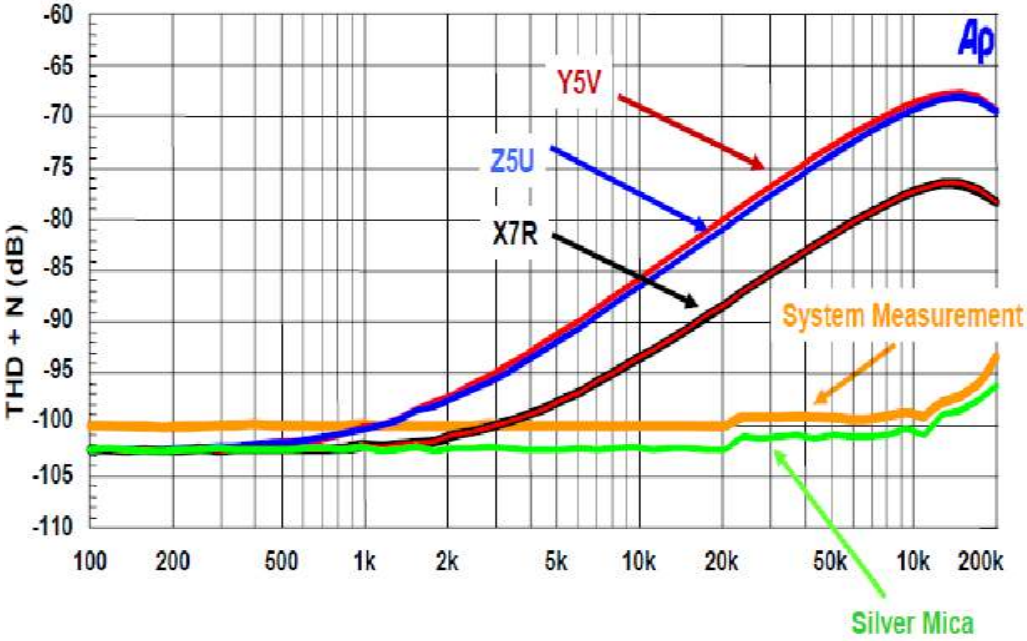
Multiplexed setup

AD7980
16-bit 1MSPS



R and C values considerations





- C_{EXT} attenuates 'kick', typically couples of nF
  - Too large leads to instability of driver
  - Low voltage, low frequency coef NP0 caps
- R_{EXT} helps amp drive C_{EXT}
  - Too small degrades phase margin of driver => instability or ringing
  - Too large results in increased distortion. May be ok for lower f_{in}
- Low R_{EXT} requires low R_{out} amplifier