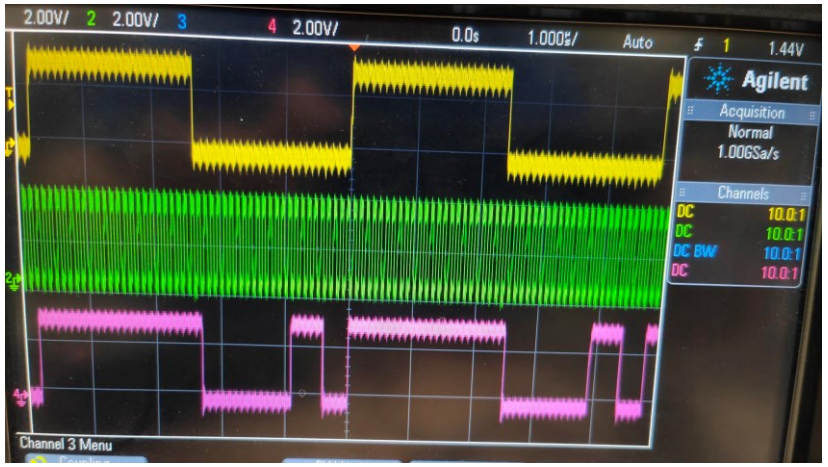
Identified bug and workarounds

- Problem encountered with the communication between FPGA and ADC.
- Reading CHIP_ID register. Sending 1000000000000001, should expect 00101111, but I get back 11110000.
- Notice that the SDIO signal from ADC (probe ADC pin directly) is showing an unexpected decay, which triggers the FPGA to output the incorrect digital levels.
- The SDIO voltage from AD9273 for Logic 1 is 1.79 V, but V_IH of Artix-7 in LVCMOS33 IO Standard is 2 V minimum.



CSB SCLK SDIO (FPGA)

CSB SCLK SDIO (ADC)