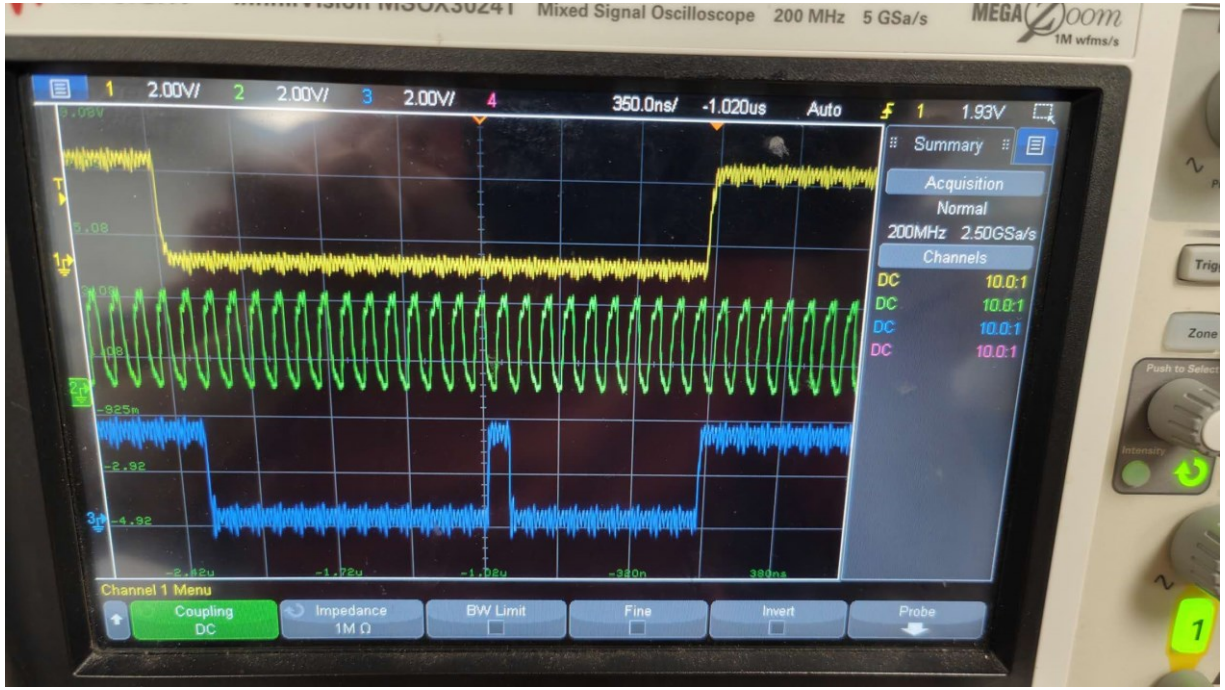
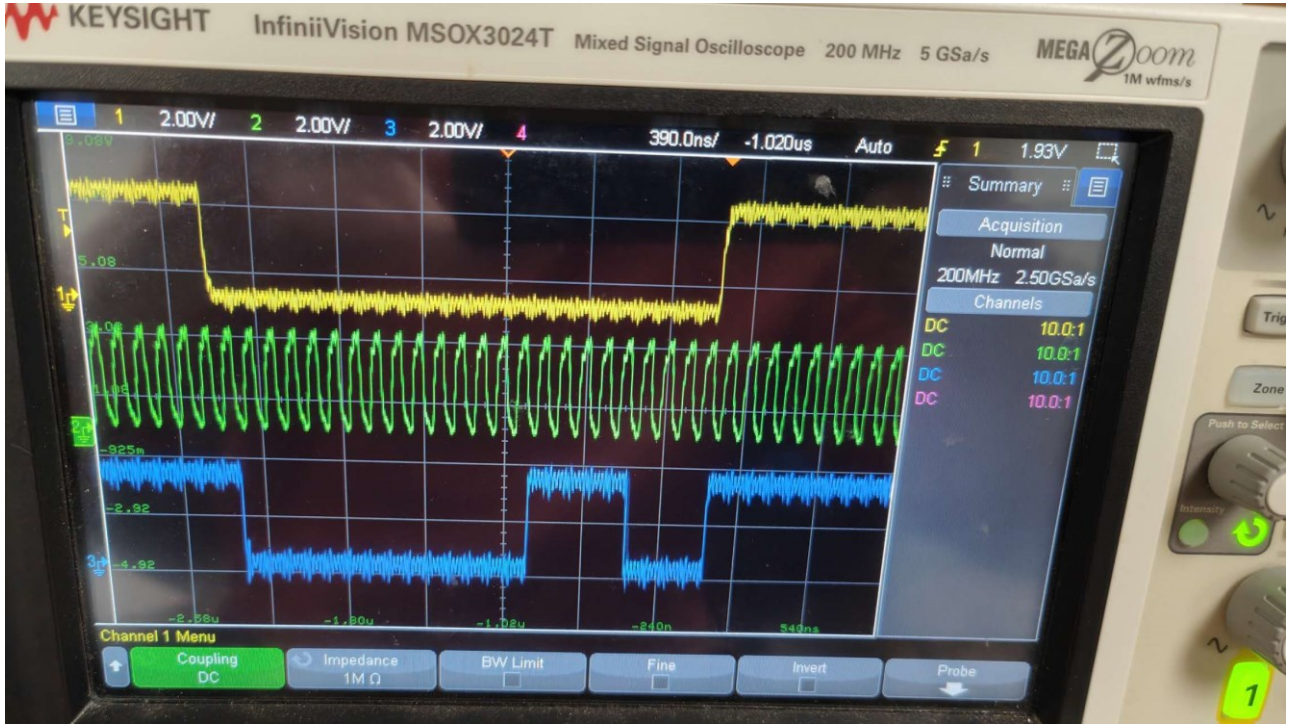



CSB

SCLK

SDIO

**Reading CHIP_GRADE register. Sending 1000000000000010, should expect XX10XXXX, but I get back 00000000.**



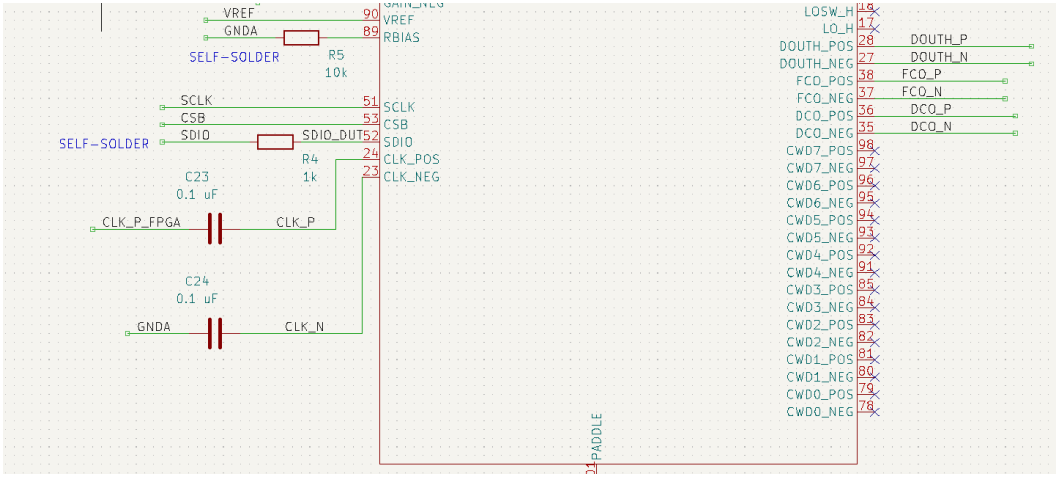

CSB

SCLK

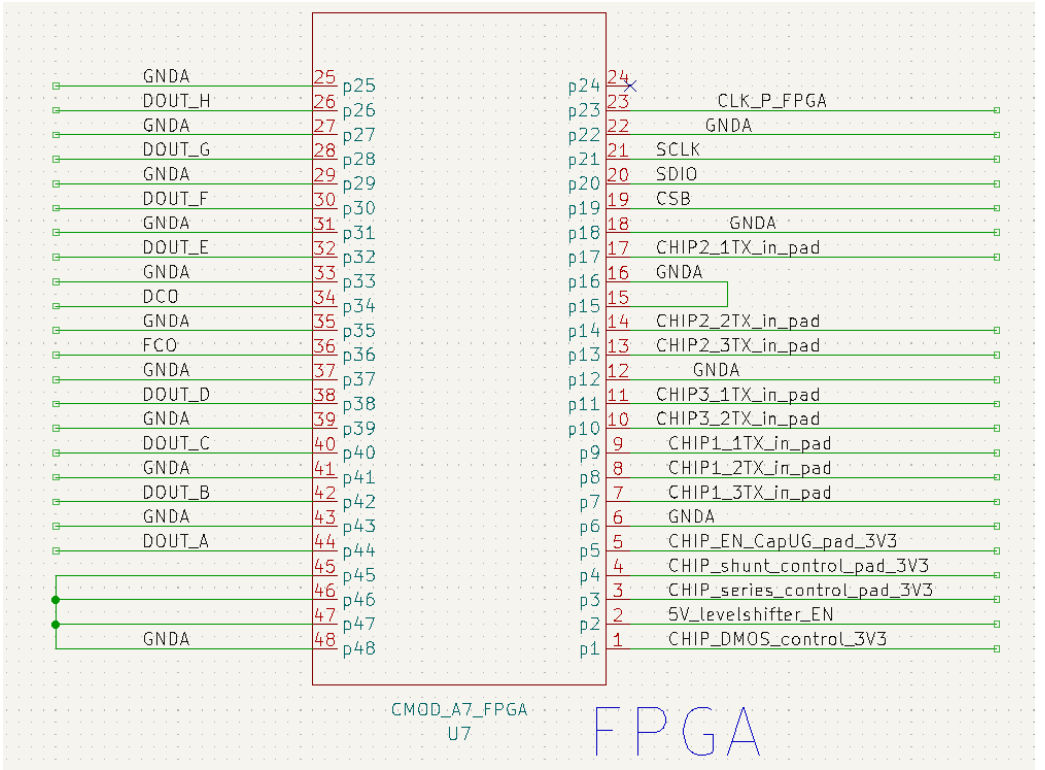
SDIO

**Reading CHIP_ID register. Sending 1000000000000001, should expect 00101111, but I get back 11110000.**

# ADC

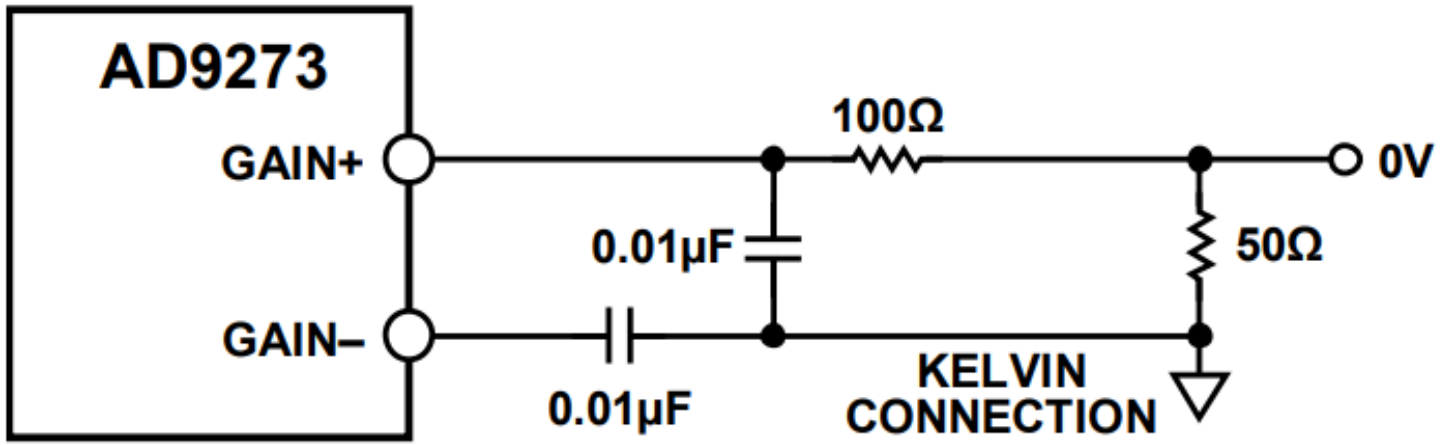



# FPGA




**Basically, the SCLK, CSB pins of the ADC are directly connected to the FPGA (Digilent CMOD A7).**

**The SDIO pin has a 1 k resistor in series to limit the current, as per datasheet guidance.**




**The GAIN+ and GAIN- pins were connected like this to a 0 V, i.e. ground.**