Quick Start Guide for testing the AD9230 Customer Evaluation Board with the HSC-ADC-EVALCZ in external trigger mode
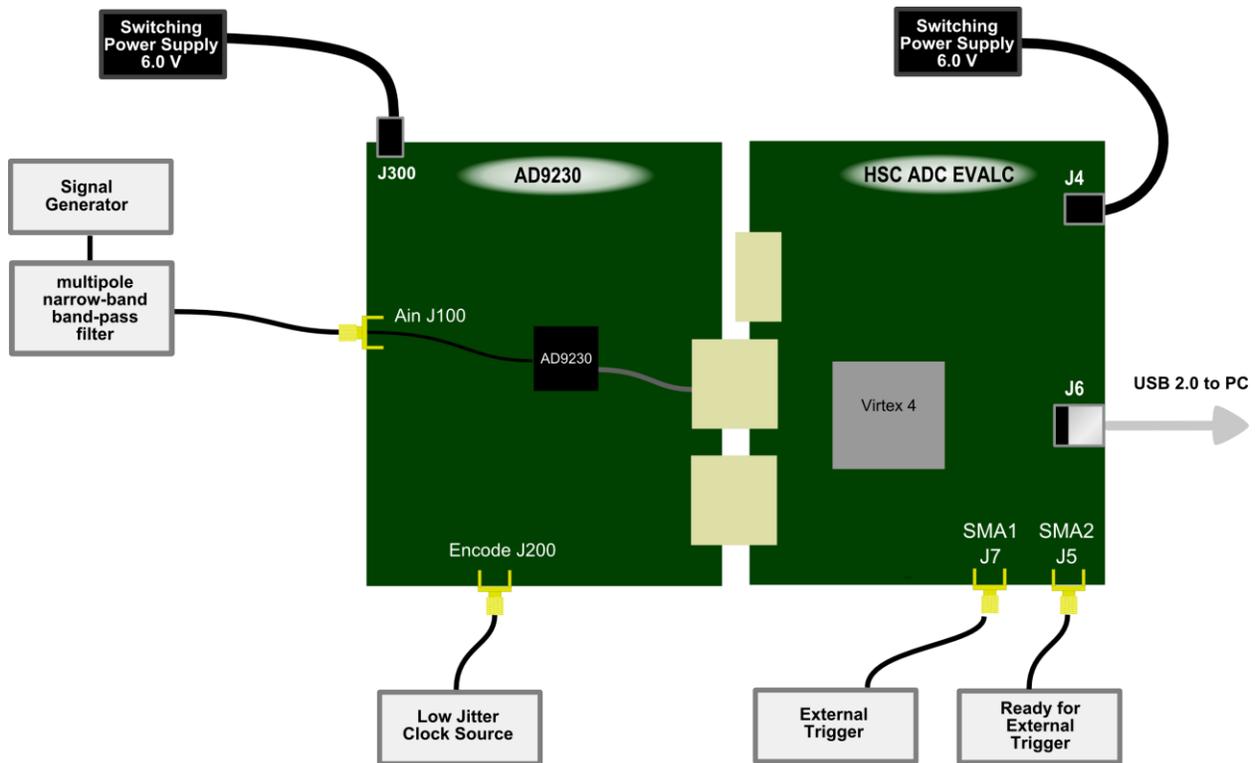

Figure 1: AD9230 ADC Evaluation Board – HSC ADC EVALCZ Data Capture Board

Equipment Needed
► Analog signal source and antialiasing filter
► Analog Clock Source
► PC running Windows XP or Vista
► USB 2.0 port recommended (USB 1.1-compatible)
► AD9230 evaluation board
► HSC-ADC-EVALCZ FPGA Based Data Capture Kit

Documents Needed
► AD9230 Datasheet
► HSC-ADC-EVALCZ FPGA Based Data Capture Kit Datasheet
► VisualAnalog User Manual
► High Speed ADC SPI Control Software User Manual, AN-878
► Interface to High Speed ADC via SPI Control Port User Manual, AN-877

Software Needed
► VisualAnalog version 1.9.7.26 or higher

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o AD9230_LVDS_Ext_Trig.bin
► SPIController version 1.0.55.3 or higher

All documents and software are available at http://www.analog.com/fifo.
For any questions please send an email to highspeed.converters@analog.com.

Testing

Hardware setup:
1. Connect the AD9230 evaluation board and the HSC-ADC-EVALCZ board together as shown in Figure 1.

2. Connect one 6V, 2A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the AD9230 board.

3. Connect one 6V, 2A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.

4. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable. (Connect to J6.)

5. On the ADC evaluation board, provide a clean, low jitter clock source to connector J200 at the desired Sample Rate and set the amplitude to 14dBm.

6. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal at connector J100. Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (ADI uses TTE, Allen Avionics, and K&L band-pass filters.)

7. Connect the external trigger source to SMA 1(J7). This needs to be 3.3V CMOS signal with a pulse width greater than the period of the clock.

VisualAnalog Setup:
8. Open VisualAnalog on the PC. After the "New Canvas" window appears, click on the "New" tab and select "AD9230". Then select the canvas that corresponds to the type of testing that you are doing. Click "open". When prompted to program the FPGA, Select "No" to skip programing.

9. Expand the Canvas if necessary by clicking on the "Expand Canvas" button. Click the "Settings" button of the "ADC Data Capture" block, click on the "capture" tab and navigate to the AD9230_LVDS_Ext_Trig.bin file. Click the "Program" Button. The 'DONE' LED should illuminate on the HSC-ADC-EVALCZ board indicating that the FPGA has been correctly programmed.

SPI Controller Setup:
10. Click SPI Controller under the Tools menu in VisualAnalog to open the SPI Controller software. (See note below if SPI controller is not listed.) If prompted for a configuration file, select the AD9230spiR03.cfg file. If not, check the title bar of the window to see which configuration is loaded. If necessary, choose "Cfg Open" from the "File" menu and select the

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above configuration file. Note that the CHIP ID(1) field may be filled whether the correct SPI Controller configuration file is loaded or not.

Note: If SPI Controller is not listed in the "Tools" menu, first make sure that it is installed and then select "External Tools" from the "Tools" menu in VisualAnalog. Click the Add button on the External Tools from the "Tools" menu in VisualAnalog window. Under "Display Text: " enter "SPI Controller". Then, enter the path to the SPI controller executable.

11. Click the New DUT button ( ) in SPI Controller.

Testing:

12. Click the Run button ( ) in VisualAnalog.

13. Wait for the "Ready to Capture" signal on SMA2 (J5). This usually happens very fast and can be skipped in many instances.

14. Apply the trigger signal to SMA1 (J7), after this signal is applied, you should see the captured data displayed in VisualAnalog.

15. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the "Fund Power" reading in the left panel of the VisualAnalog FFT window.)

16. If desired, click on File>Save Form as in the FFT window to save the FFT plot.

Troubleshooting

► *SPI Controller does not work…*
- ✓ Click on Config>Controller Dialog. FIFO Chip Sel should be "1" for the AD9230 SPI controller.

► *The FFT plot appears abnormal...*

- ✓ If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce input level if necessary.
- ✓ In VisualAnalog, Click on the Settings button in the "Input Formatter" block. Check that "Number Format" is set to the correct encoding (offset binary by default). Repeat for the other channel.
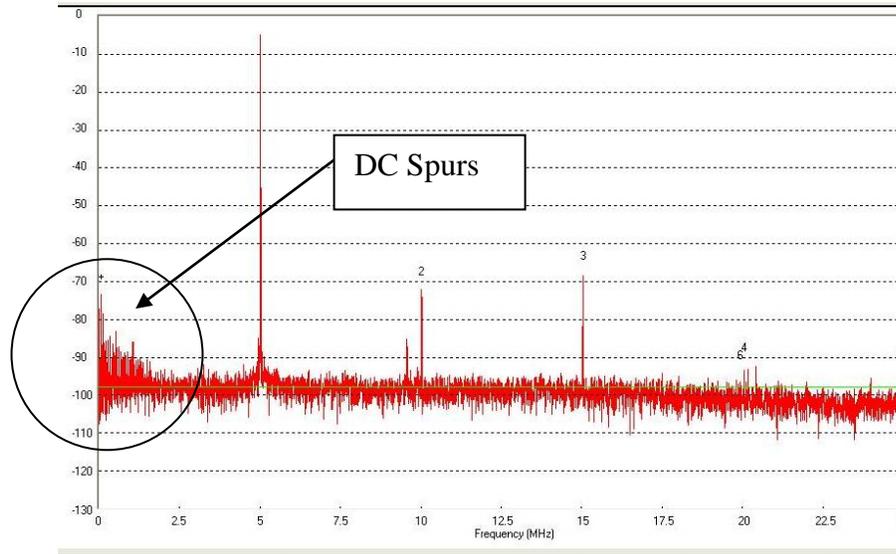- ✓ If DC Spurs appear in the "FFT" plot from VisualAnalog? See Figure 2.

Figure 2: DC Spurs on FFT

Add a ferrite core to ALL switching power supplies used in the evaluation platform, like Digi-Key Part number: 240-2287-ND (M/N: LFB360230-300). See Figure 3.

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Figure 3: Power supply modification to SPU15A-103 switching power supply.

Otherwise, email the HSC Applications Group at highspeed.converters@analog.com and ask for Part Number: EPS060250UH-P5P-SZ, CUI Inc. switching power supply. This switching power supply has a ferrite core built into the DC lead to snub any switching noise.

► *The FFT plot appears normal, but performance is poor.*
  - ✓ Make sure you are using an appropriate filter on the analog input.
  - ✓ Make sure the signal generators for the clock and the analog input are clean (low phase noise).
  - ✓ If you are using non-coherent sampling, change the analog input frequency slightly.
  - ✓ Make sure the SPI config file matches the product being evaluated.

► *The FFT window remains blank after the Run button is clicked.*
  - ✓ Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board
  - ✓ Repeat steps 10 through 16.
  - ✓ Make sure the FPGA has been programmed by verifying that the 'DONE' LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated make sure the U4 switch on the board is in the correct position for USB CONFIG.
  - ✓ Make sure the correct FPGA program was installed.

► *VisualAnalog indicates that the "FIFO capture timed out."*
  - ✓ Make sure all power and USB connections are secure.
  - ✓ Repeat steps 11 through 16.
  - ✓ Probe the DCOA test point on the evaluation board and confirm a clock signal is present at the ADC sampling rate.

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