SPI TIMING CHARACTERISTICS

AVDD1x = 1.65 V, AVSSx[1] = −1.65 V (dual supply operation), AVDD1x = 3.3 V, AVSSx = AGND, AVDD2 − AVSSx = 2.2 V to 3.6 V; IOVDD = 1.8 V to 3.6 V; DGND = 0 V, REFx+/REFx− = 2.5 V (internal/external), MCLK = 8192 kHz; all specifications at T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Description[2]	Test Conditions/Comments	Min	Typ	Max	Unit
t_{12}	SCLK period	50:50			30	MHz
t_{13}	SCLK low time		7			ns
t_{14}	SCLK high time		7			ns
t_{15}	SCLK rising edge to $\overline{CS}$ falling edge		10			ns
t_{16}	$\overline{CS}$ falling edge to SCLK rising edge		10			ns
t_{17}	SCLK rising edge to $\overline{CS}$ rising edge		10			ns
t_{18}	$\overline{CS}$ rising edge to SCLK rising edge		10			ns
t_{19}	Minimum $\overline{CS}$ high time		10			ns
t_{20}	SDI setup time		5			ns
t_{21}	SDI hold time		5			ns
t_{22A}	$\overline{CS}$ falling edge to SDO enable (SPI = Mode 0)				30	ns
t_{22B}	SCLK falling edge to SDO enable (SPI = Mode 3)				49	ns
t_{23}	SDO setup time		10			ns
t_{24}	SDO hold time		10			ns
t_{25}	$\overline{CS}$ rising edge to SDO disable				30	ns

[1] AVSSx refers to the following pins: AVSS1A, AVSS1B, AVSS2A, AVSS2B, AVSS3, and AVSS4. This term is used throughout the data sheet.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

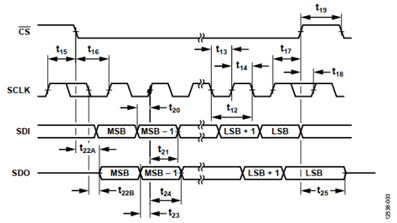


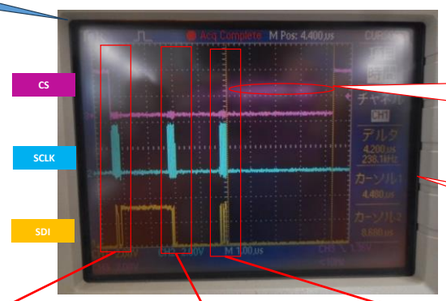
Figure 3. SPI Control Interface Timing Diagram

Waveform of writting to SRC_N_LSB(0x061)

	R/W	Address	Write Data	CRC
	1bit	7bits	8bits	8bits
Send data frame size	8bits		8bits	8bits
Total Send Data size	24bits			

send data

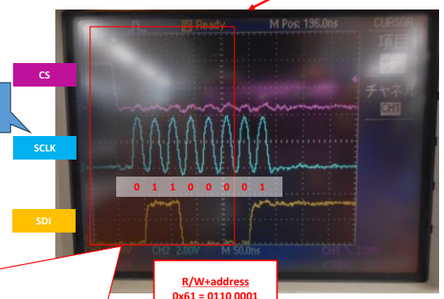
R/W+Address	Write Data	CRC
0x61	0xC8	0x96



t17(SCLK rising edge to CS rising edge)
Spec 10ns
Actual 4.2us

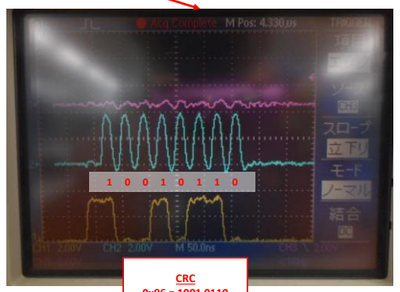
The process flow I previously explained did not include this, but in reality, we consecutively perform both writing and reading data to and from a single register to confirm that the data has been written correctly.

The SCLK waveform is distorted, but this is due to the performance of the

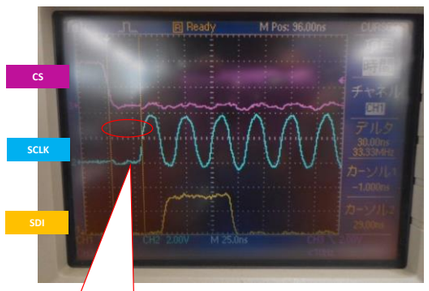


R/W+address
0x61 = 0110 0001

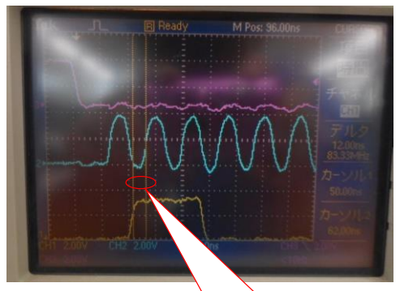
WriteData
0xC8 = 1100 1000



CRC
0x96 = 1001 0110



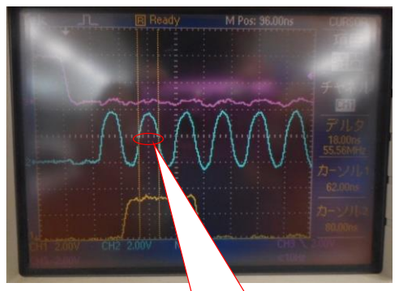
t16(CS falling edge to SCLK rising edge)
Spec 10ns(min)
Actual 30ns



t20(SDI setup time)
Spec 5ns(min)
Actual 12ns

t21(SDI hold time)
Spec 5ns
Actal 21ns

t13(SCLK low time)
Spec 7ns
Actual 16ns



t14(SCLK high time)
SPEC 7ns
Actual 18ns