AD916x MCS Procedure

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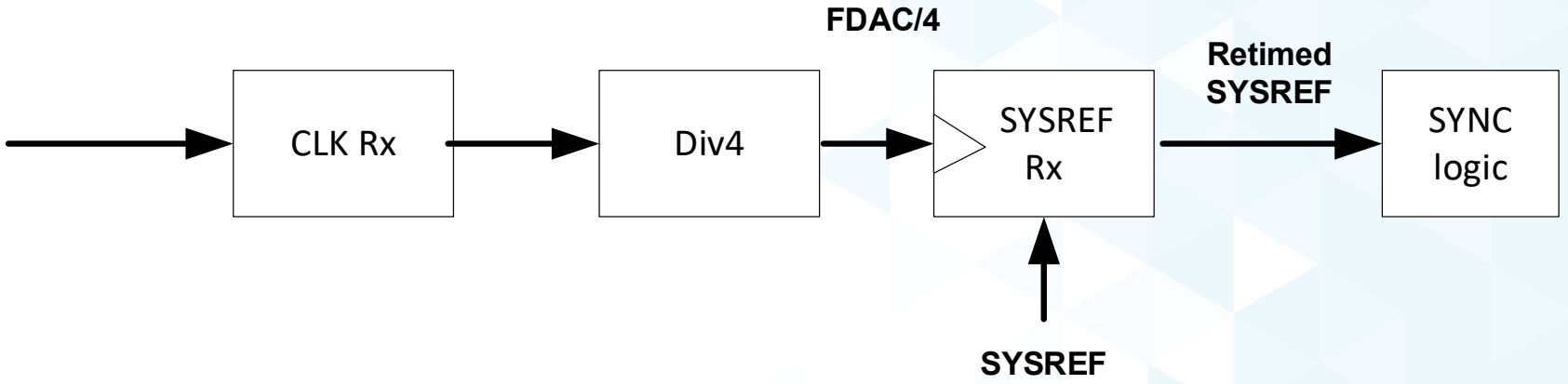
AHEAD OF WHAT'S POSSIBLE™

Sysref Receiver Diagram



AD916x MCS Procedure

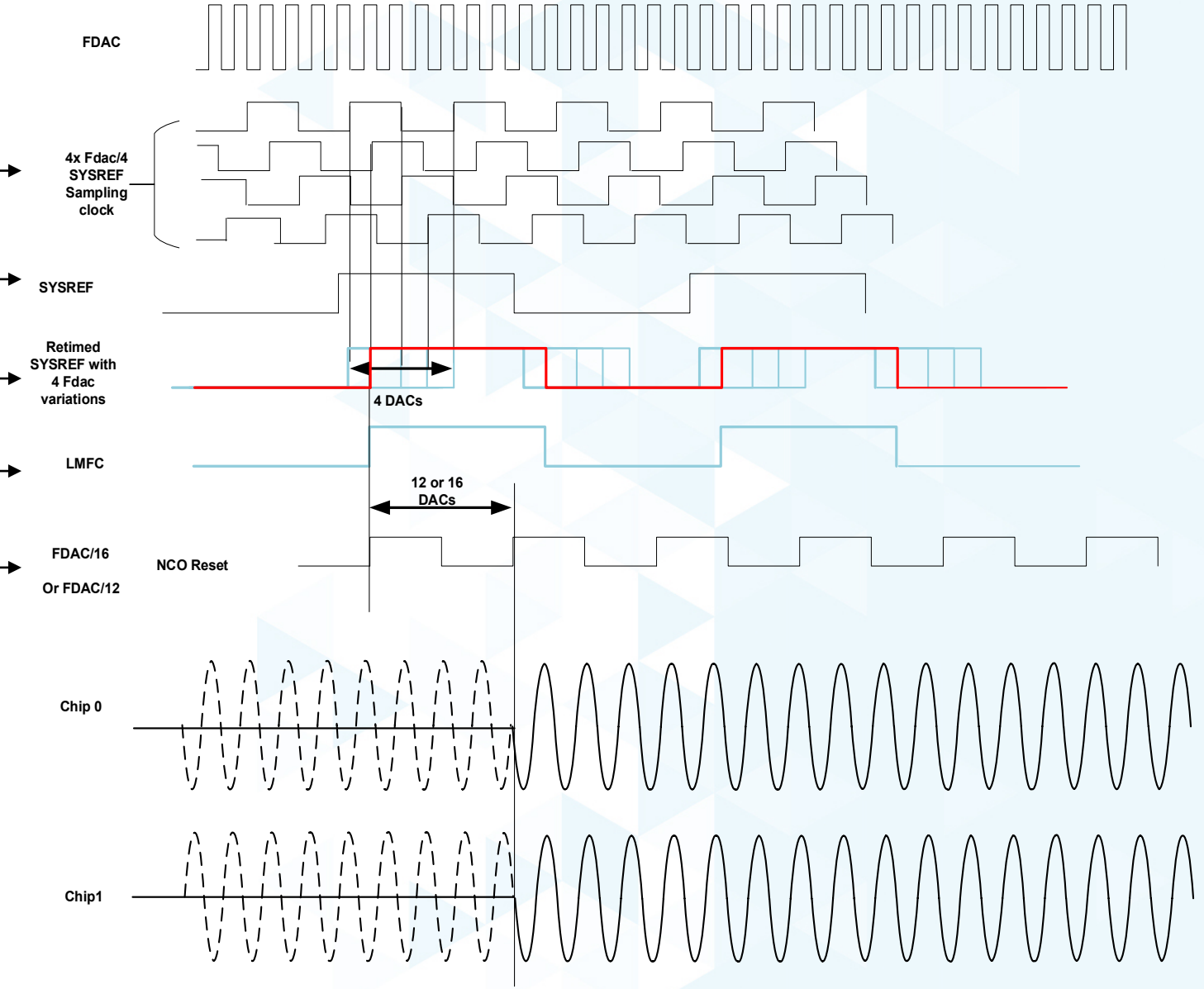
4 Random phases due to DIV4 divider

SYSREF should meet Setup/hold timing

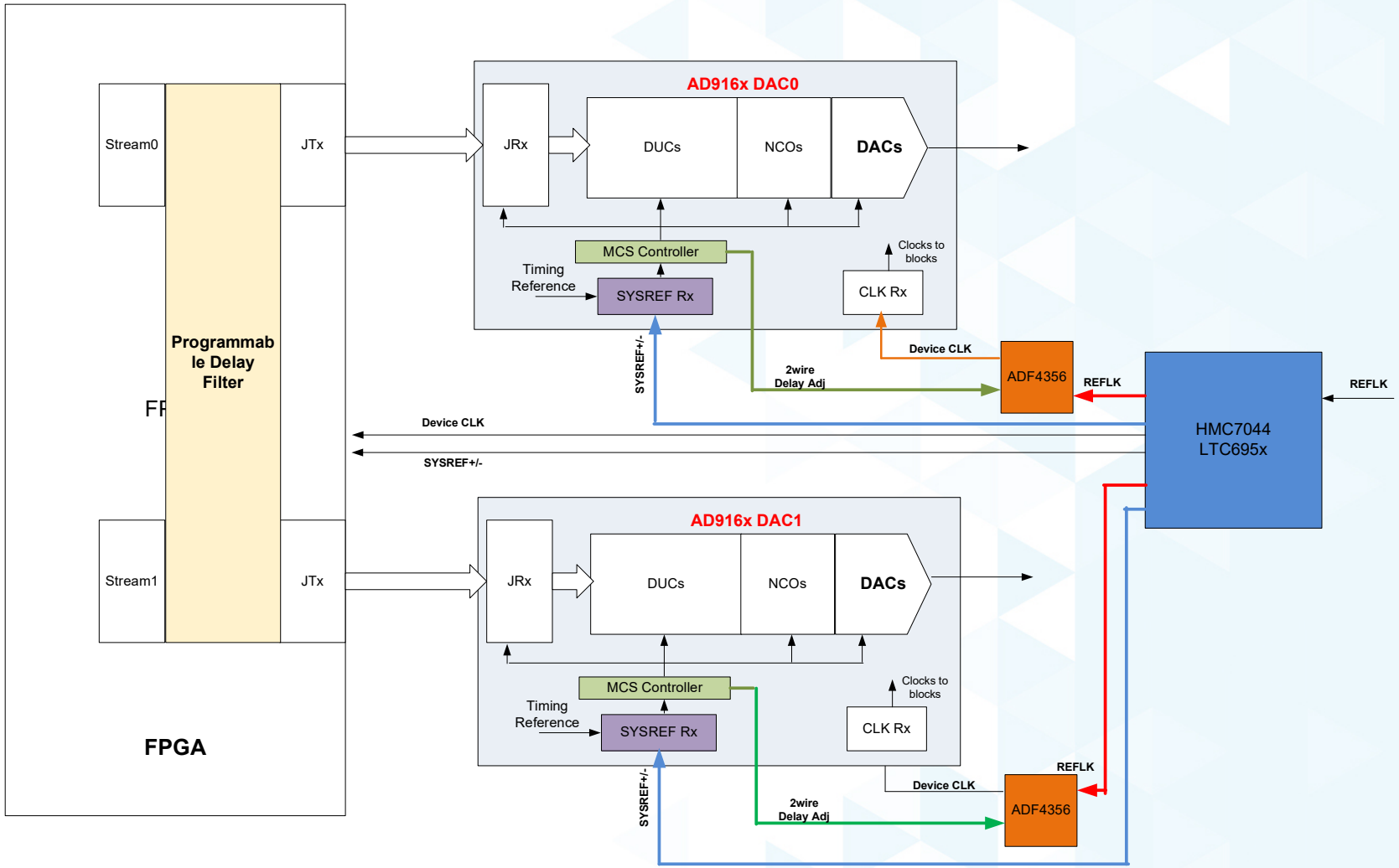
Retimed SYSREF

LFMC aligned to Retimed SYSREF

FDAC/16 for 2x, 4x, 8x…
FDAC/12 for 3x, 6x, 12x



Clock Distribution



One SYSREF Pulse to Synchronize the System

- SYSREF shall be DC-coupling
- SYSREF pulses shall arrive at the pins simultaneously across multiple chips.
- Readback SYSREF phase. The reg0x37[7:4] SPI readbacks are 0b0000, 0b1000m 0b1100 and 0b1110. these represent 4 phases.
  - Use phase 0 as the base
  - Get the delta of all the chips referring to phase 0.
- Then use FPGA programable Delay Filter to compensate the offset

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Multiple Pulses to Synchronize the System

- Use phase 0 as baseline
- Toggle the clock or reboot the chip to reset the DIV4 divider, then readback sysref phase
  - If phase 0, move on.
  - Else repeat the process.
- If the NCO frequency is integer multiple of LMFC, stop here. All the chips should be already synchronized.
- If the NCO isn't the integer multiple of LMFC, issue one extra SYSREF pulse.
  - The extra SYSREF pulses shall arrive at chips simultaneously.