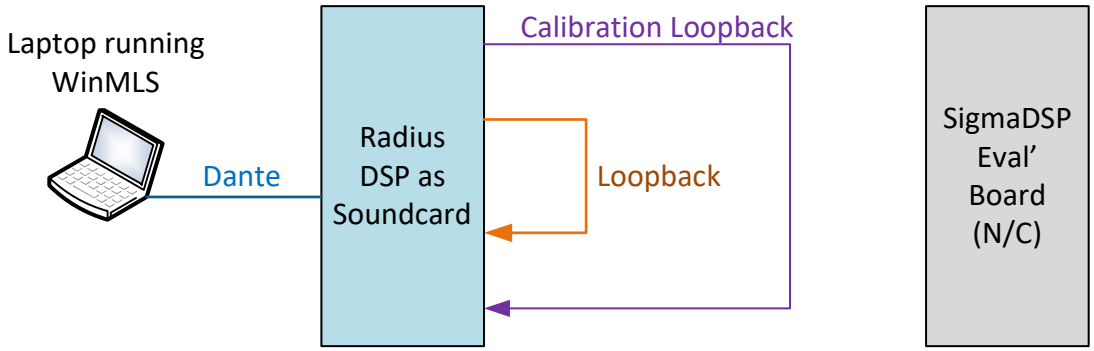
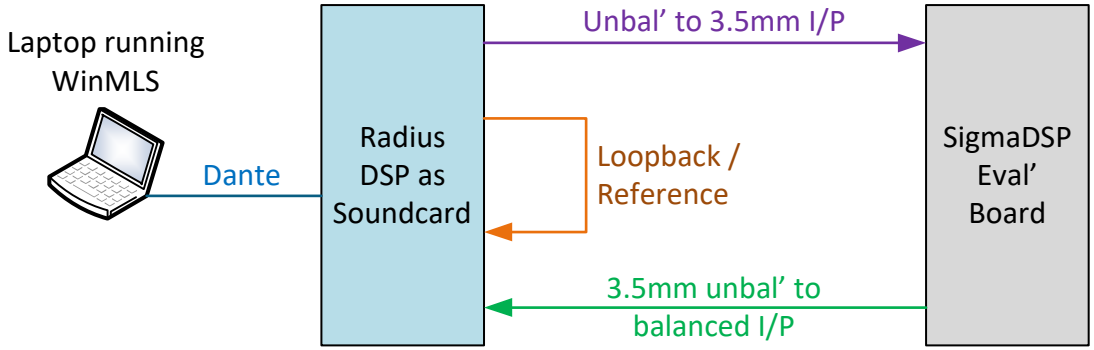
STEP #1



Output of this process results in calibrated input and output levels.

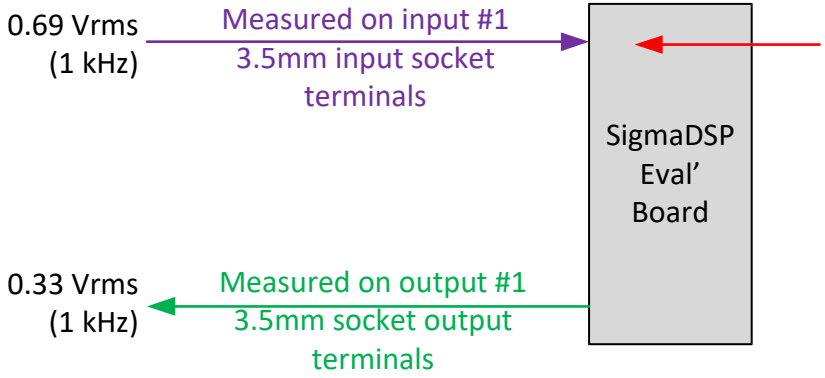
STEP #2



NOTES:

- WinMLS output level set to -24 dBFS to achieve 0.69Vrms input to SigmaDSP 3.5mm input socket
- Input & Output metering inside SigmaDSP was -12dB (scale TBC)

STEP #2 Observations



NOTE: ~1.42 Vrms (1 kHz) measured on test points ADC1LP and ADC1LN