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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# ADAU1467

## SigmaDSP Audio Processor

D

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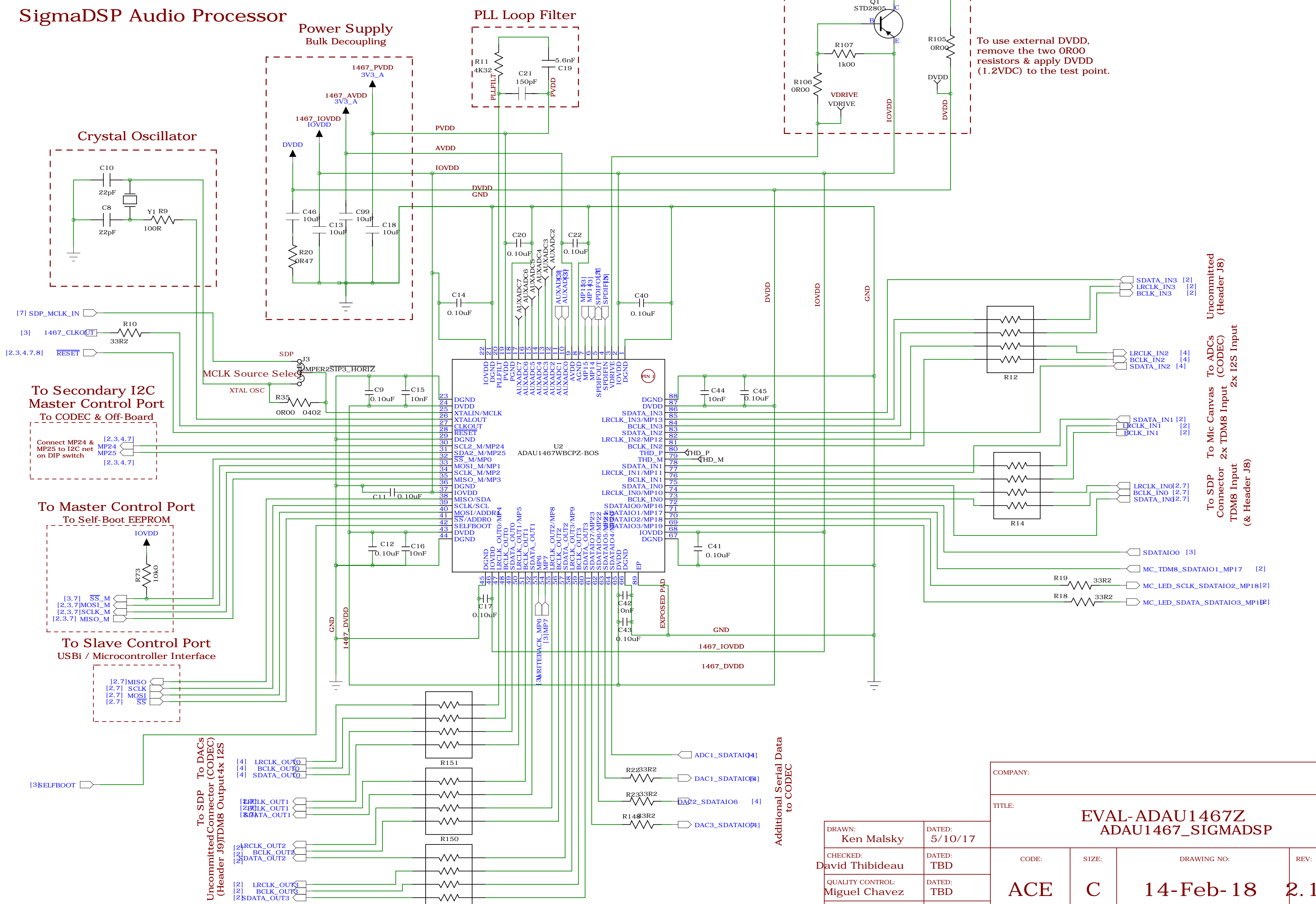
C

B

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A

A



To use external DVDD, remove the two 0R00 resistors & apply DVDD (1.2VDC) to the test point.

To Mic Canvas To ADCs (CODEC) 2x I2S Input (& Header J8)

To SDP Connector 2x TDM8 Input TDM8 Input (& Header J8)

Additional Serial Data to CODEC

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: <b>EVAL-ADAU1467Z</b> <b>ADAU1467_SIGMADSP</b>			
CODE:	SIZE:	DRAWING NO:	REV:
<b>ACE</b>	<b>C</b>	<b>14-Feb-18</b>	<b>2.1</b>
SCALE:			SHEET: 1 8

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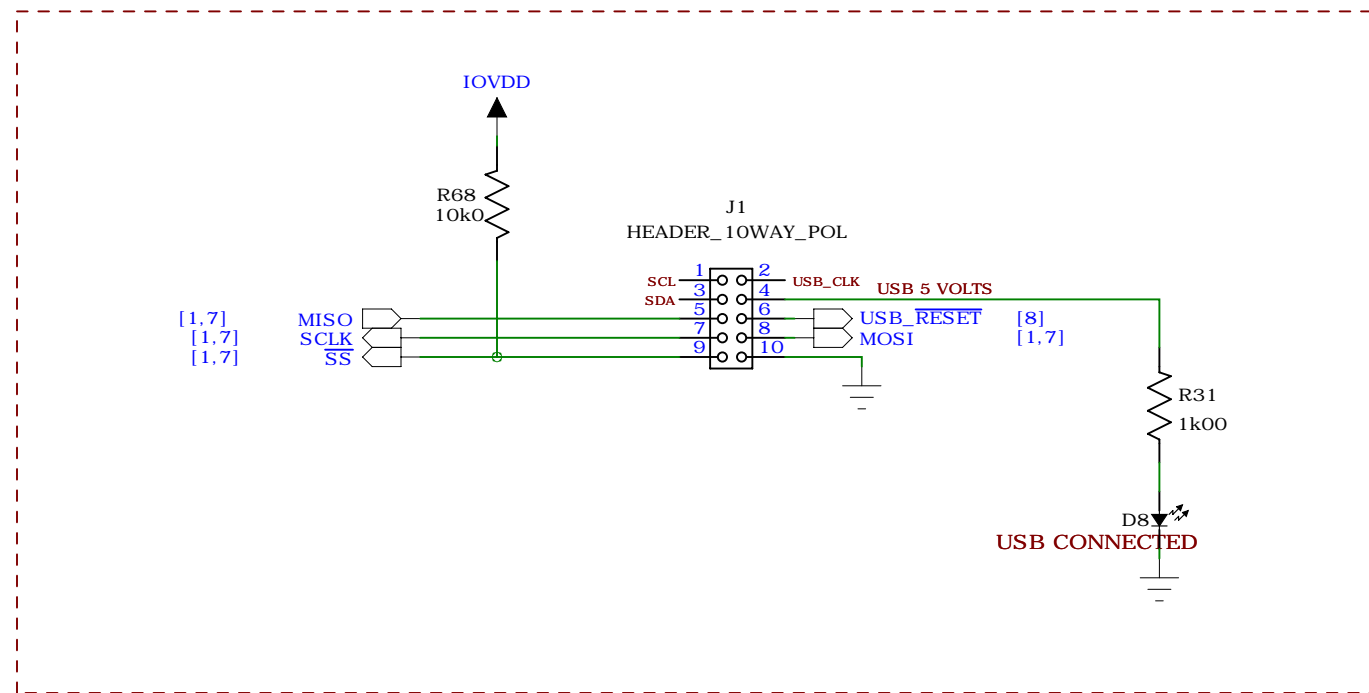
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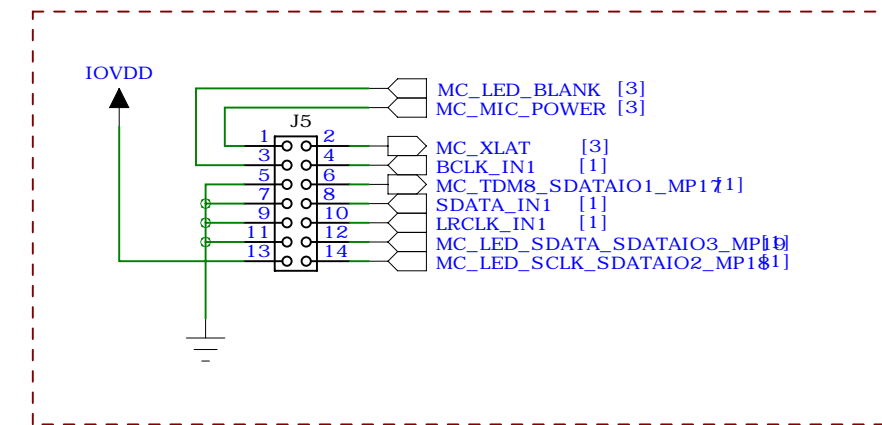
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

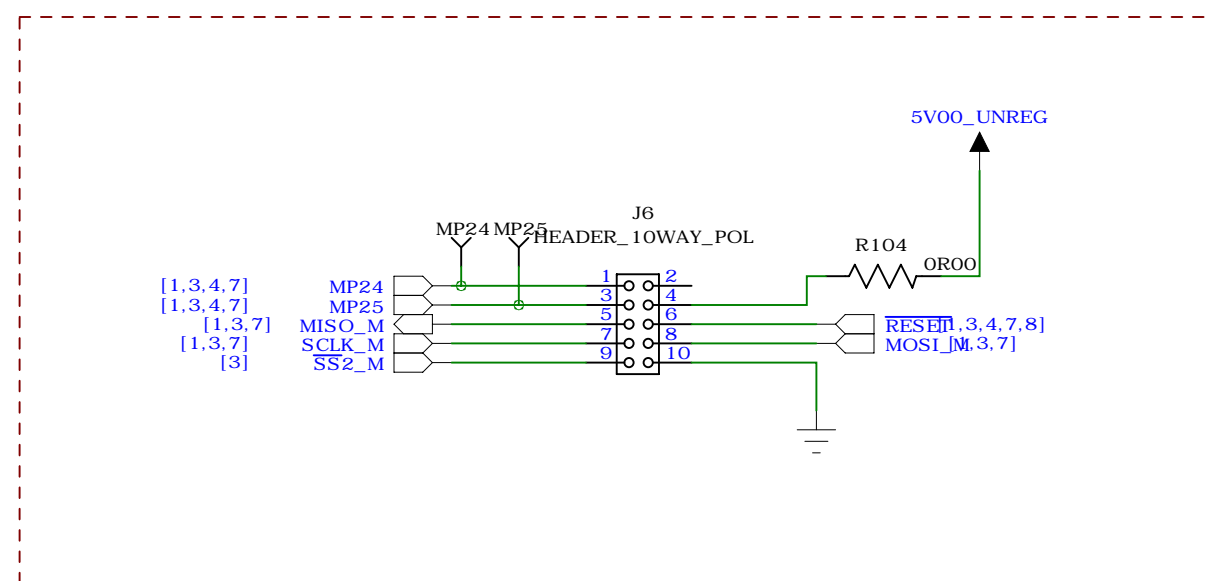
**Control Input Port Header (USBi)**  
(DSP Programming/Control Interface)



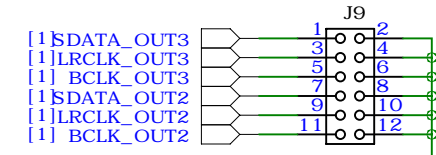
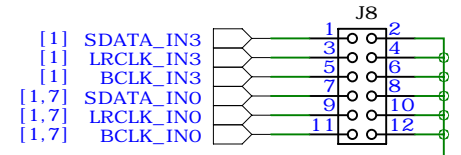
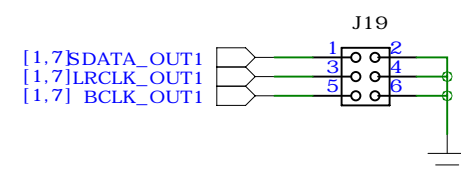
**Mic Canvas Header**



**Control Output Port Header**  
(DSP Interface to Peripherals)



**Uncommitted Serial Ports**  
(for user peripherals)



COMPANY:

TITLE:  
**EVAL-ADAU1467Z**

DRAWN: <b>Ken Malsky</b>	DATED: <b>5/10/17</b>
CHECKED: <b>David Thibideau</b>	DATED: <b>TBD</b>
QUALITY CONTROL: <b>Miguel Chavez</b>	DATED: <b>TBD</b>
RELEASED: <b>Ken Malsky</b>	DATED: <b>TBD</b>

CODE: <b>ACE</b>	SIZE: <b>C</b>	DRAWING NO: <b>14-Feb-18</b>	REV: <b>2.1</b>
SCALE:			SHEET <b>2</b> of <b>8</b>

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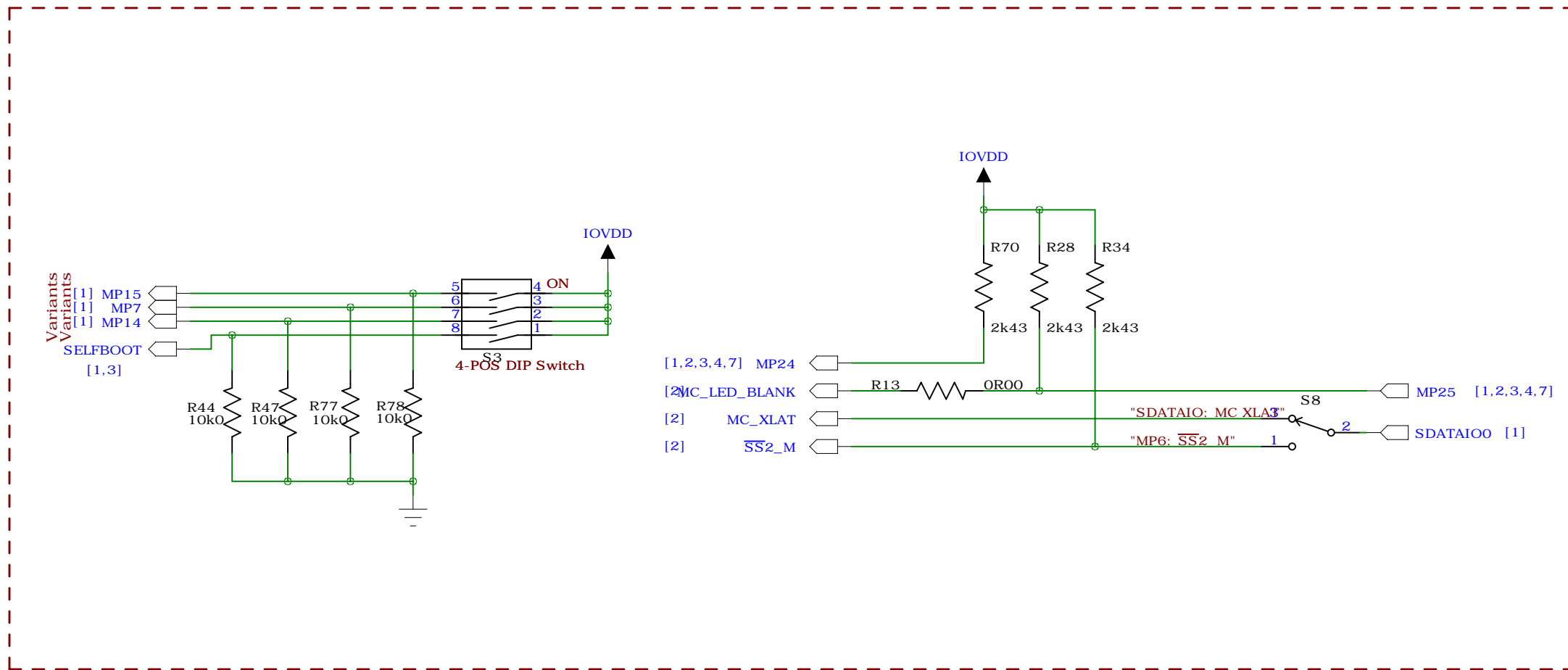
3

2

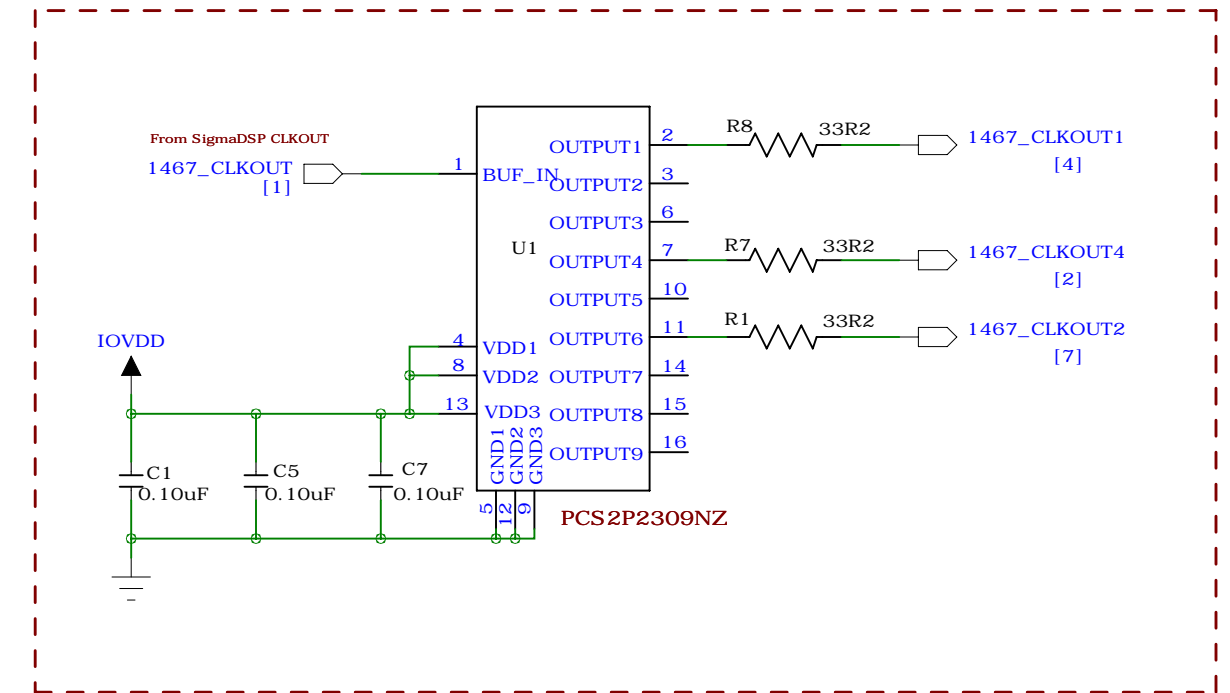
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

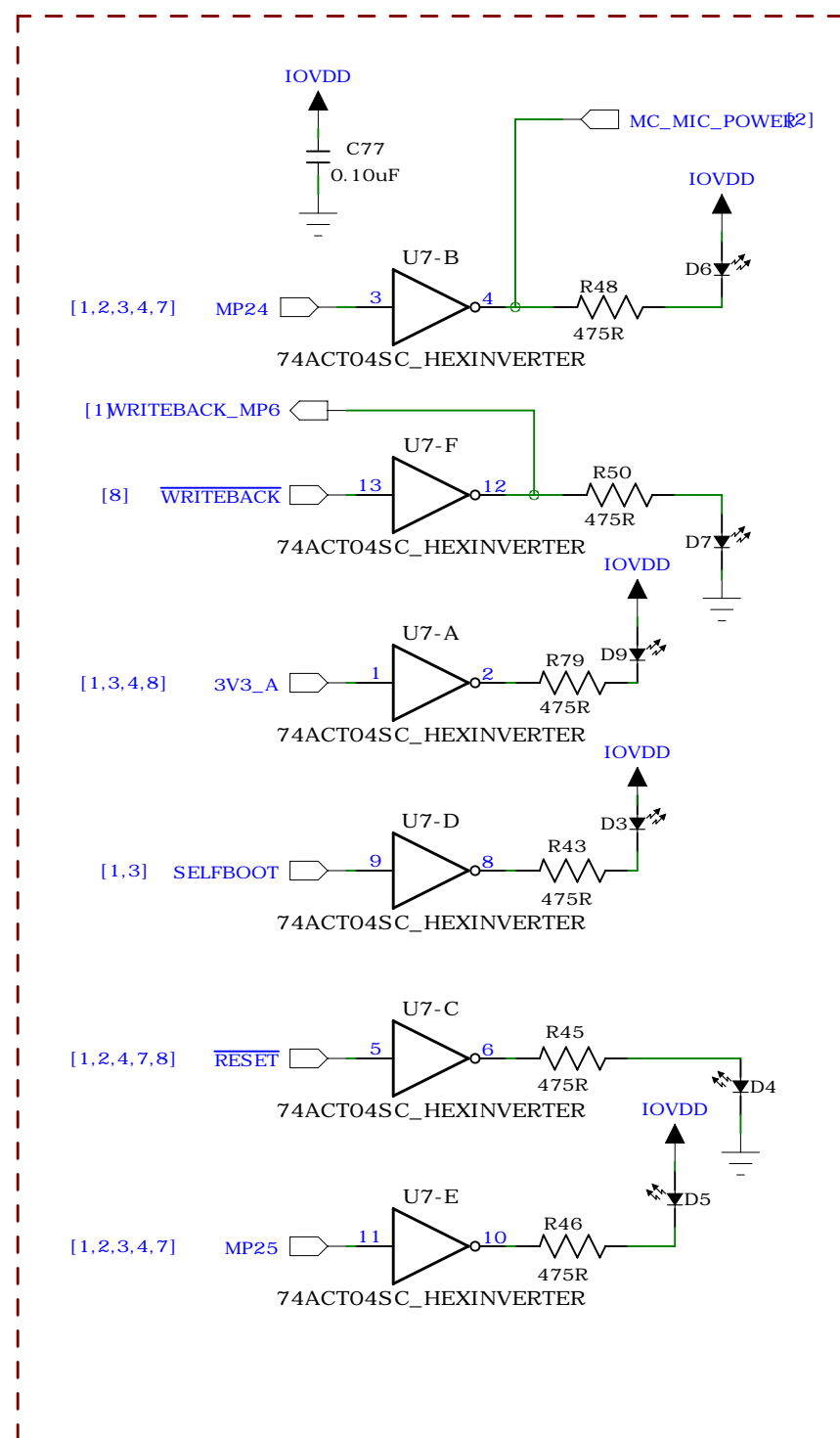
### Configuration Options



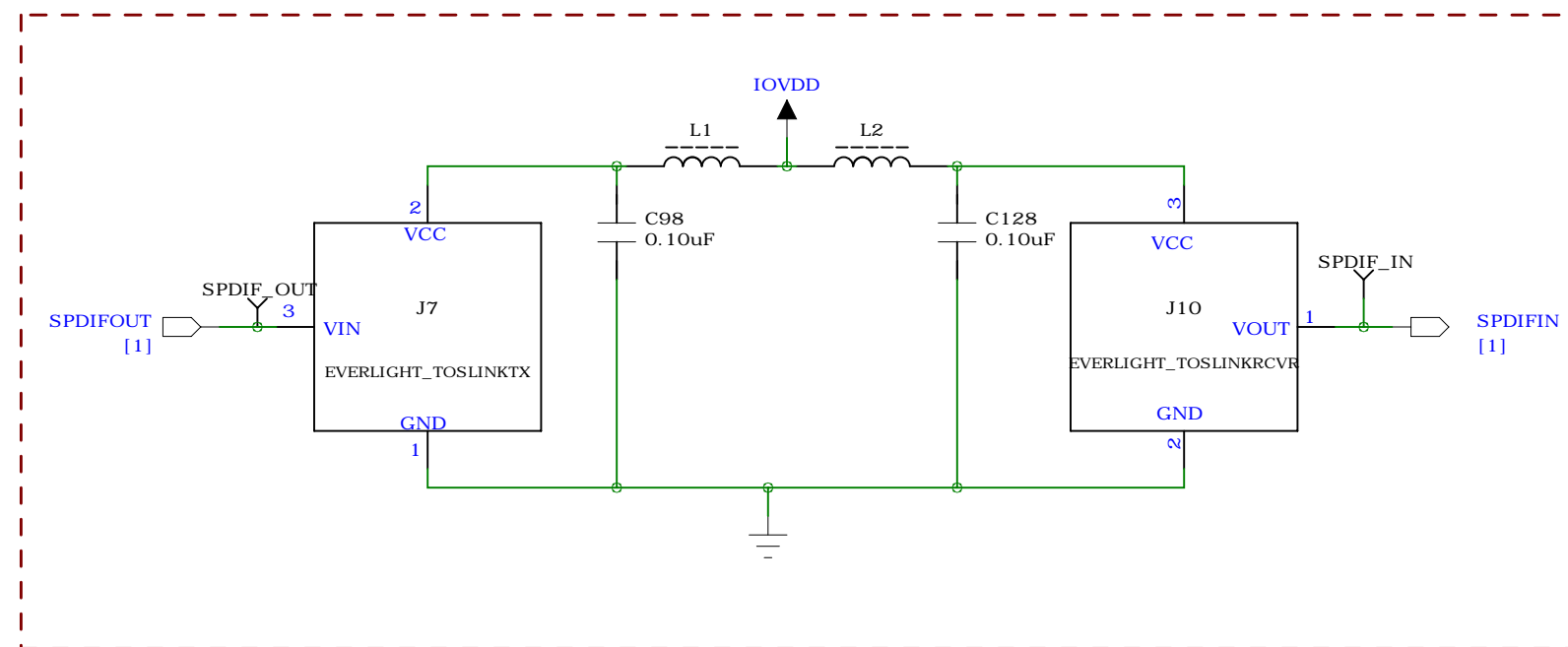
### Clock Distribution



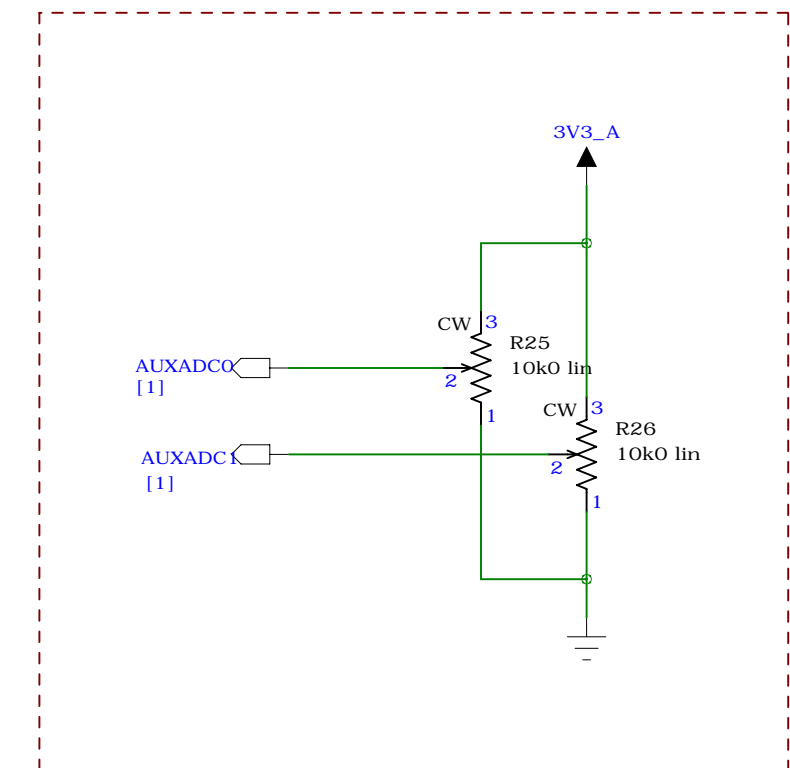
### Status LEDs



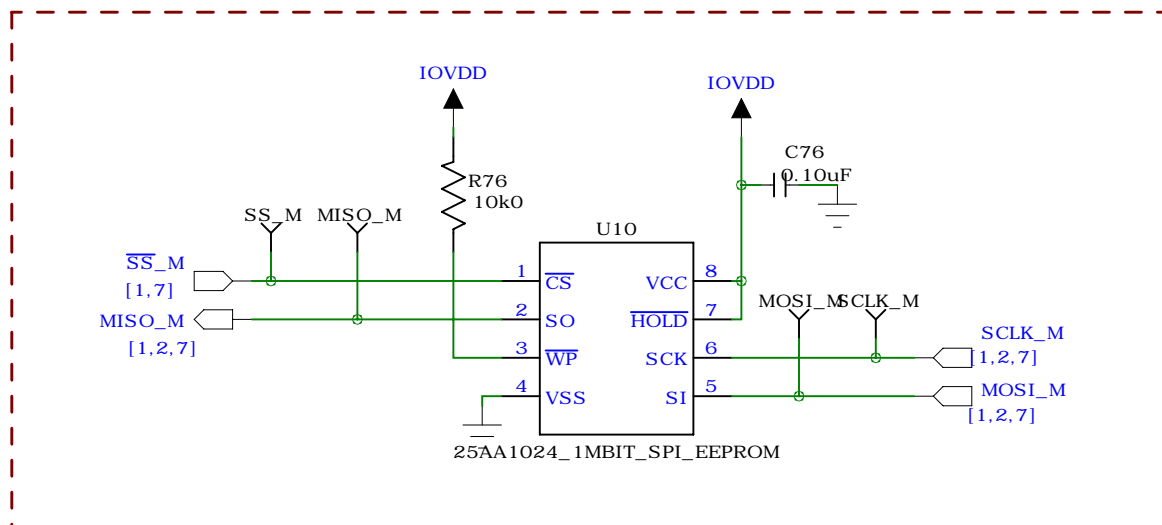
### S/PDIF TOSLINK Optical Connectors



### AUXADC Input



### Self-Boot Memory



DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: <b>EVAL-ADAU1467Z DSP_PERIPHERALS</b>			
CODE: <b>ACE</b>	SIZE: <b>C</b>	DRAWING NO: <b>14-Feb-18</b>	REV: <b>2.1</b>
SCALE:			SHEET 3 8

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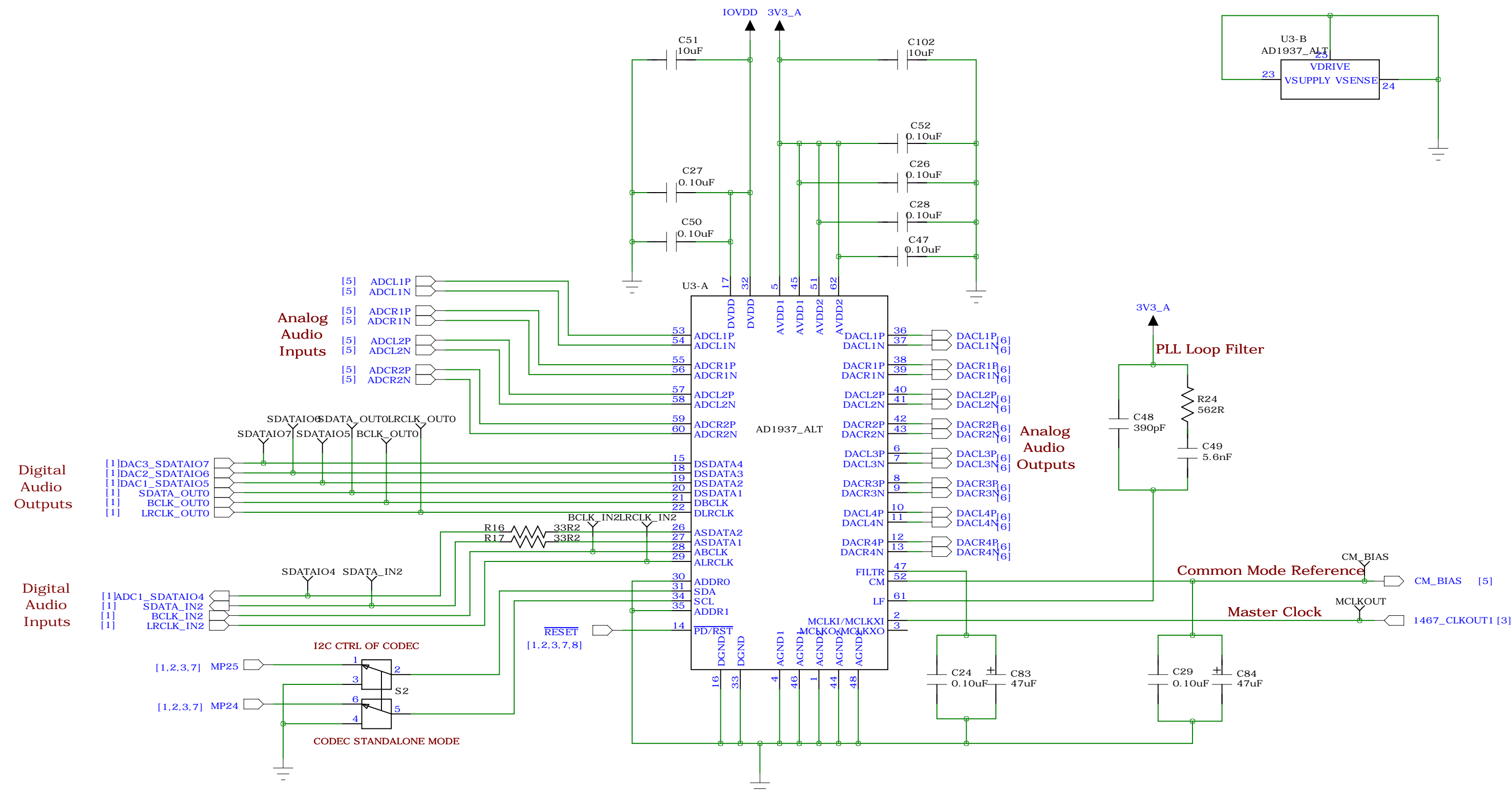
2

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# AD1937

## 4xADC 8xDAC Audio CODEC



COMPANY:			
TITLE: EVAL-ADAU1467Z AD1937_CODEC			
CODE:	SIZE:	DRAWING NO:	REV:
ACE	C	14-Feb-18	2.1
SCALE:			SHEET 4 8

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

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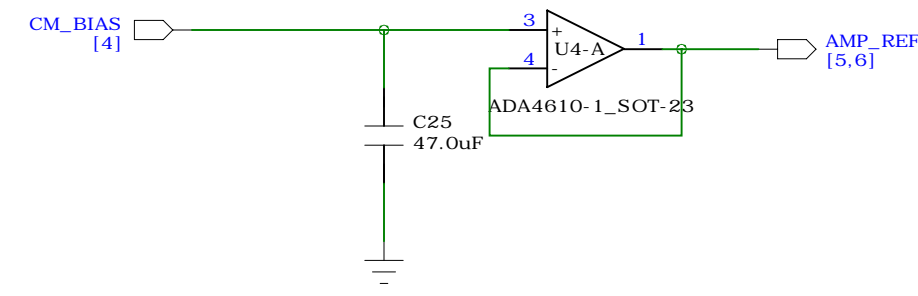
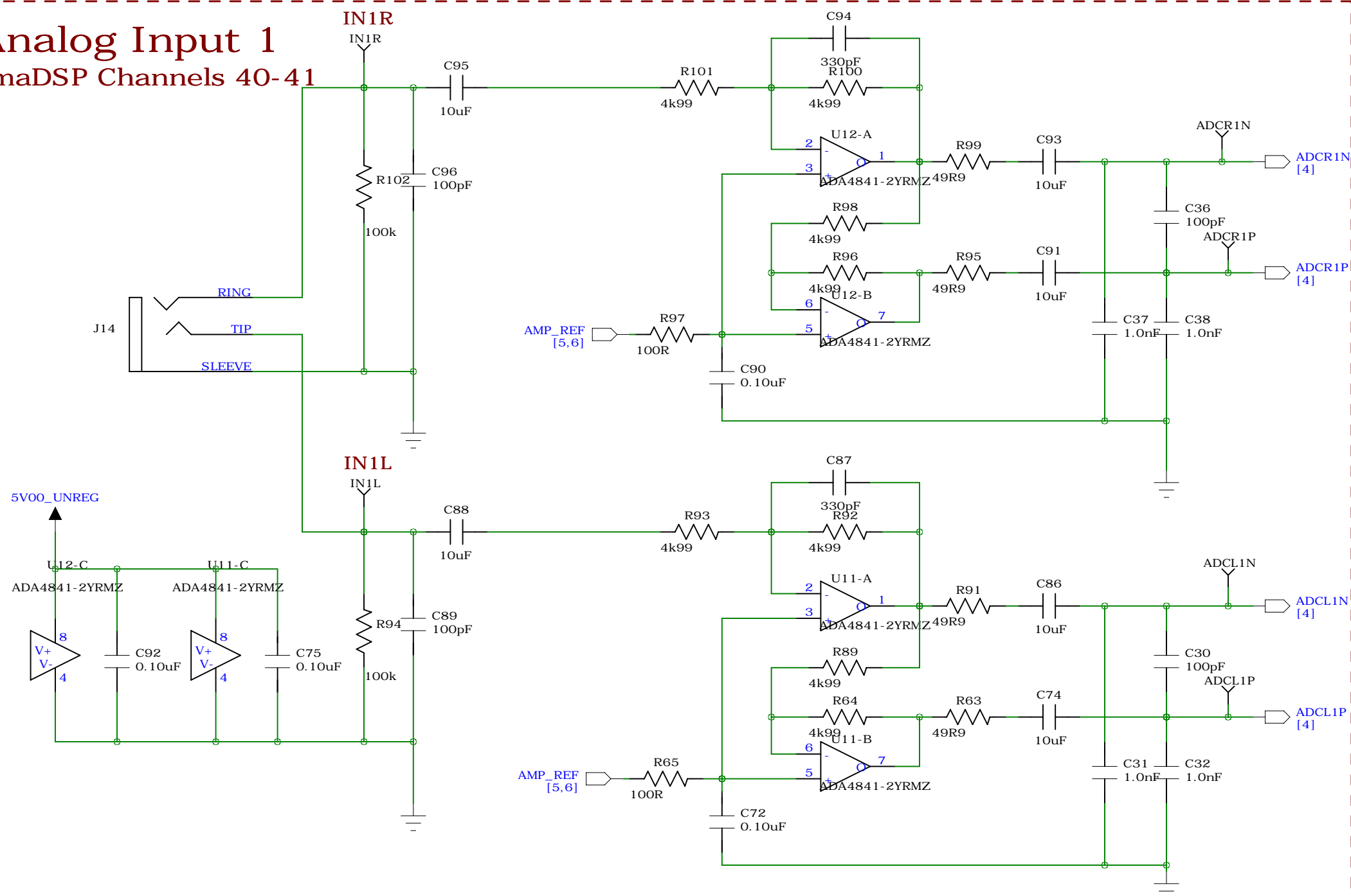
3

2

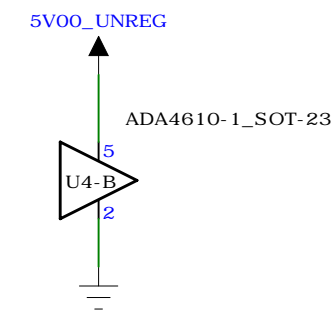
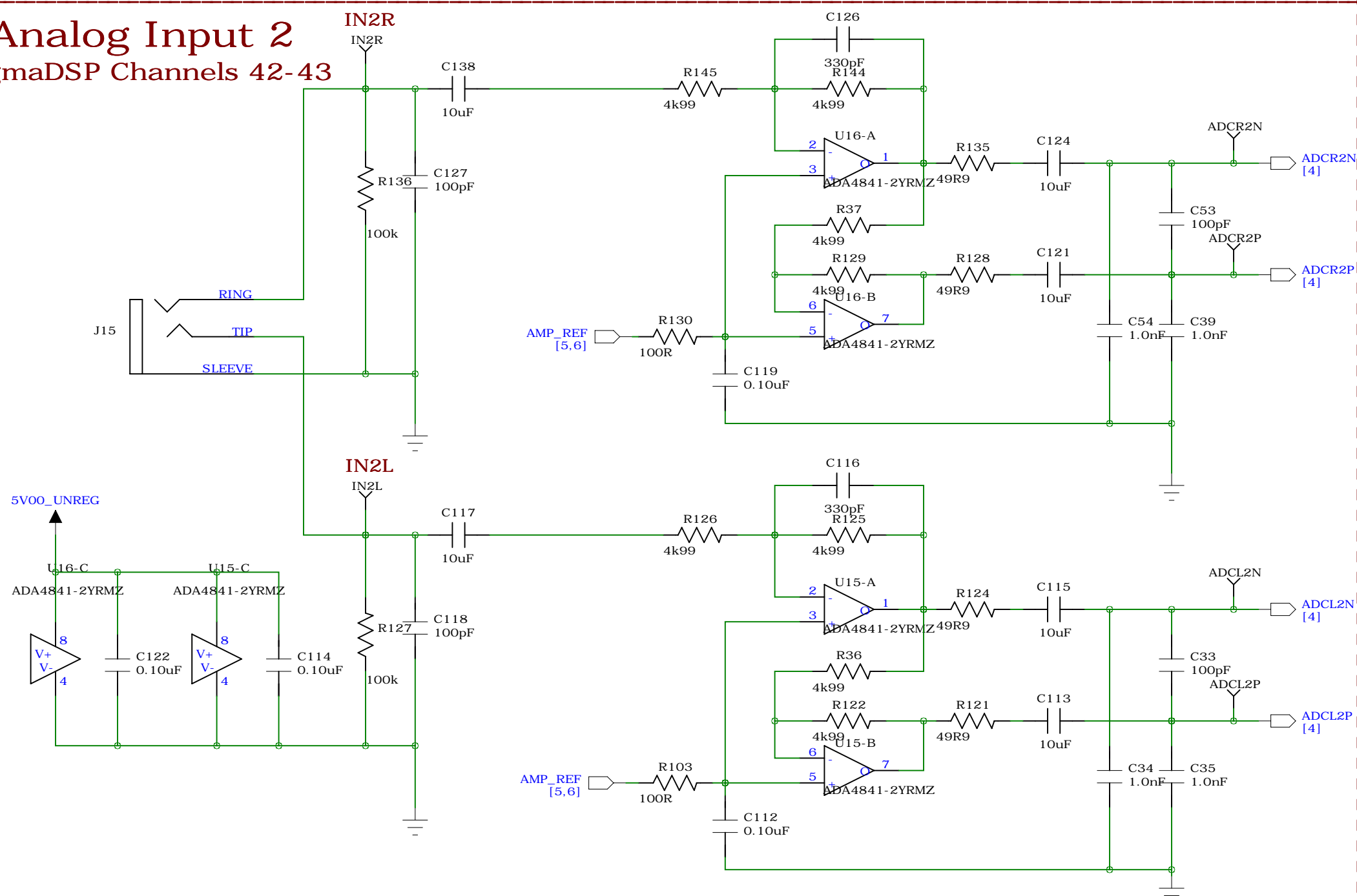
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

### Analog Input 1 SigmaDSP Channels 40-41



### Analog Input 2 SigmaDSP Channels 42-43



DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: <b>EVAL-ADAU1467Z ADC_BUFFERS</b>			
CODE: <b>ACE</b>	SIZE: <b>C</b>	DRAWING NO: <b>14-Feb-18</b>	REV: <b>2.1</b>
SCALE:			SHEET 5 of 8



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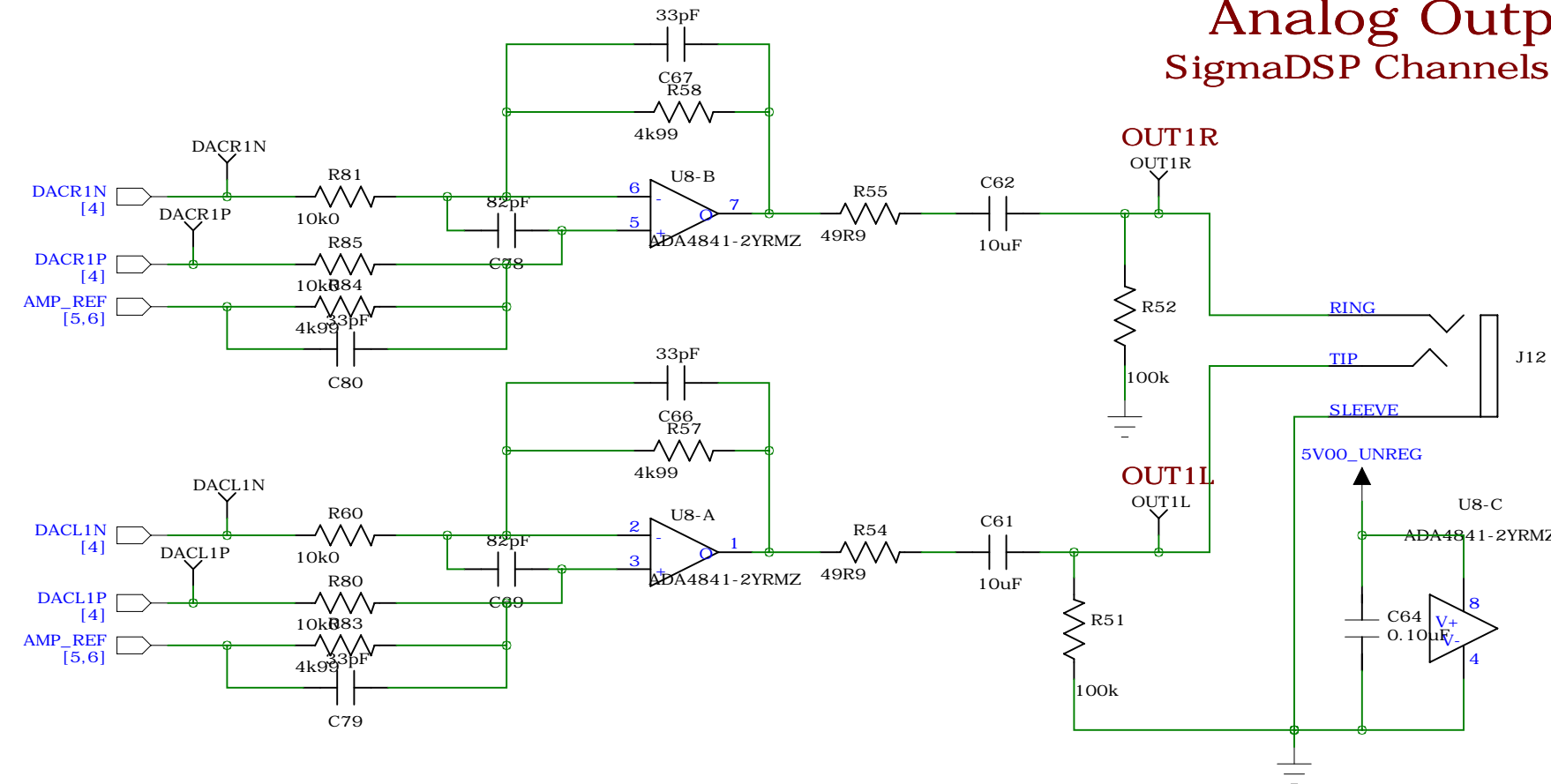
2

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

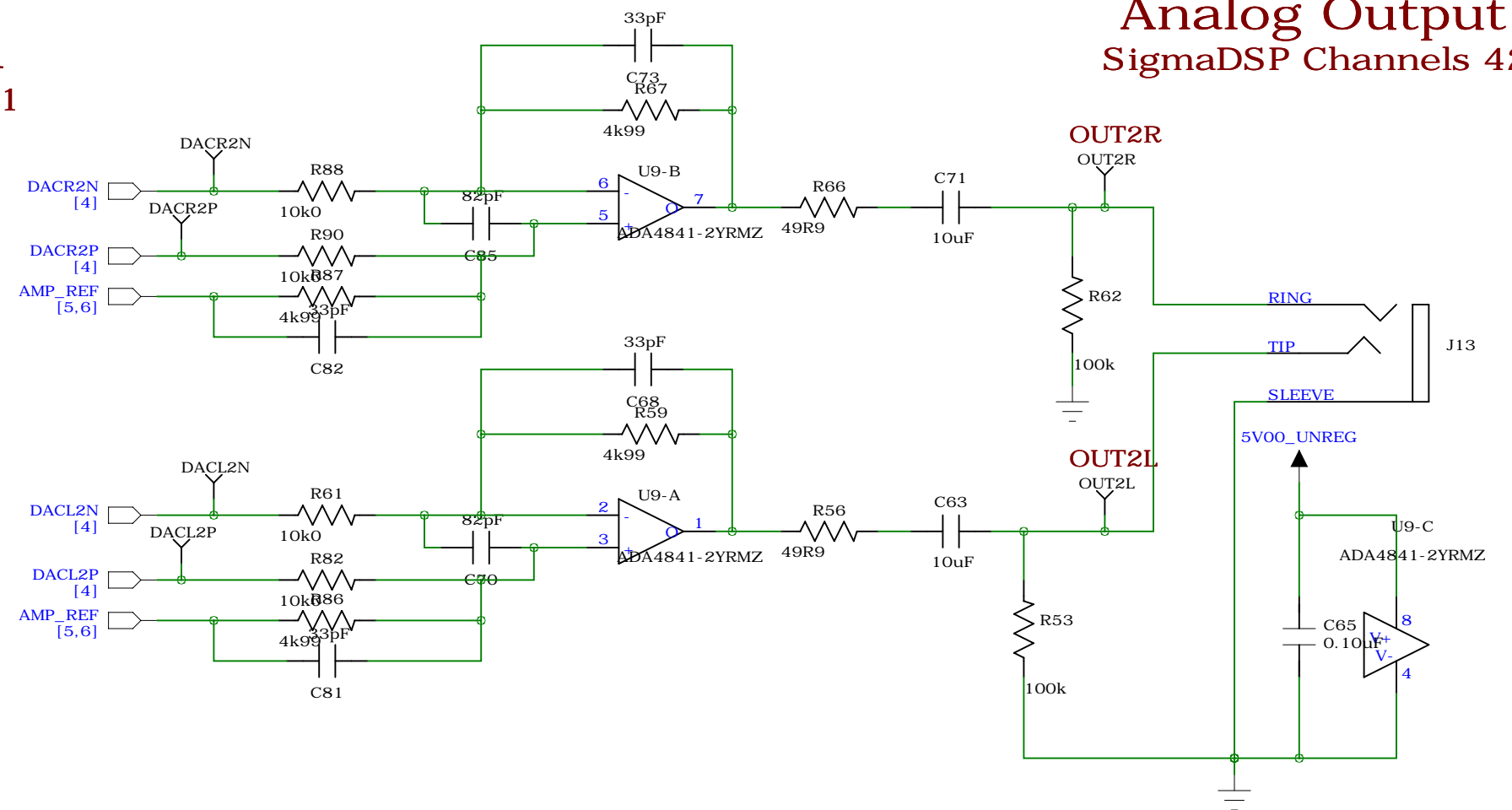
D

### Analog Output 1 SigmaDSP Channels 40-41



C

### Analog Output 2 SigmaDSP Channels 42-43

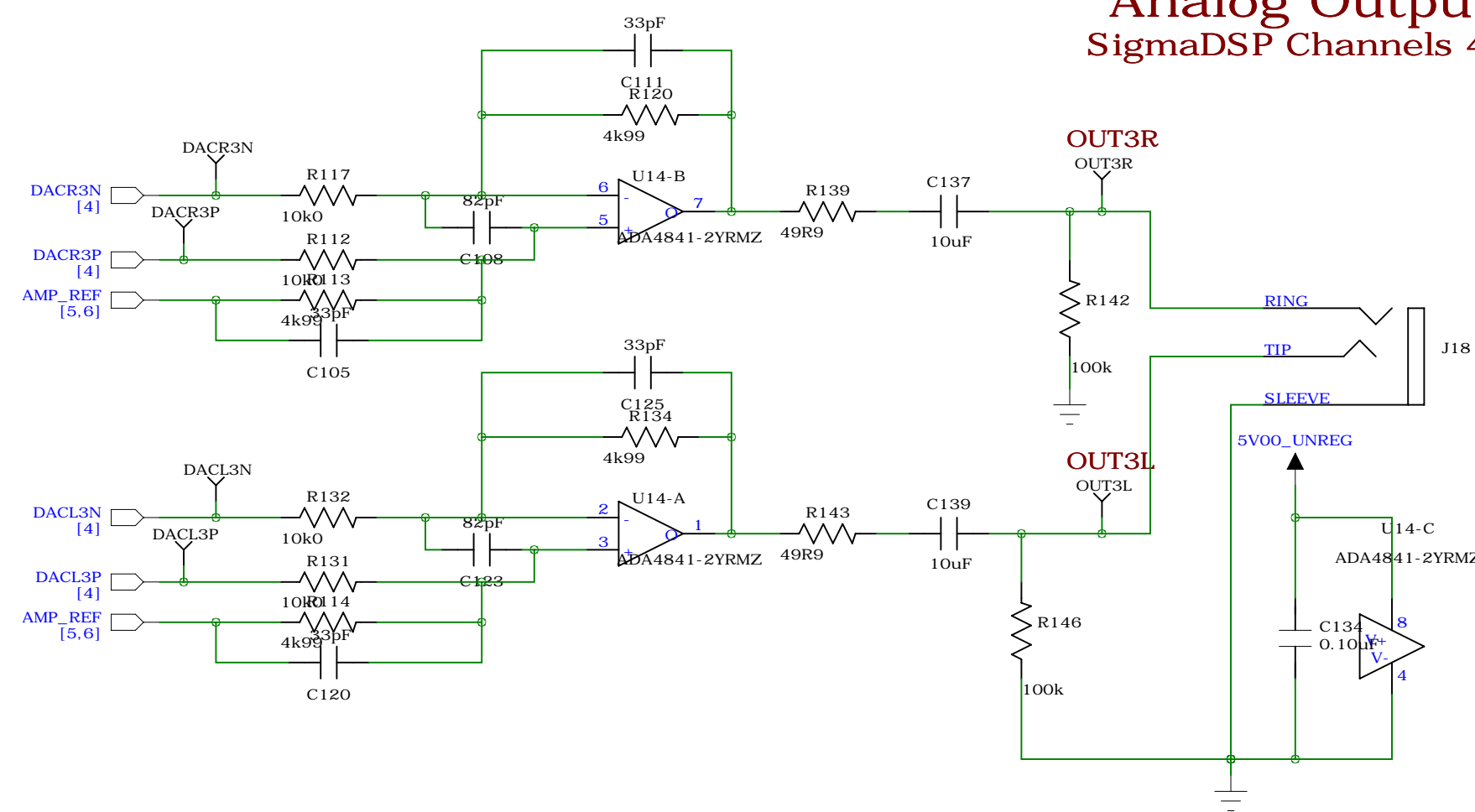


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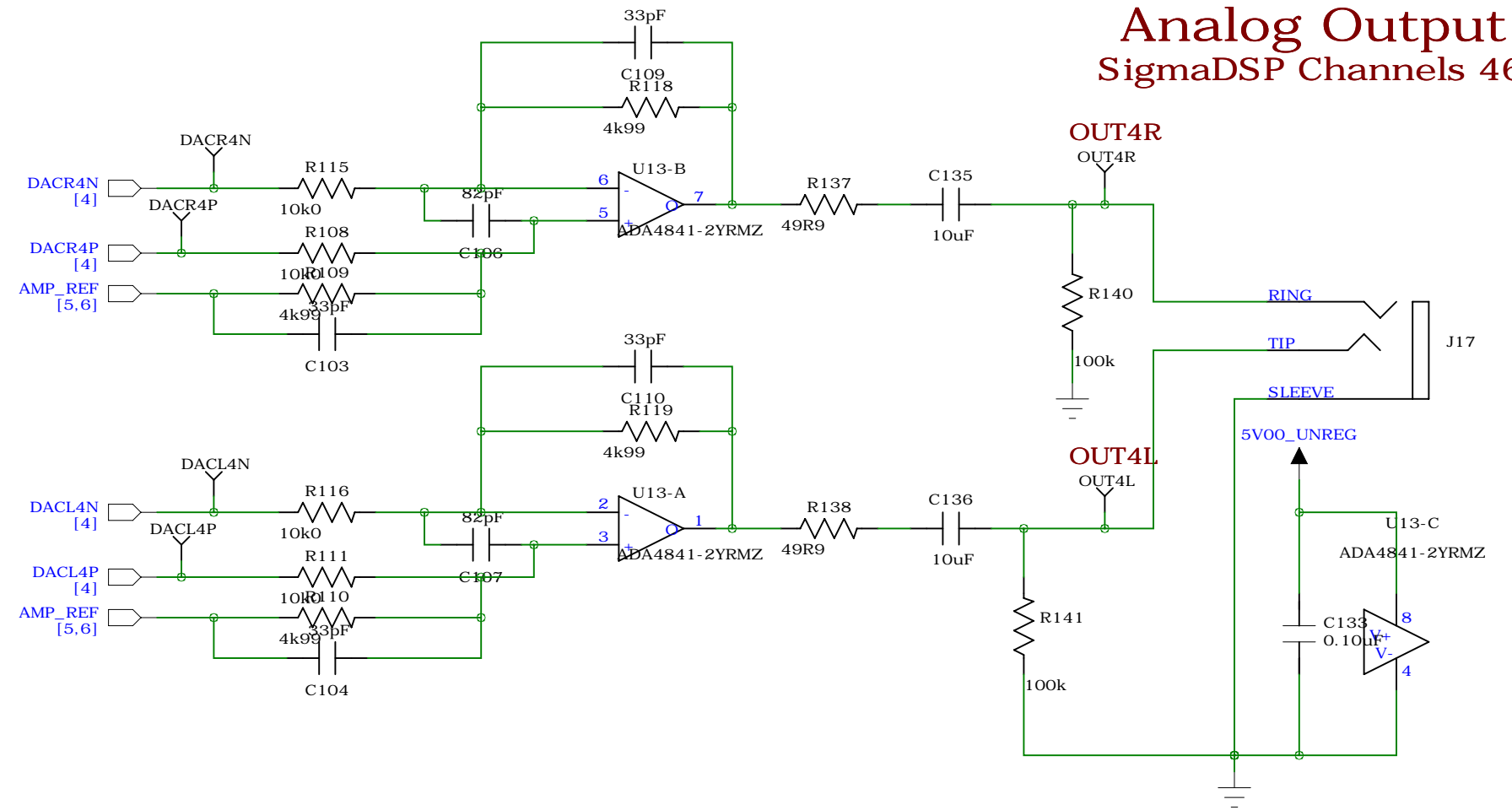
B

### Analog Output 3 SigmaDSP Channels 44-45



A

### Analog Output 4 SigmaDSP Channels 46-47



B

A

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: <b>EVAL-ADAU1467Z DAC_BUFFERS</b>			
CODE: <b>ACE</b>	SIZE: <b>C</b>	DRAWING NO: <b>14-Feb-18</b>	REV: <b>2.1</b>
SCALE:			SHEET <b>6</b> of <b>8</b>

6

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

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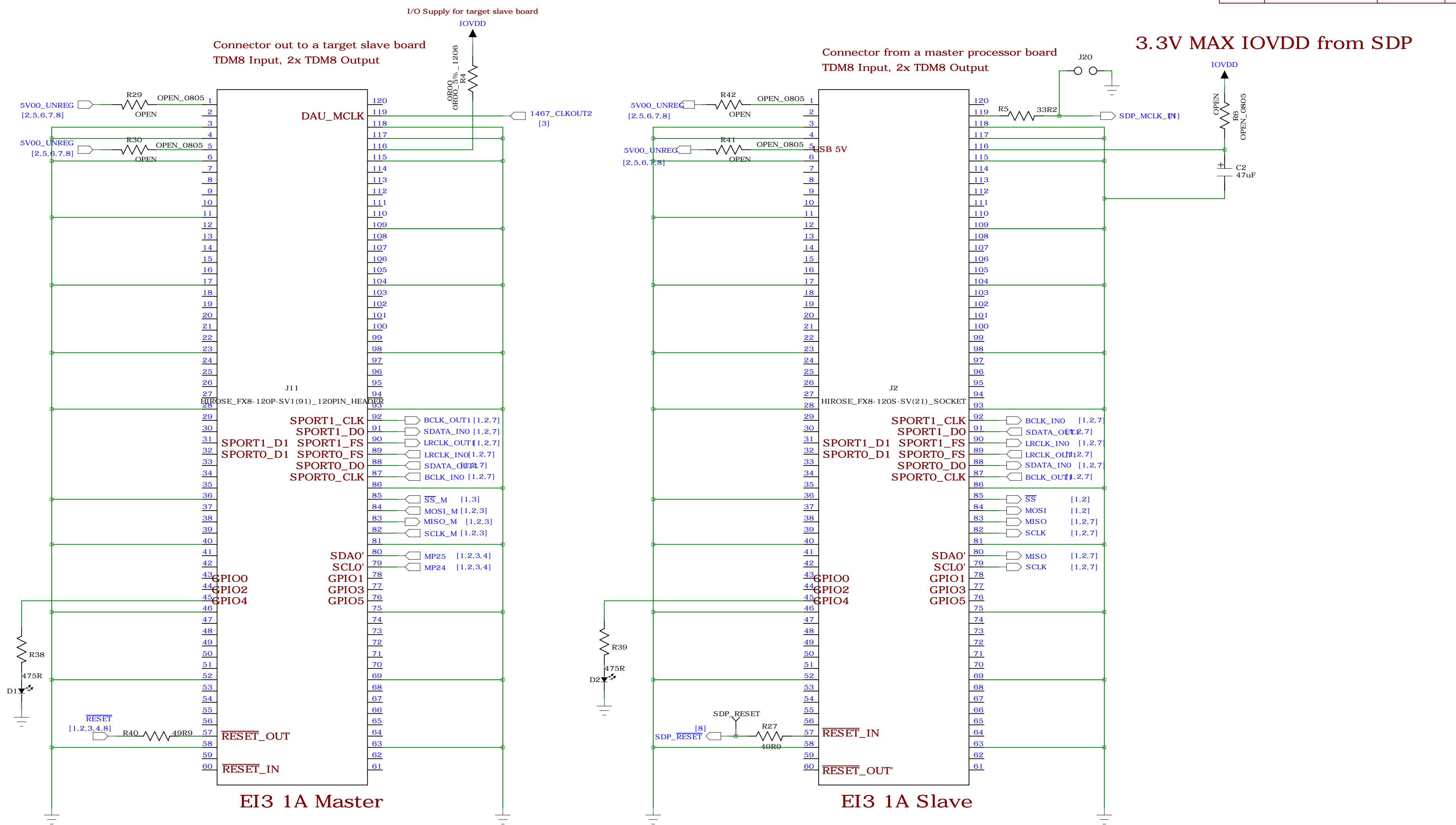
A

D

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A



BCLK\_IN0 [1,2,7] R2 OPEN BCLK\_OUT1 [1,2,7] R3 OPEN LRCLK\_IN0 [1,2,7] R4 OPEN LRCLK\_OUT1 [1,2,7]

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: <b>EVAL-ADAU1467Z</b> <b>SDP_INTERFACE</b>			
CODE:	SIZE:	DRAWING NO:	REV:
<b>ACE</b>	<b>EVAL-ADAU1467Z</b>	<b>2</b>	<b>1</b>
SCALE:			SHEET 7 8

6

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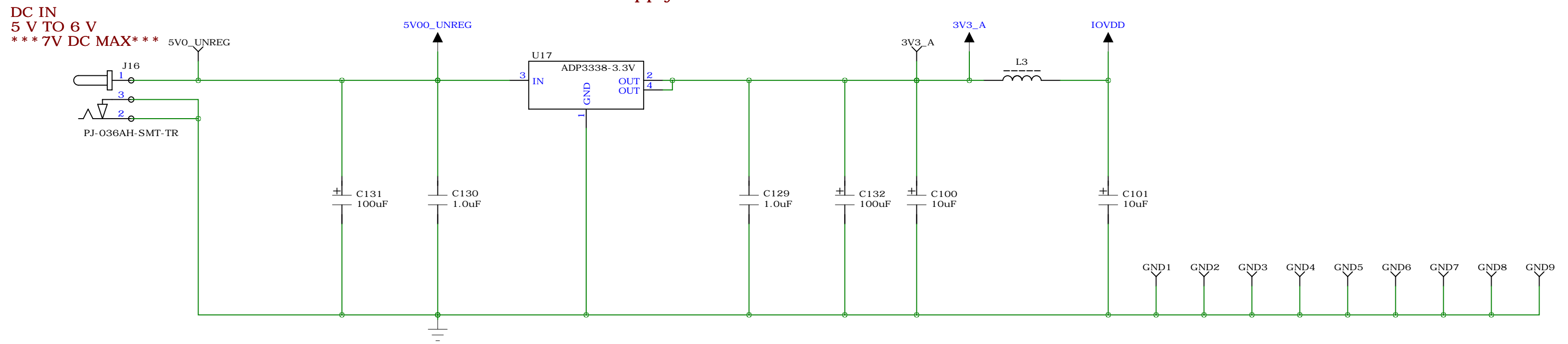
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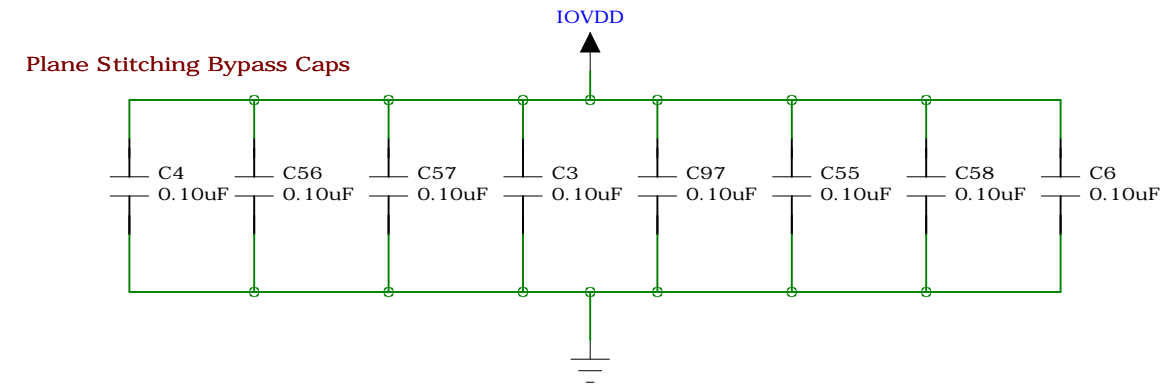
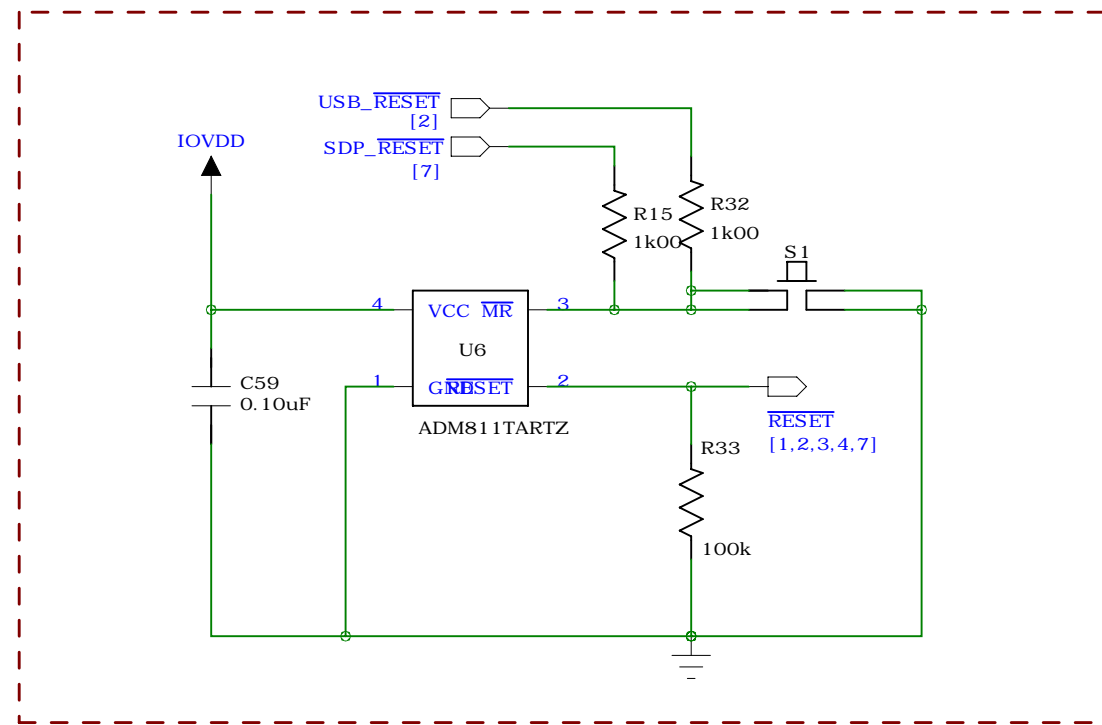
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

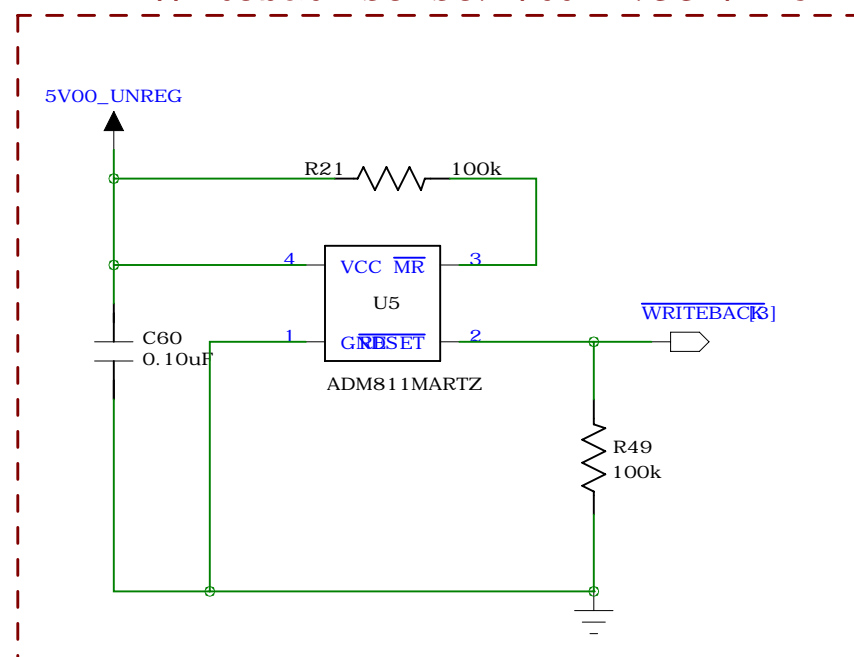
### Power Supply



### Reset Generator and Control



### Writeback sense: Vcc < 4.38 V DC



COMPANY:			
TITLE: <b>EVAL-ADAU1467Z POWER_SUPPLY</b>			
CODE:	SIZE:	DRAWING NO:	REV:
<b>ACE</b>	<b>C</b>	<b>14-Feb-18</b>	<b>2.1</b>
SCALE:			SHEET 8 8

DRAWN: <b>Ken Malsky</b>	DATED: <b>5/10/17</b>
CHECKED: <b>David Thibideau</b>	DATED: <b>TBD</b>
QUALITY CONTROL: <b>Miguel Chavez</b>	DATED: <b>TBD</b>
RELEASED: <b>Ken Malsky</b>	DATED: <b>TBD</b>