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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

ADAU1467

SigmaDSP Audio Processor

D

D

C

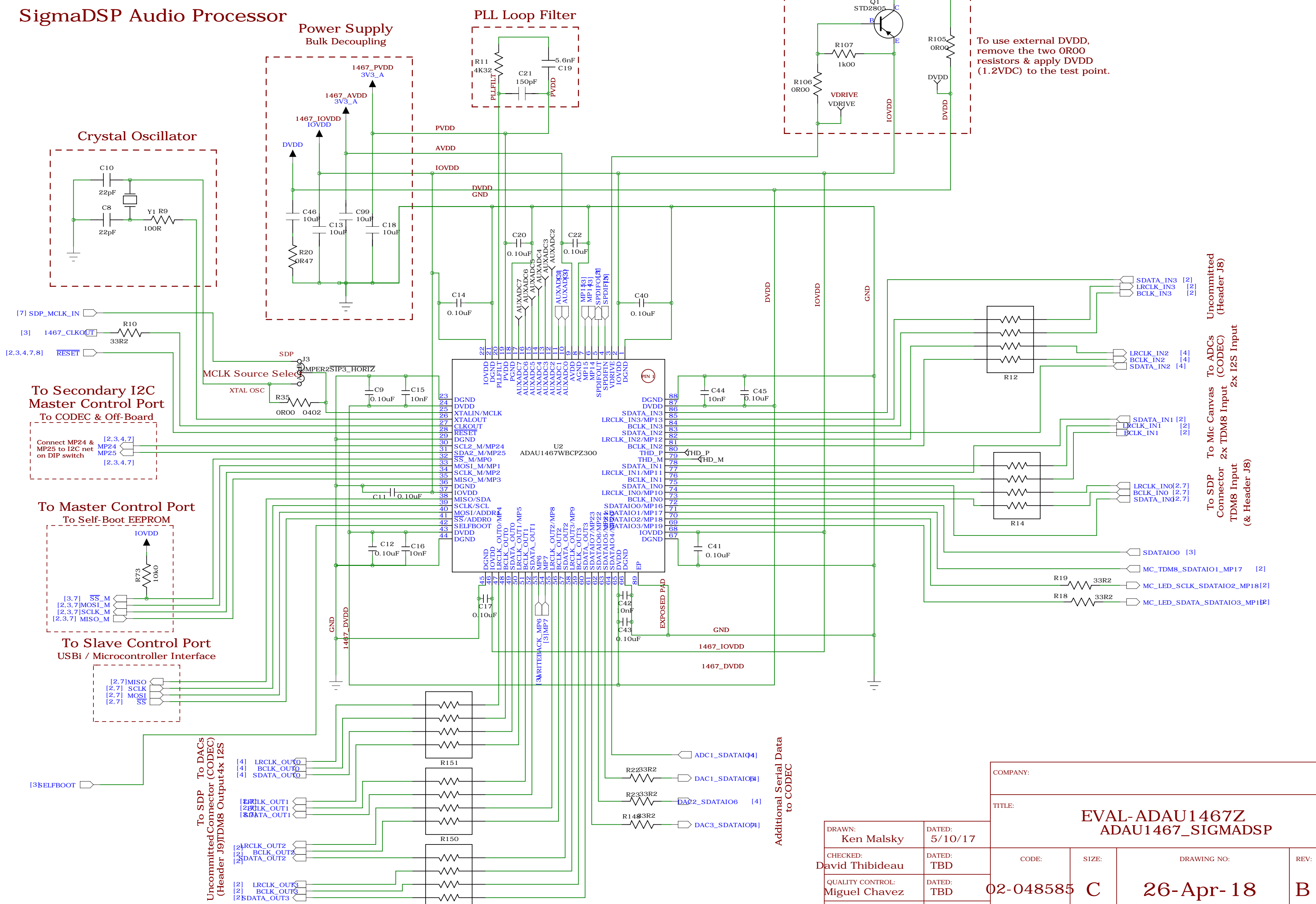
C

B

B

A

A



To use external DVDD, remove the two 0R00 resistors & apply DVDD (1.2VDC) to the test point.

To Mic Canvas To ADCs Uncommitted Connector (Header J8)
 To SDP Connector 2x TDM8 Input (CODEC) 2x I2S Input (& Header J8)

Additional Serial Data to CODEC

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: EVAL-ADAU1467Z ADAU1467_SIGMADSP			
CODE:	SIZE: C	DRAWING NO:	REV: B
02-048585		26-Apr-18	
SCALE:		SHEET: 1 of 8	

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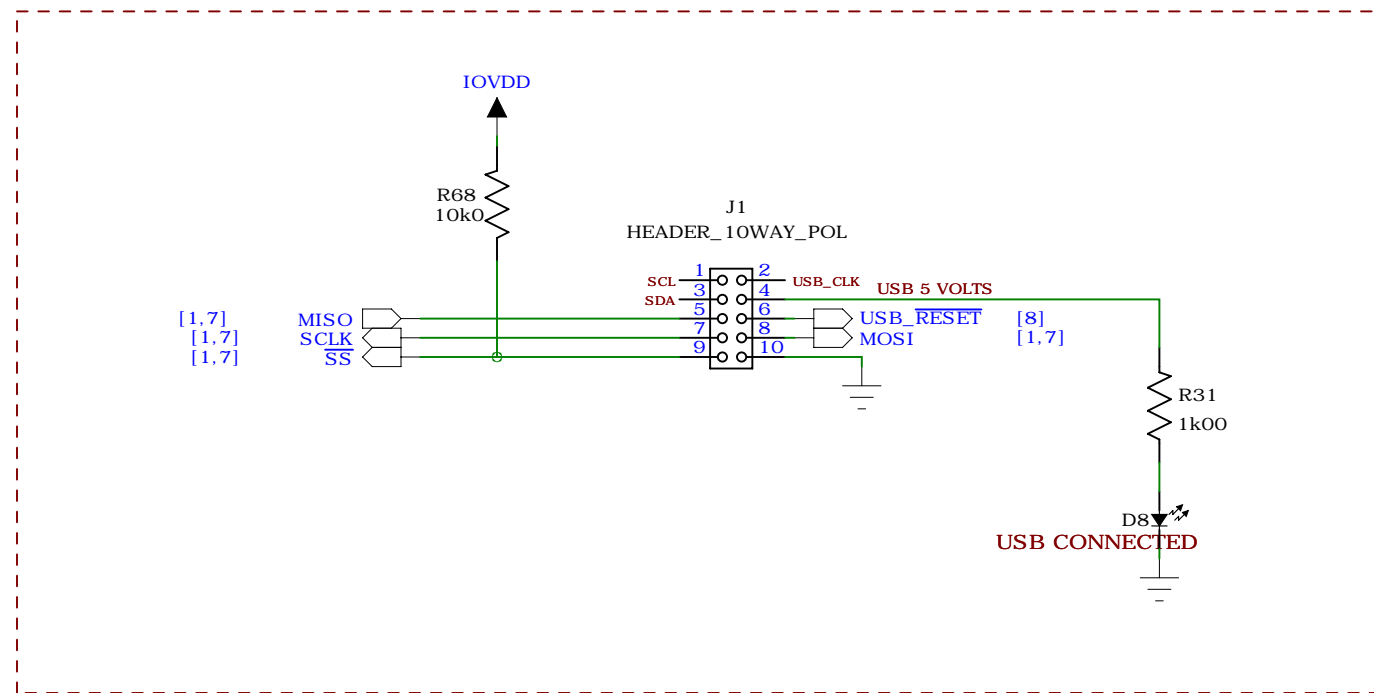
3

2

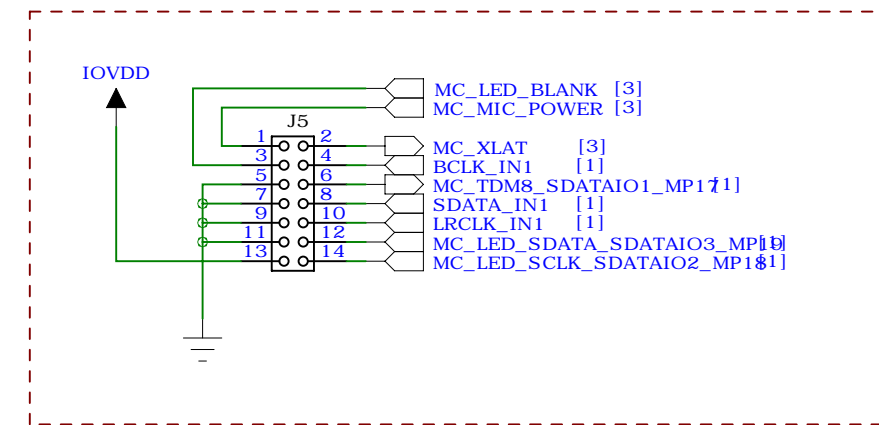
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

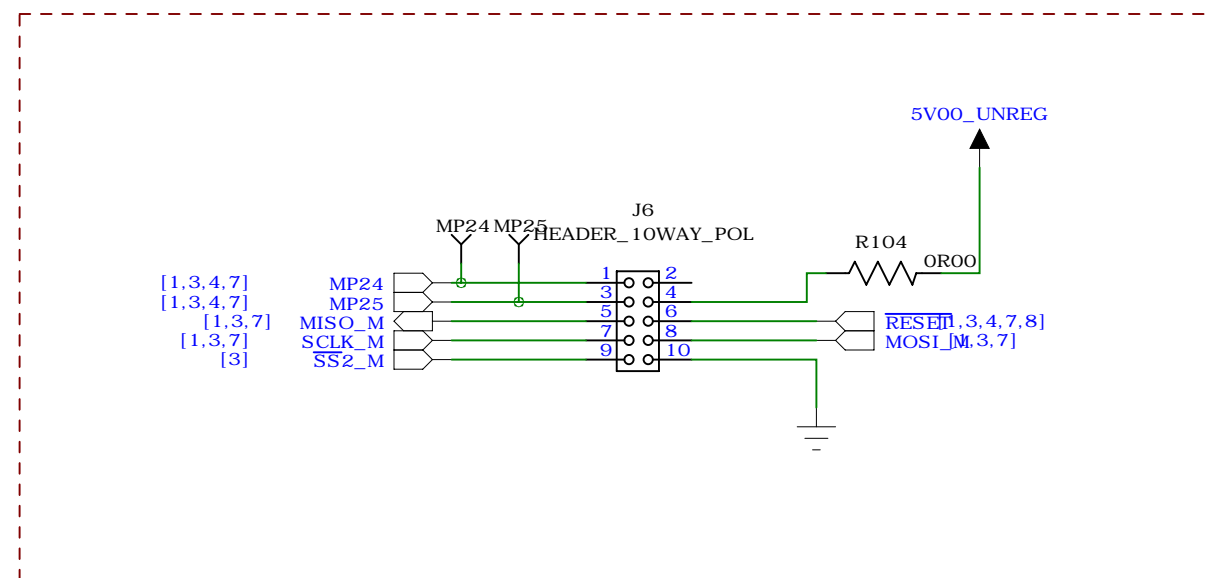
Control Input Port Header (USBi)
(DSP Programming/Control Interface)



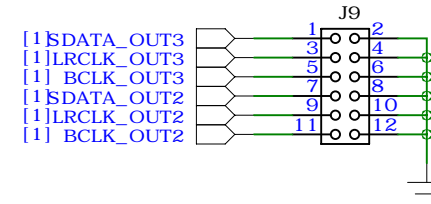
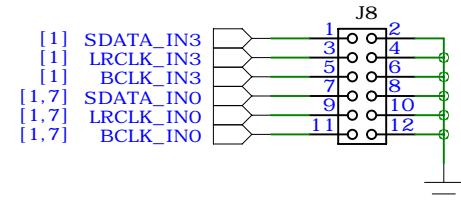
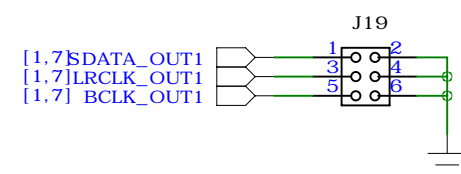
Mic Canvas Header



Control Output Port Header
(DSP Interface to Peripherals)



Uncommitted Serial Ports
(for user peripherals)



COMPANY:			
TITLE:			
EVAL-ADAU1467Z			
CODE:	SIZE:	DRAWING NO:	REV:
02-048585	C	26-Apr-18	B
SCALE:			SHEET 2 8

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

D

D

C

C

B

B

A

A

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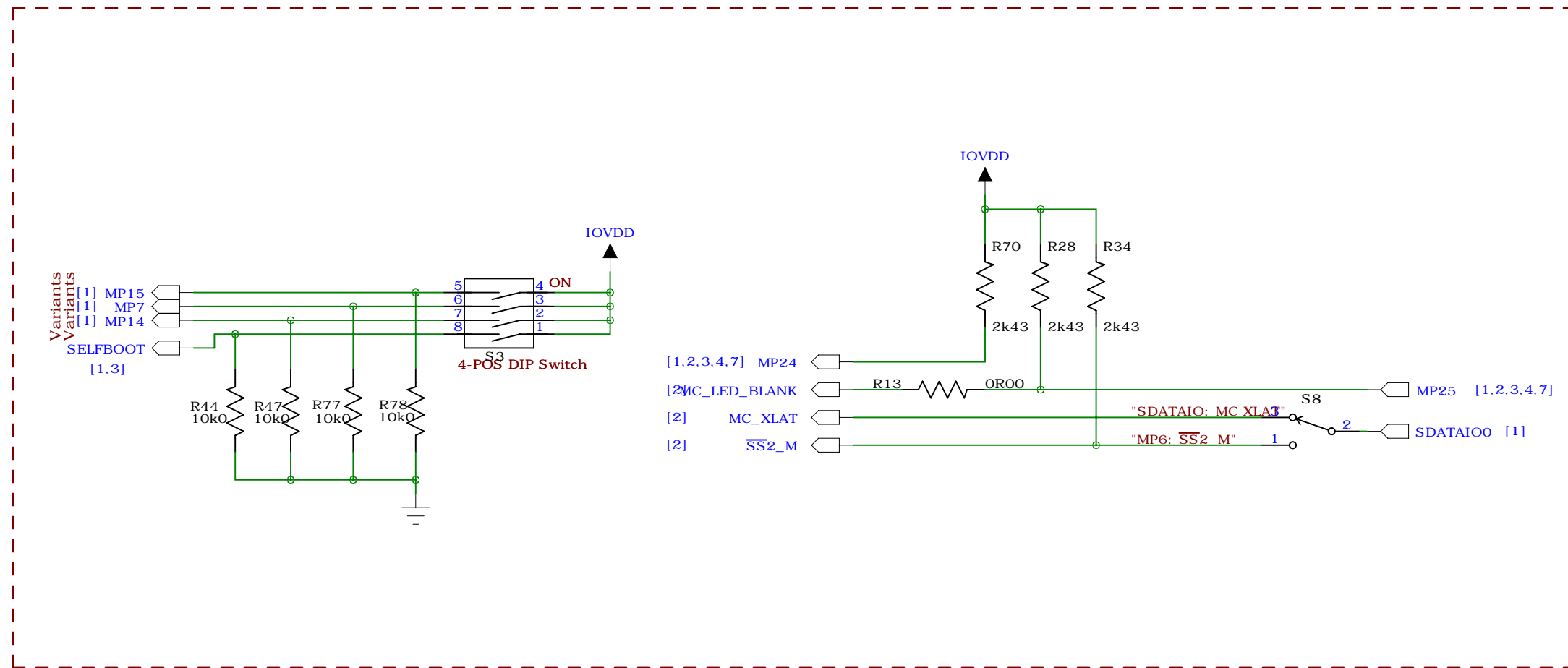
3

2

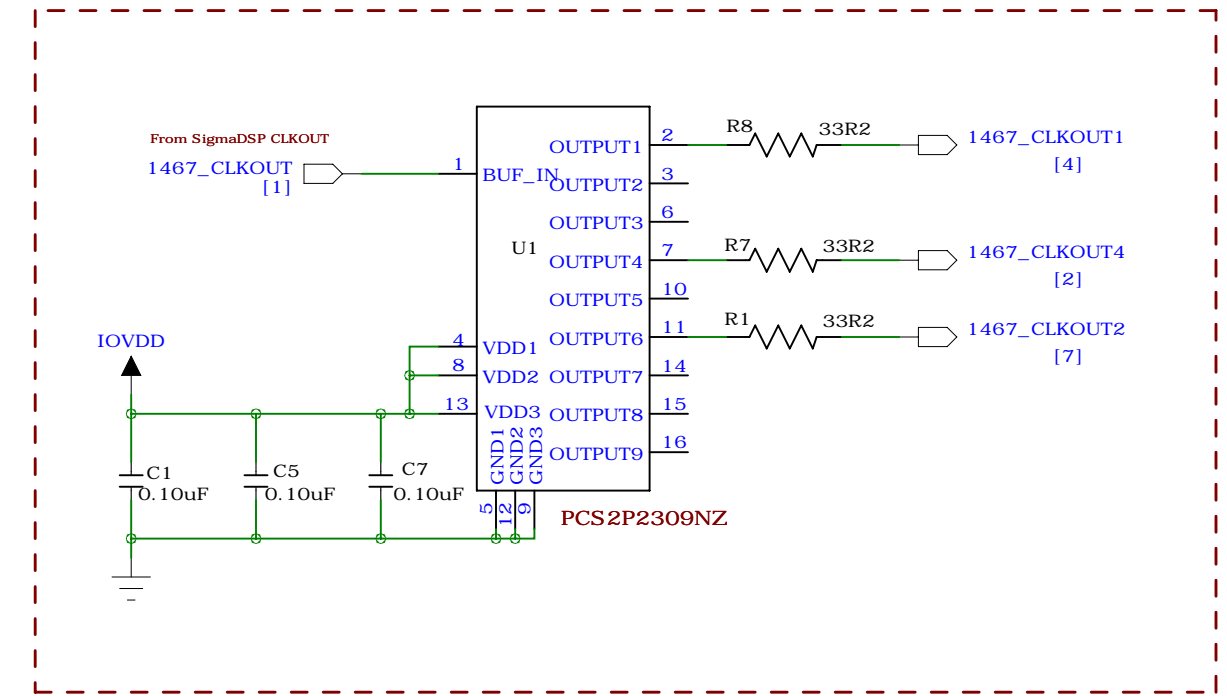
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

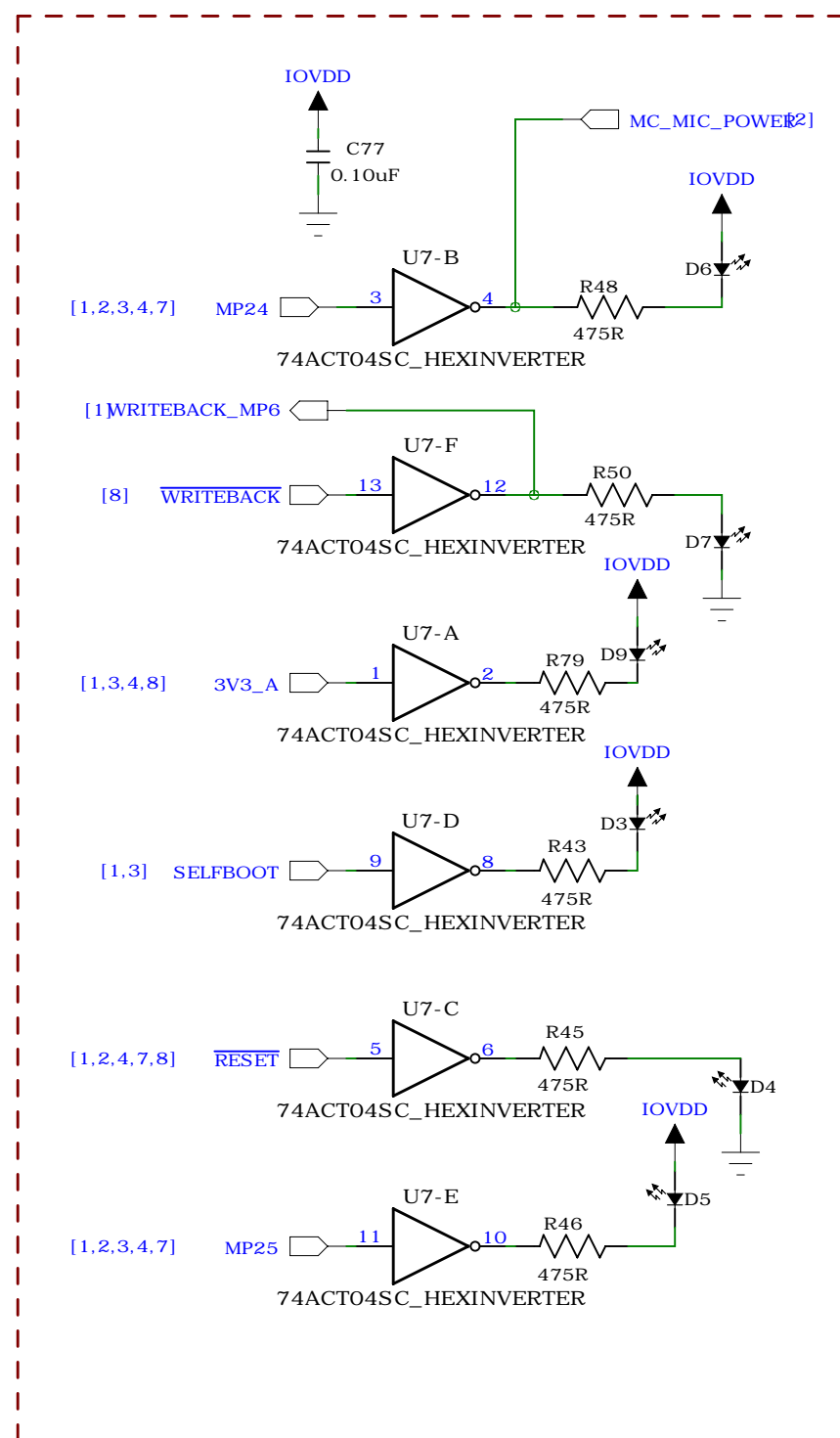
Configuration Options



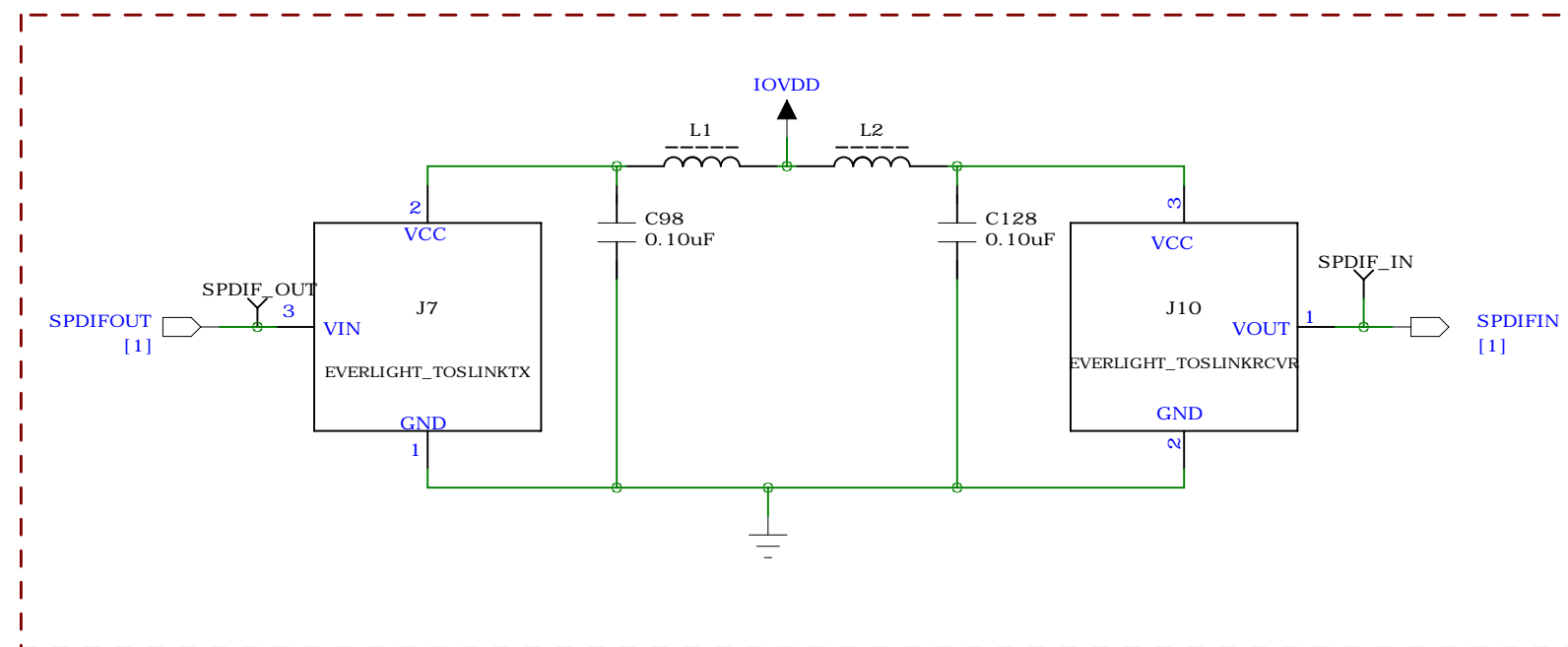
Clock Distribution



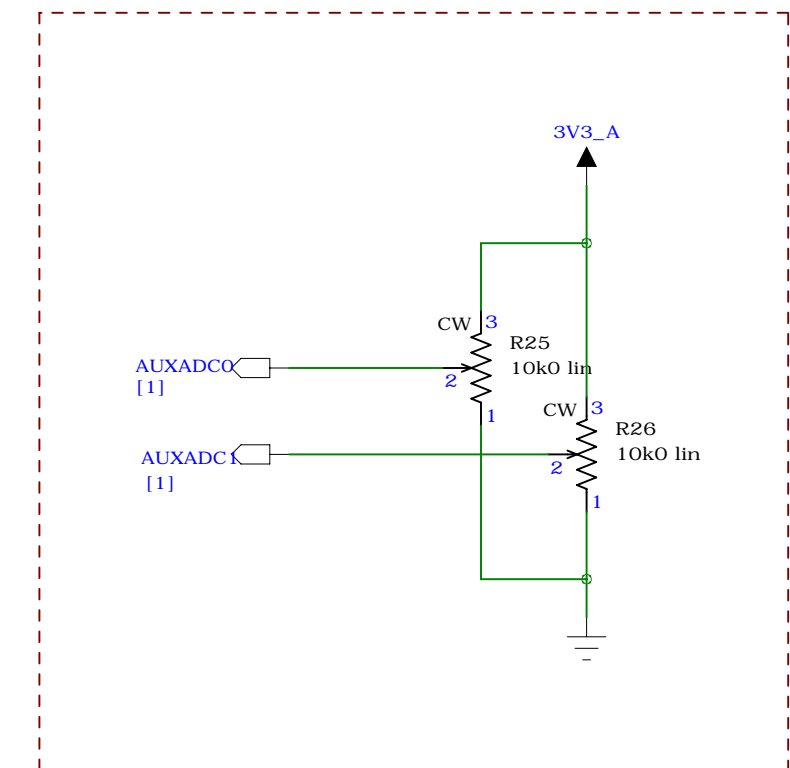
Status LEDs



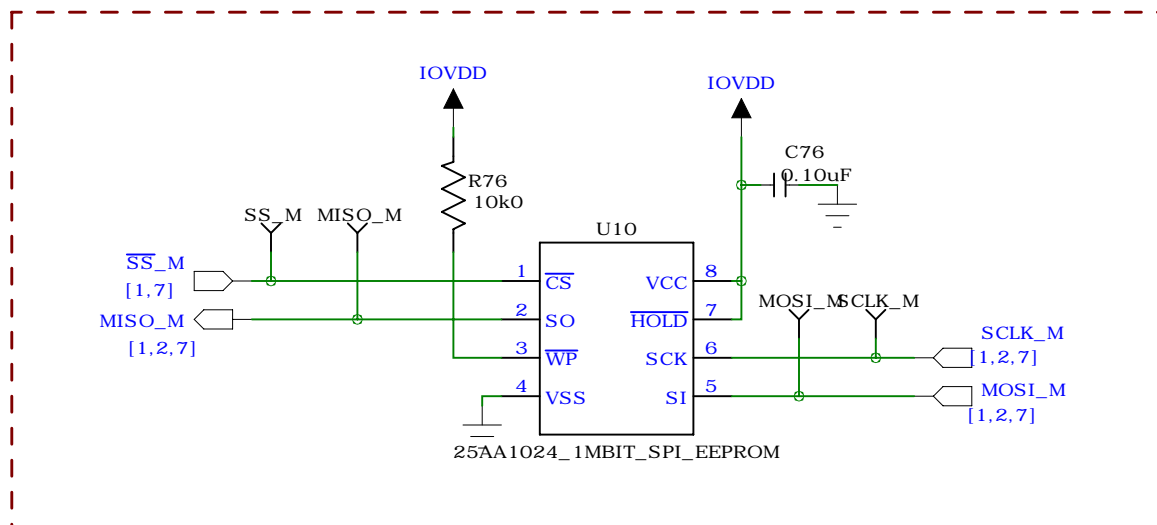
S/PDIF TOSLINK Optical Connectors



AUXADC Input



Self-Boot Memory



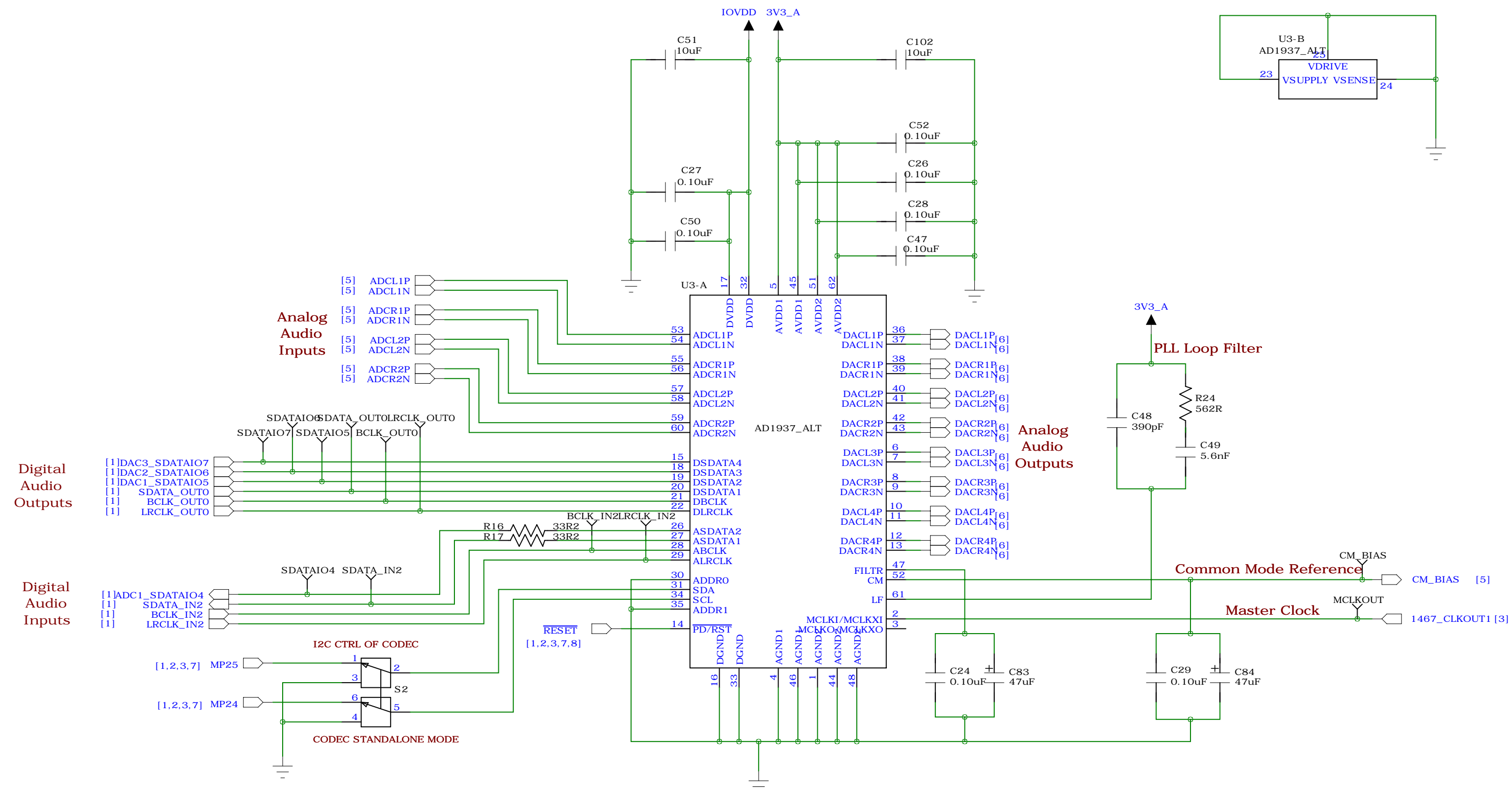
COMPANY:			
TITLE: EVAL-ADAU1467Z DSP_PERIPHERALS			
CODE:	SIZE:	DRAWING NO:	REV:
02-048585	C	26-Apr-18	B
SCALE:			SHEET 8

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

AD1937

4xADC 8xDAC Audio CODEC



COMPANY:			
TITLE: EVAL-ADAU1467Z AD1937_CODEC			
CODE:	SIZE:	DRAWING NO:	REV:
02-048585	C	26-Apr-18	B
SCALE:			SHEET 4 8

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

6

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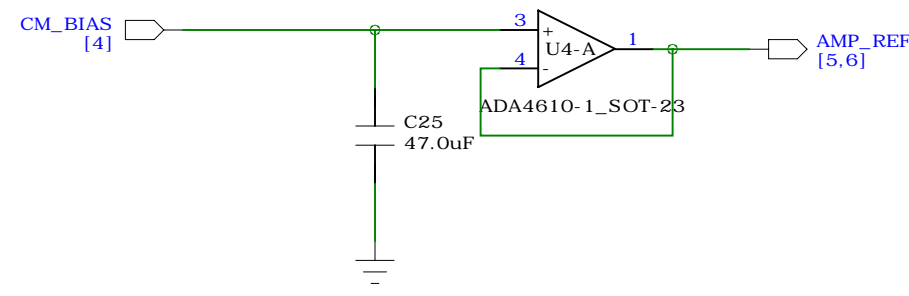
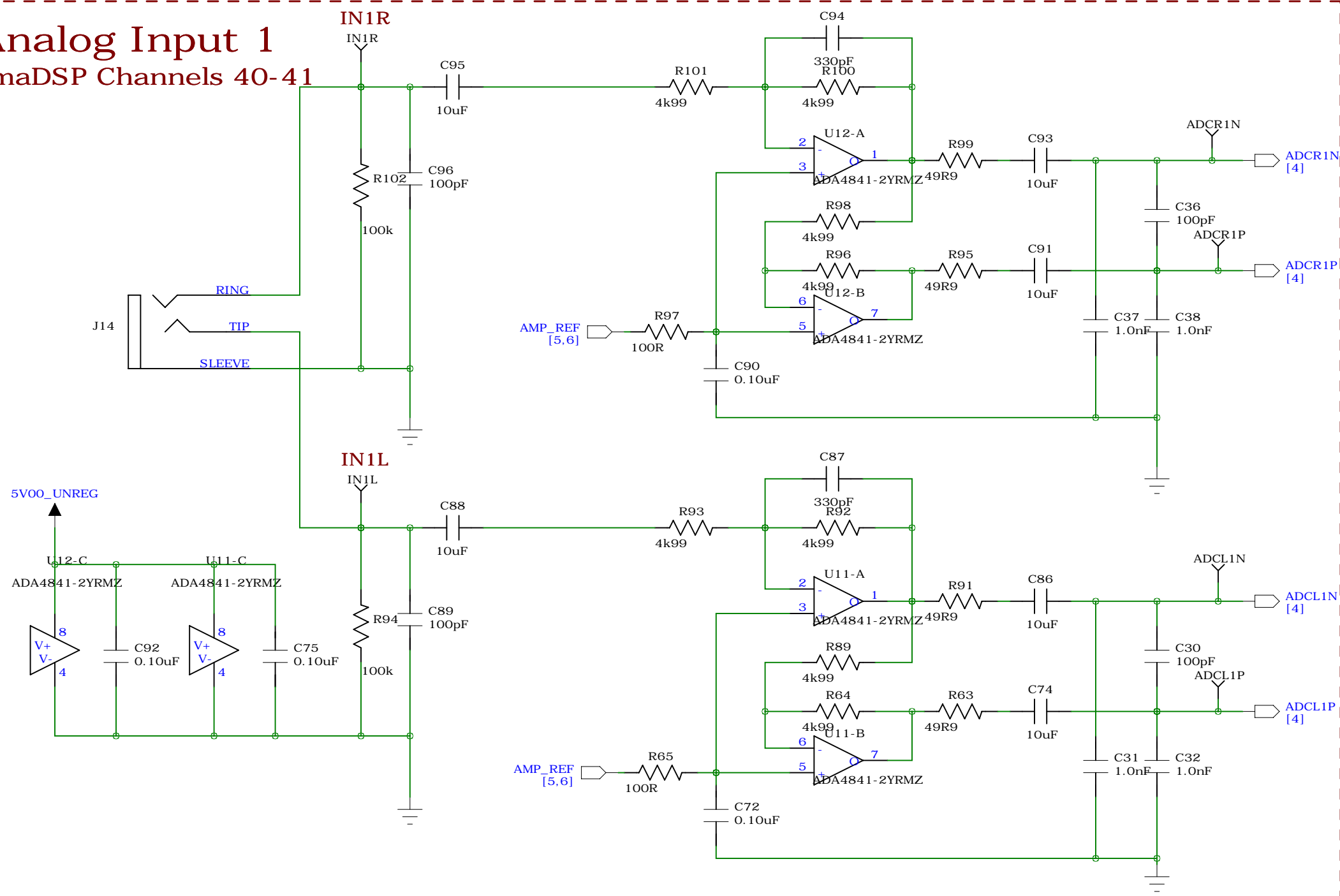
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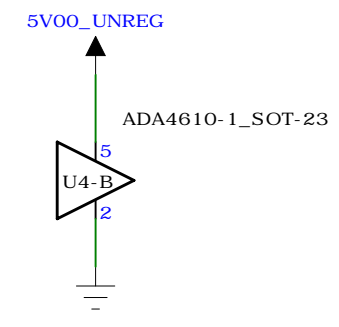
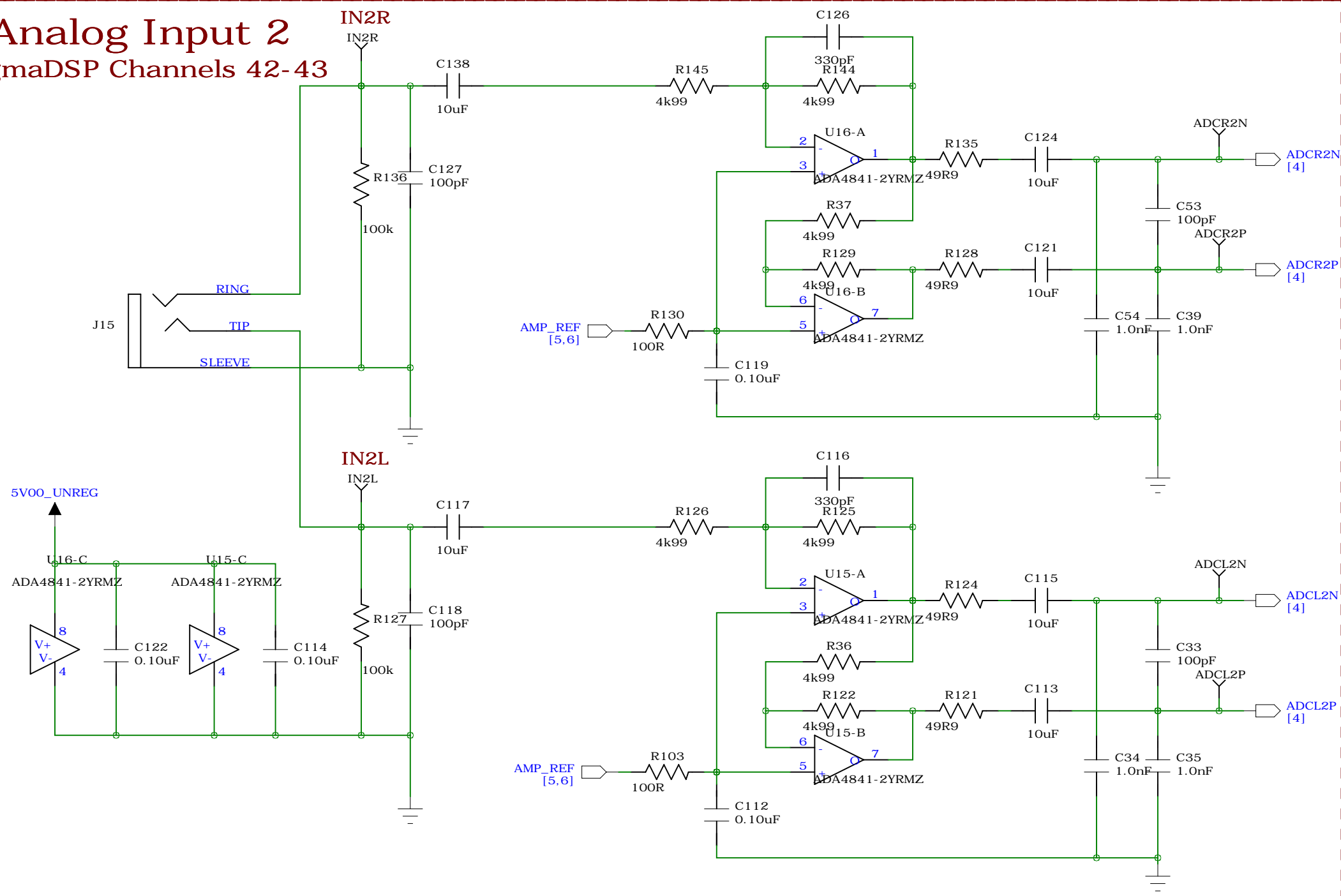
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Analog Input 1 SigmaDSP Channels 40-41



Analog Input 2 SigmaDSP Channels 42-43



DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: EVAL-ADAU1467Z ADC_BUFFERS			
CODE: 02-048585	SIZE: C	DRAWING NO: 26-Apr-18	REV: B
SCALE:			SHEET 5 of 8

6

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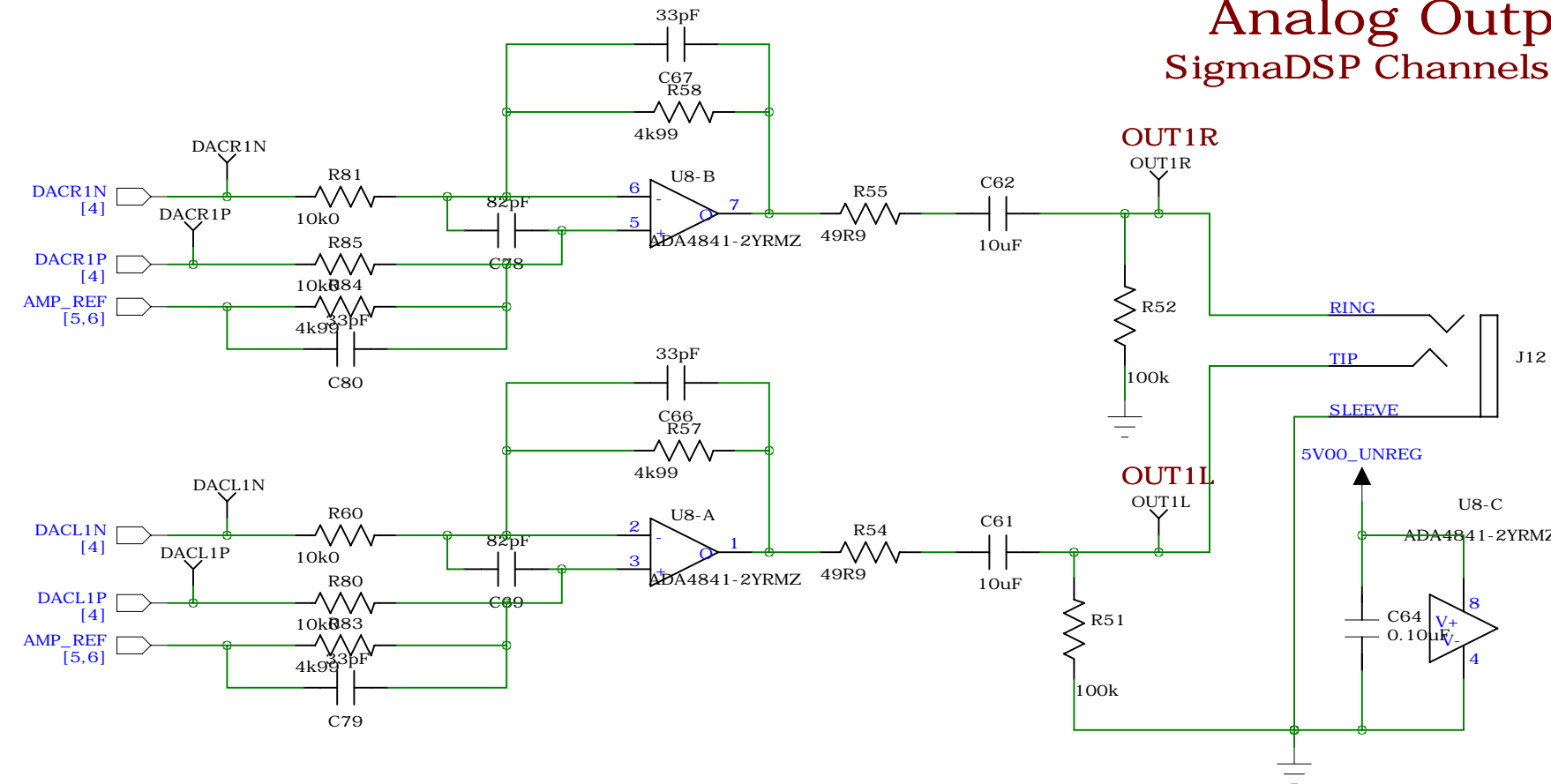
2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

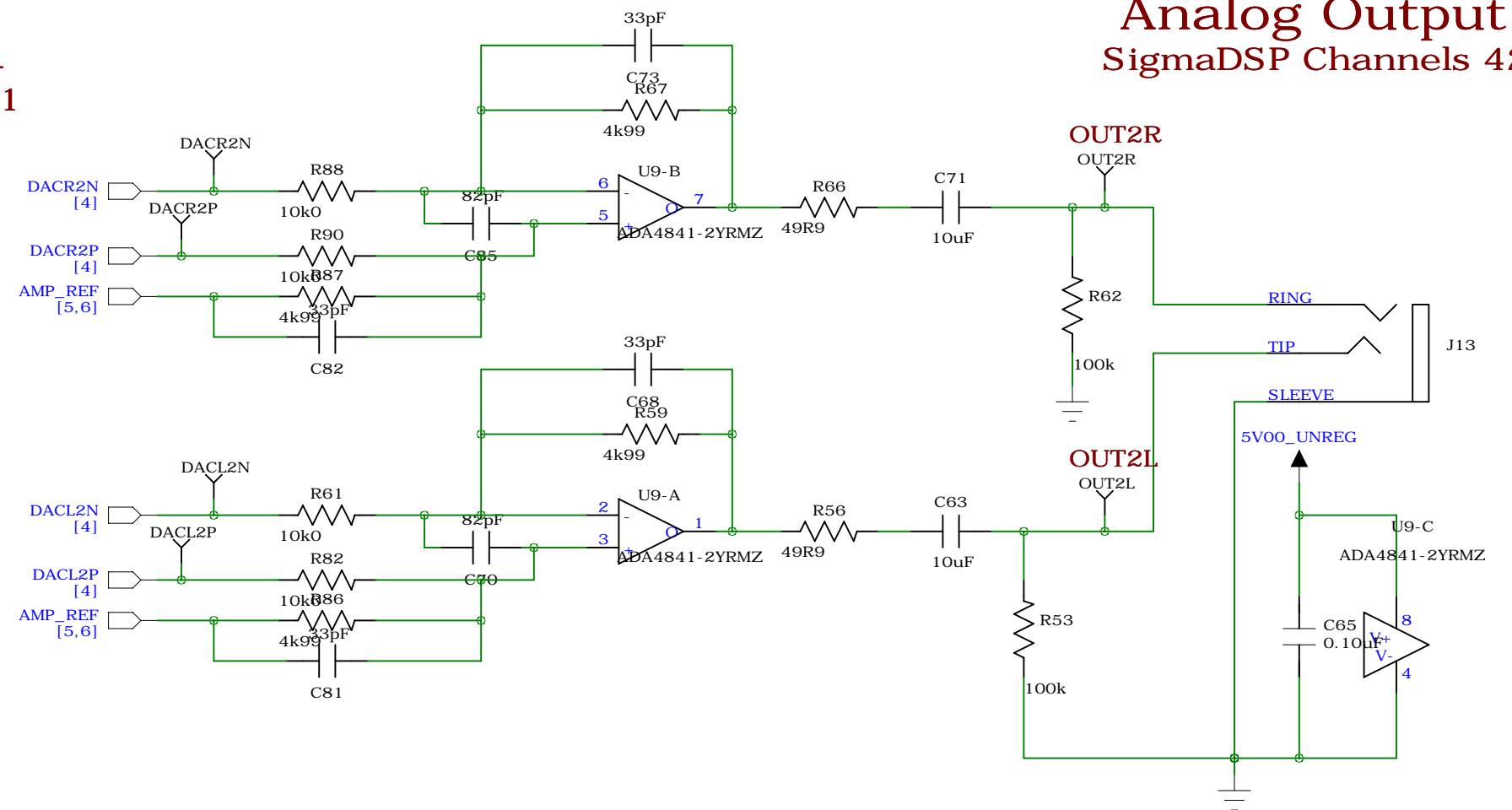
D

Analog Output 1 SigmaDSP Channels 40-41



C

Analog Output 2 SigmaDSP Channels 42-43

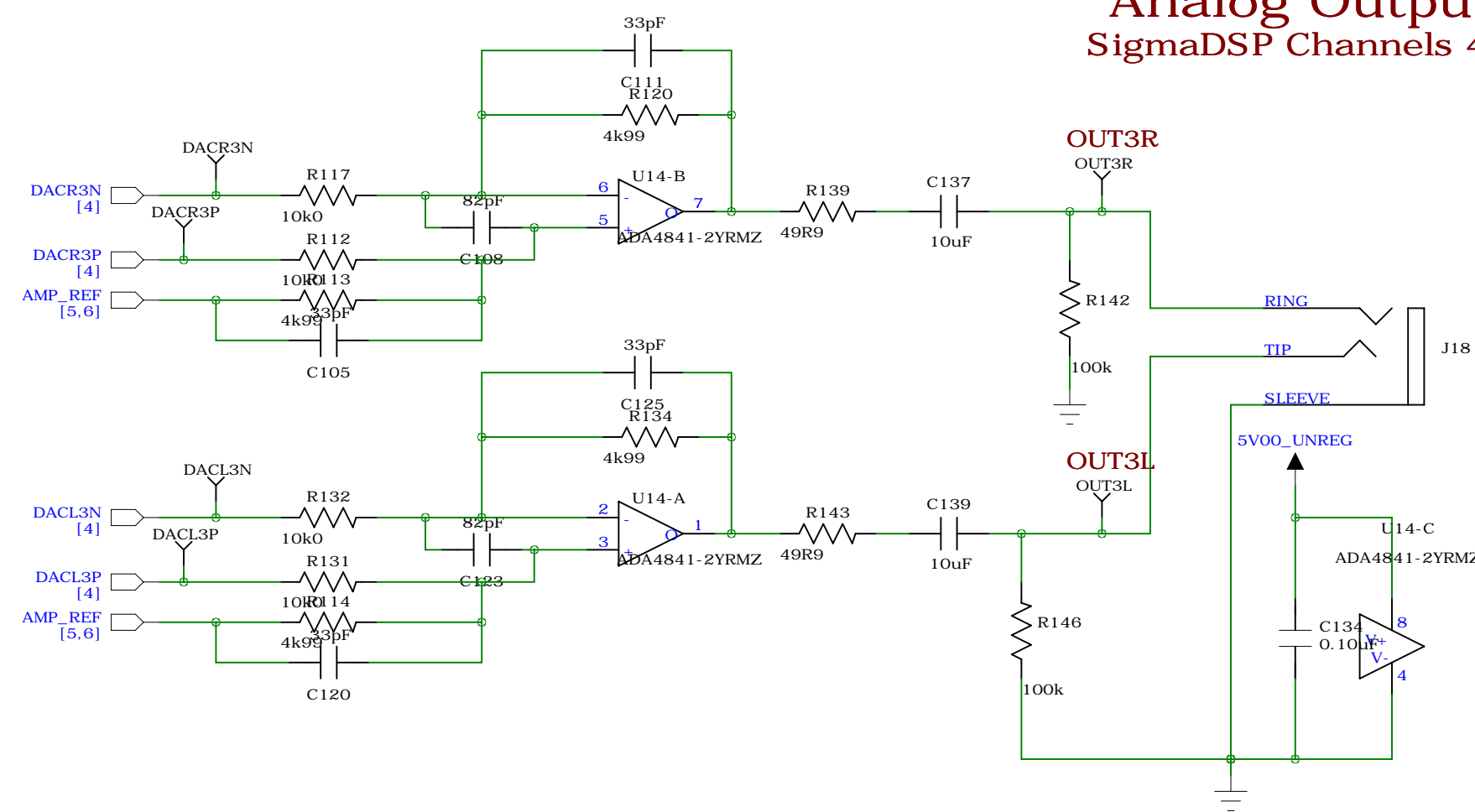


D

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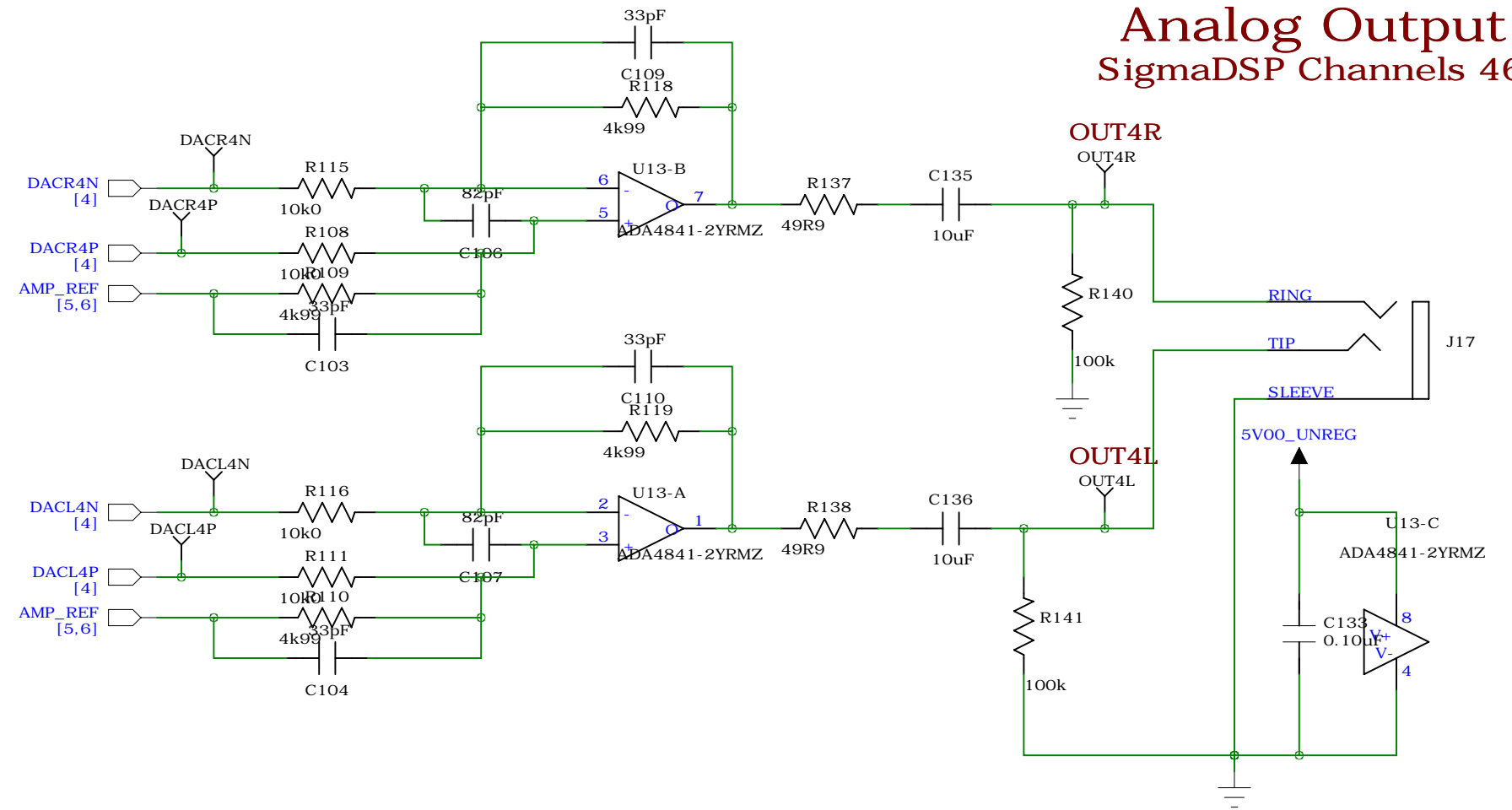
B

Analog Output 3 SigmaDSP Channels 44-45



A

Analog Output 4 SigmaDSP Channels 46-47



B

A

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD

COMPANY:			
TITLE: EVAL-ADAU1467Z DAC_BUFFERS			
CODE:	SIZE:	DRAWING NO:	REV:
02-048585	C	26-Apr-18	B
SCALE:			SHEET 6 8

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

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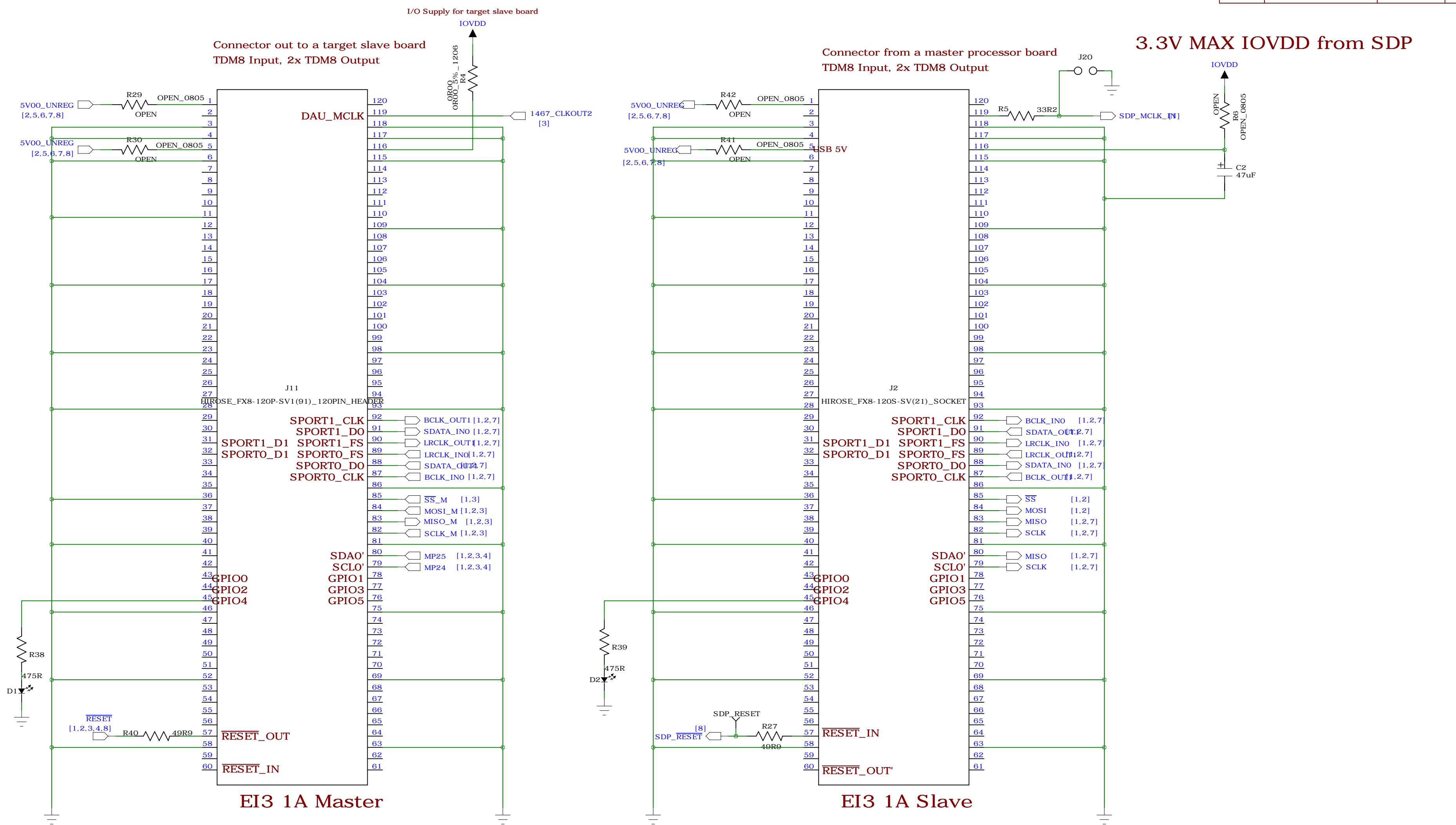
A

D

C

B

A



BCLK_IN0 [1,2,7] — R2 — OPEN — BCLK_OUT1 [1,2,7] — R3 — OPEN — LRCLK_IN0 [1,2,7] — R3 — OPEN — LRCLK_OUT1 [1,2,7]

COMPANY:			
TITLE: EVAL-ADAU1467Z SDP_INTERFACE			
DRAWN: Ken Malsky	DATED: 5/10/17	CODE:	REV:
CHECKED: David Thibideau	DATED: TBD	SIZE:	DRAWING NO:
QUALITY CONTROL: Miguel Chavez	DATED: TBD	02-048585 EVAL-ADAU1467Z B	
RELEASED: Ken Malsky	DATED: TBD	SCALE:	SHEET 7 8

6

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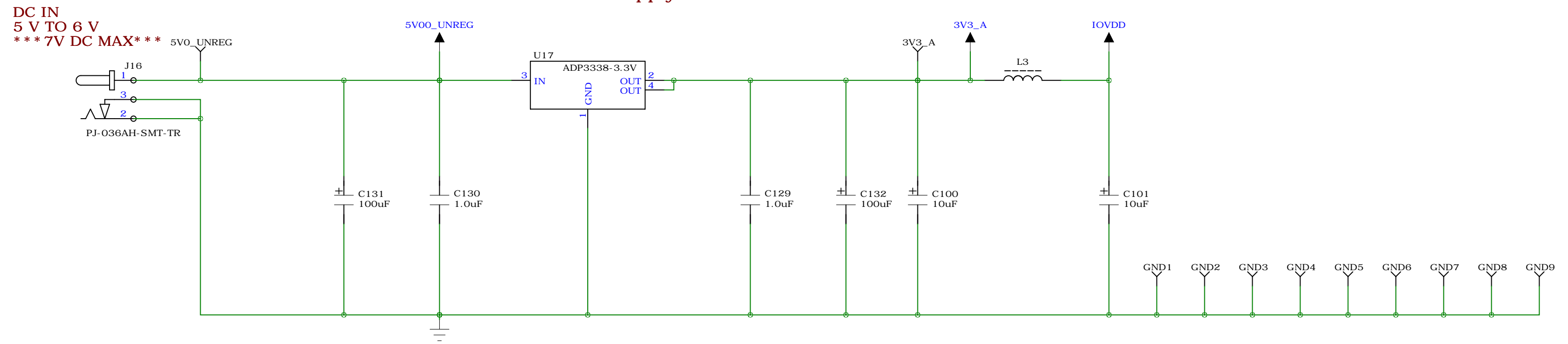
3

2

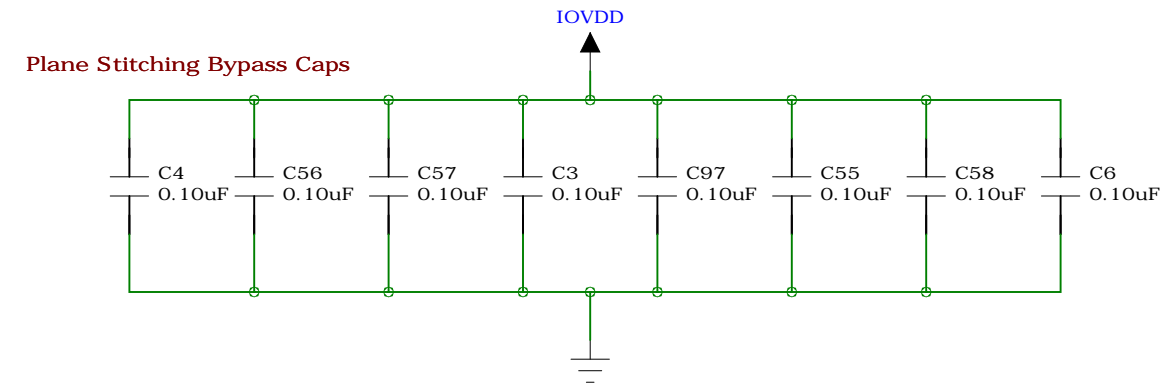
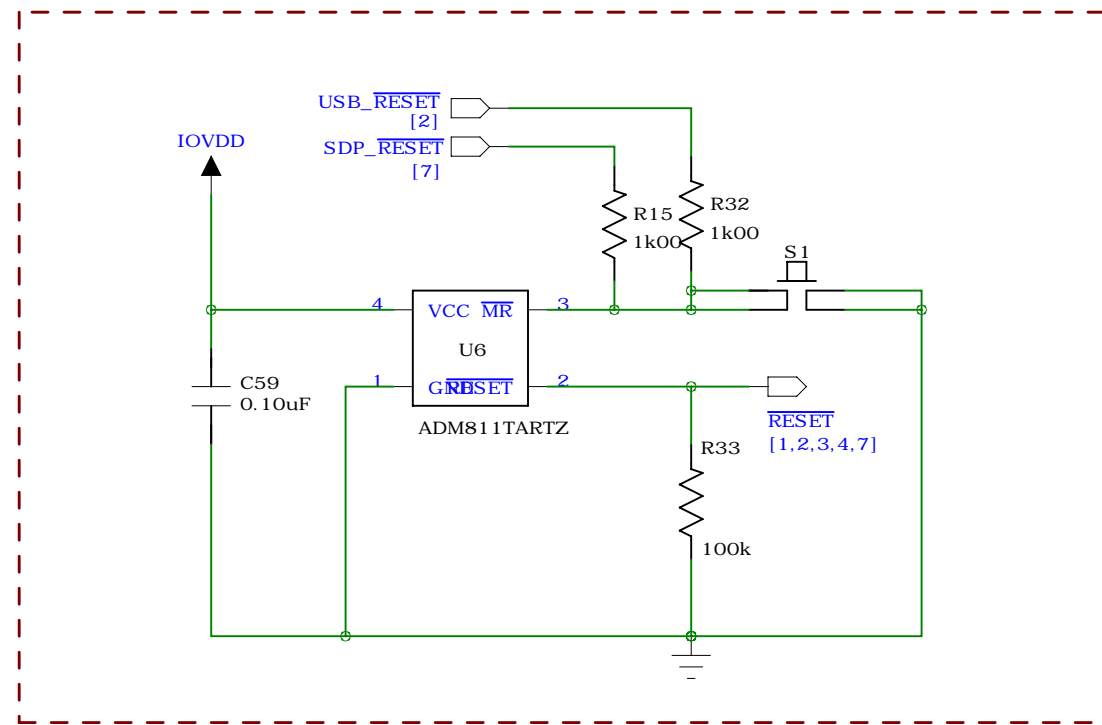
1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

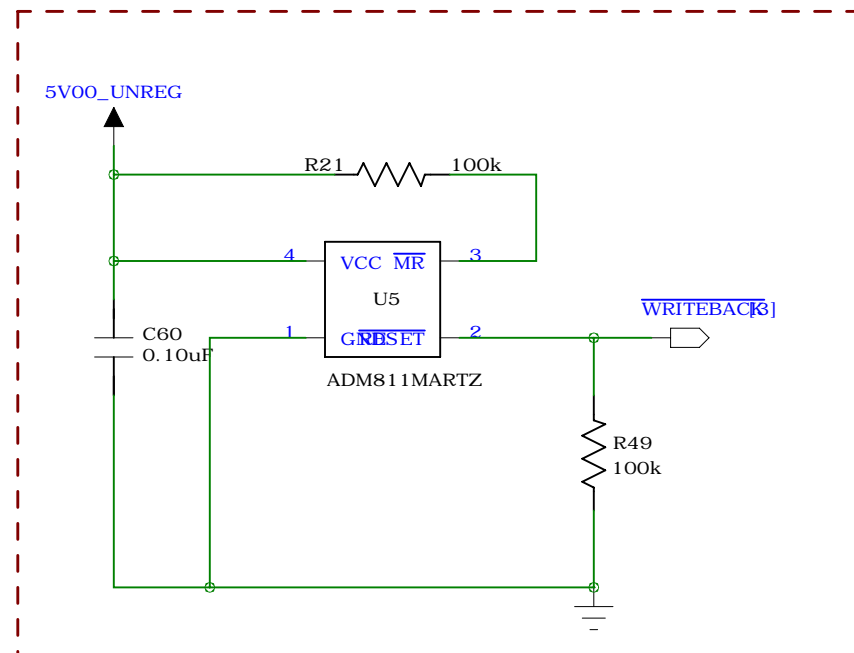
Power Supply



Reset Generator and Control



Writeback sense: Vcc < 4.38 V DC



COMPANY:			
TITLE: EVAL-ADAU1467Z POWER_SUPPLY			
CODE:	SIZE:	DRAWING NO:	REV:
02-048585	C	26-Apr-18	B
SCALE:			SHEET 8

DRAWN: Ken Malsky	DATED: 5/10/17
CHECKED: David Thibideau	DATED: TBD
QUALITY CONTROL: Miguel Chavez	DATED: TBD
RELEASED: Ken Malsky	DATED: TBD