APPLICATIONS INFORMATION

A typical application circuit for the ADMV7710 is shown in Figure 47. Combine the supply lines as shown in the application circuit schematic to minimize the external component count and to simplify power supply routing.

The ADMV7710 uses several amplifier, detector, and attenuator stages. All stages use depletion mode pHEMT transistors. It is important to use the following power-up bias sequence to avoid transistor damage:

1. Apply a −2 V bias to the VGG1A to VGG4A and VGG1B to VGG4B pads.
2. Apply 4 V to the VDD1A to VDD4A and VDD1B to VDD4B pads.
3. Adjust VGG1A to VGG4A and VGG1B to VGG4B between −2 V and 0 V to achieve a total amplifier drain current of 800 mA.

To power down the ADMV7710, follow the reverse procedure. For additional guidance on general bias sequencing, see the *MMIC Amplifier Biasing Procedure* application note.

ASSEMBLY DIAGRAM

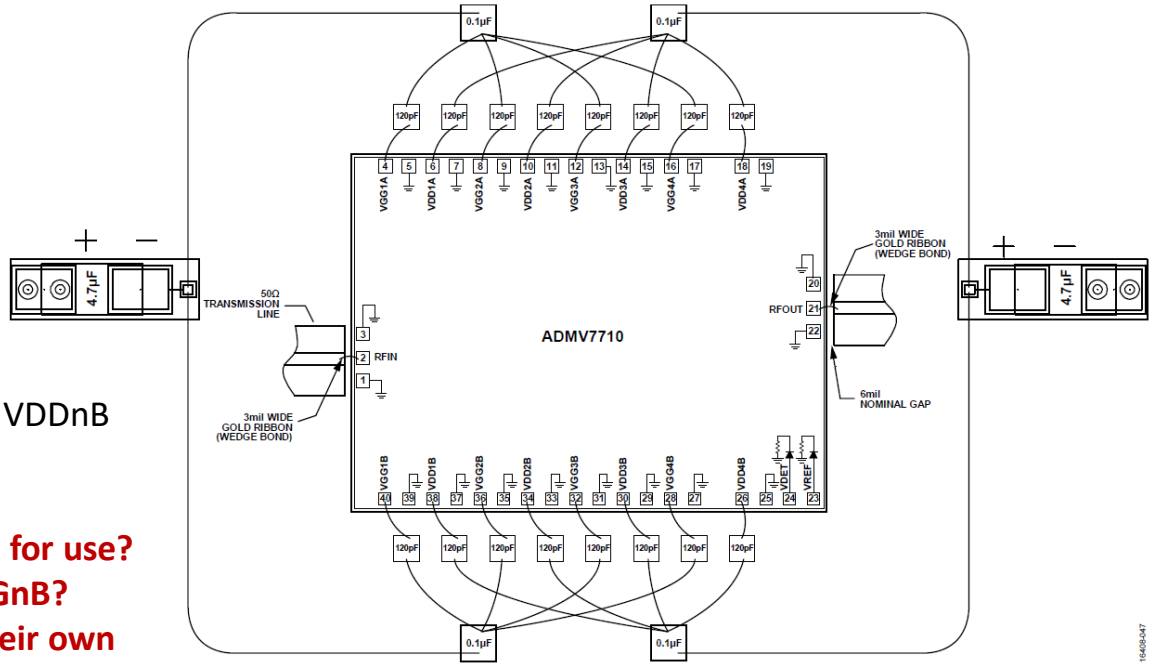

Figure 48. Assembly Diagram

Question

I have confirmed that ADMV7710 works normally when VDD1A to VDD4A were connected to 4V and VDD1B to VDD4B were not connected anywhere.
Of course, it also worked normally when VDD1B to VDD4B were connected to 4V, but the drain current was the same as when only VDD1A to VDD4A were connected.
I also confirmed that there was conduction between VDDnA and VDDnB by measuring with a tester. (n=1,2,3,4)

Is there any problem if I supply VDD to either VDDnA or VDDnB for use?
Similarly, is there any problem if I connect either VGGnA or VGGnB?
As far as VDD is concerned, why do VDDnA and VDDnB need their own power supply when they are connected internally?