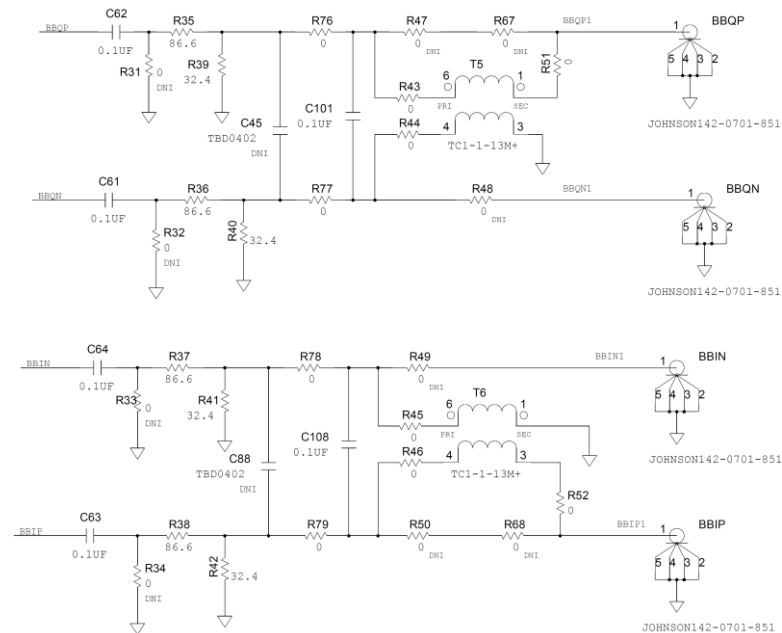
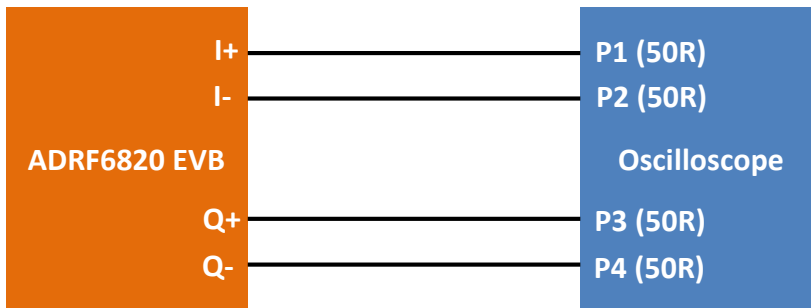


# Test 1 (1/3)

## HW Settings :

1. I path and Q path connected with oscilloscope directly.
  - R35/R36/R37/R38 changed to 0R
  - R39/R40/R41/R42 changed to DNI
  - C45/C88/C101/C108 changed to DNI
  - R43/R44/R45/R46/R51/R52 changed to DNI
  - R47/R48/R49/R50/R67/R68 changed to 0R
2. Oscilloscope set to 50R for each port.
3. RF (RF0 port) : 1960MHz, -1.95dBm  
LO (LO IP port) : 1950MHz, -1.25dBm



# Test 1 (2/3)

## SW Settings :

1. Control SW set to "EXT VCO/LO", "Polyphase Filter" and "BWSEL=0".

ADRF6820 Engineering

BWSEL	Gain	BW
0	High	High
1	High	Low
2	Low	High
3	Low	Low

**PLL Reference Input**  
 PLL REF IN (MHz) 153.6  
 PLL REF DIVIDER DIV4

**Charge Pump**  
 PFD FREQ (MHz) 38.4  
 CSCALE 500 uA  
 BLEED up 93.75 u  
 ABLDLY 0 nsec  
 CPCTRL PFD  
 CLKEDGE Div \, Ref \

**VCO Settings**  
 VCO\_SEL EXT VCO/LO  
 VCO FREQ (MHz) 4000

**Register Write Log**

```

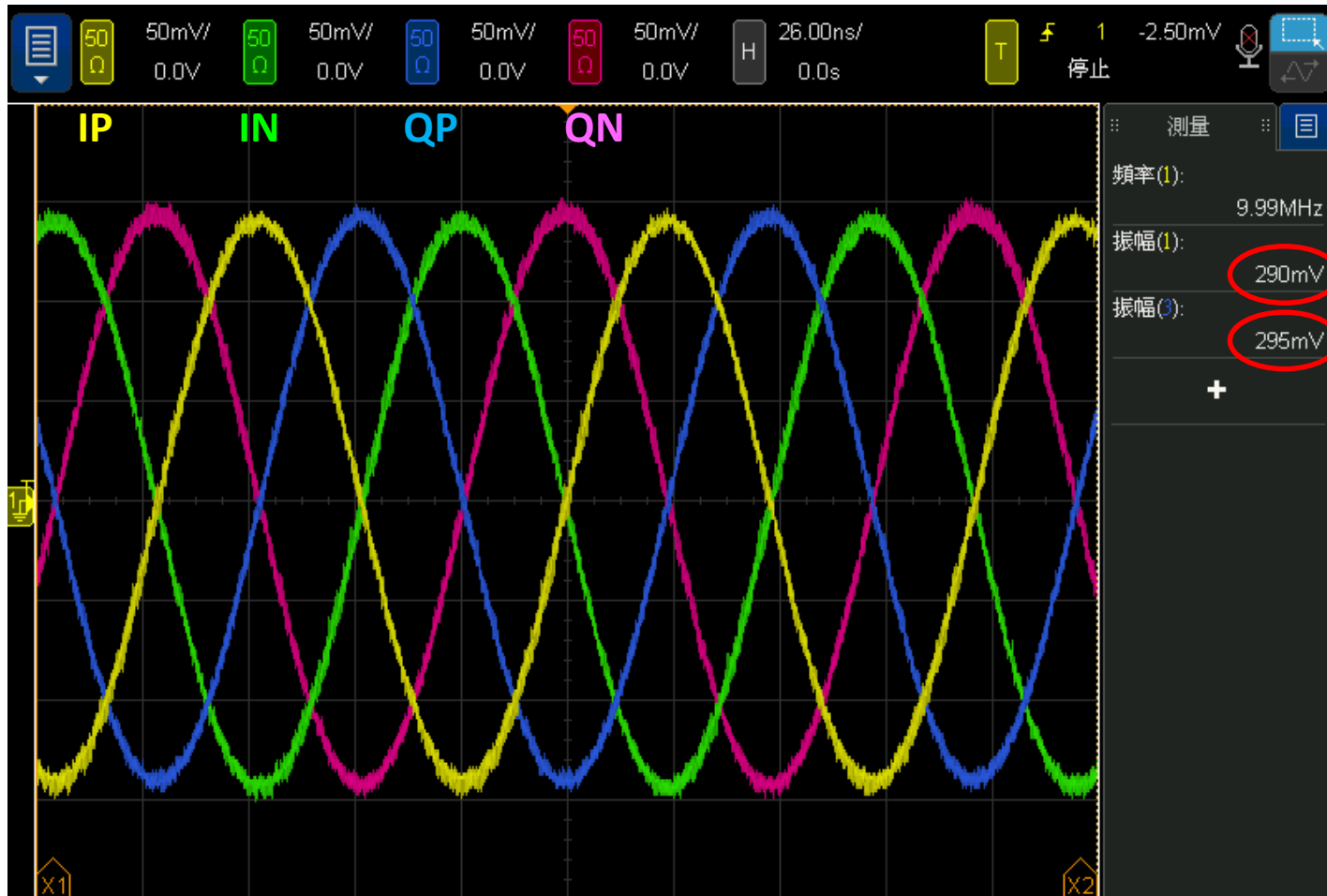
0x05:0x0000
0x01:0xde7f
0x01:0xde7f
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x20:0x0026
0x20:0x0026
0x05:0x0000
0x05:0x0000
0x21:0x0003
0x22:0x0002
  
```

**Legend:**  
 Green box, enter value  
 Yellow box, read only

**Buttons:** Update GUI, Save Register File, Open Register File, Clear

# Test 1 (3/3)

## IQ Output



# Test 2 (1/3)

## HW Settings :

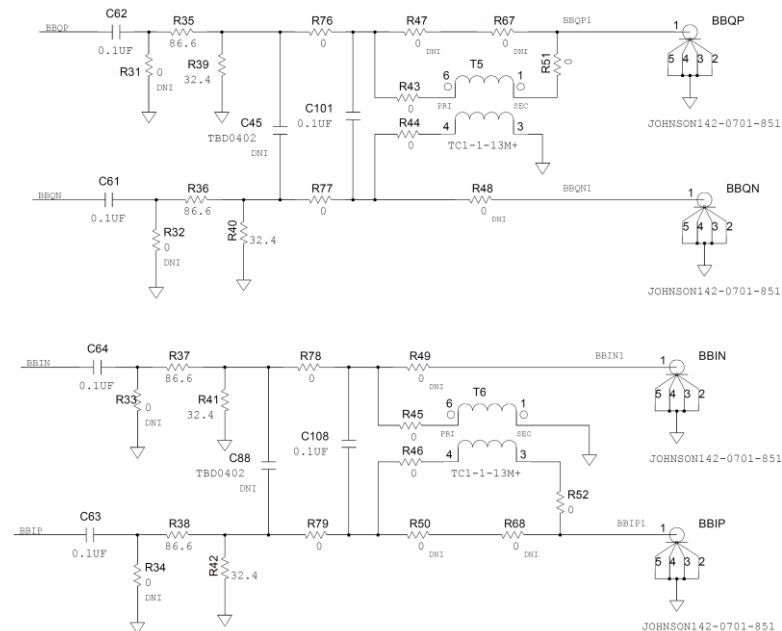
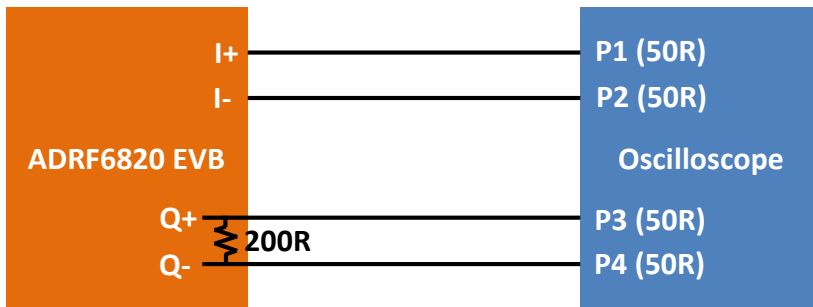
1. I path connected with oscilloscope directly and **Q path added a parallel 200R.**

- R35/R36/R37/R38 changed to 0R
- R39/R40/R41/R42 changed to DNI
- C88 changed to 200R, C45/C101/C108 changed to DNI
- R43/R44/R45/R46/R51/R52 changed to DNI
- R47/R48/R49/R50/R67/R68 changed to 0R

2. Oscilloscope set to 50R for each port.

3. RF (RF0 port) : 1960MHz, -1.95dBm

LO (LO IP port) : 1950MHz, -1.25dBm



# Test 2 (2/3)

## SW Settings :

1. Control SW set to "EXT VCO/LO", "Polyphase Filter" and "BWSEL=0".

ADRF6820 Engineering

BWSEL	Gain	BW
0	High	High
1	High	Low
2	Low	High
3	Low	Low

Key Settings:

- BWSEL:** 0 (Red box)
- BB\_BIAS:** 10 mA
- Polyphase Filter:** Polyphase Filter F (Red box)
- VCO\_SEL:** EXT VCO/LO (Red box)
- PFD FREQ (MHz):** 38.4 (Yellow box)
- VCO FREQ (MHz):** 4000 (Yellow box)
- PLL REF IN (MHz):** 153.6 (Green box)
- PLL REF DIVIDER:** DIV4 (Green box)
- LO FREQ (MHz):** 2000 (Green box)
- STEP SIZE (kHz):** 25 (Green box)
- STEP SIZE MULT:** 1 (Green box)

Register Write Log:

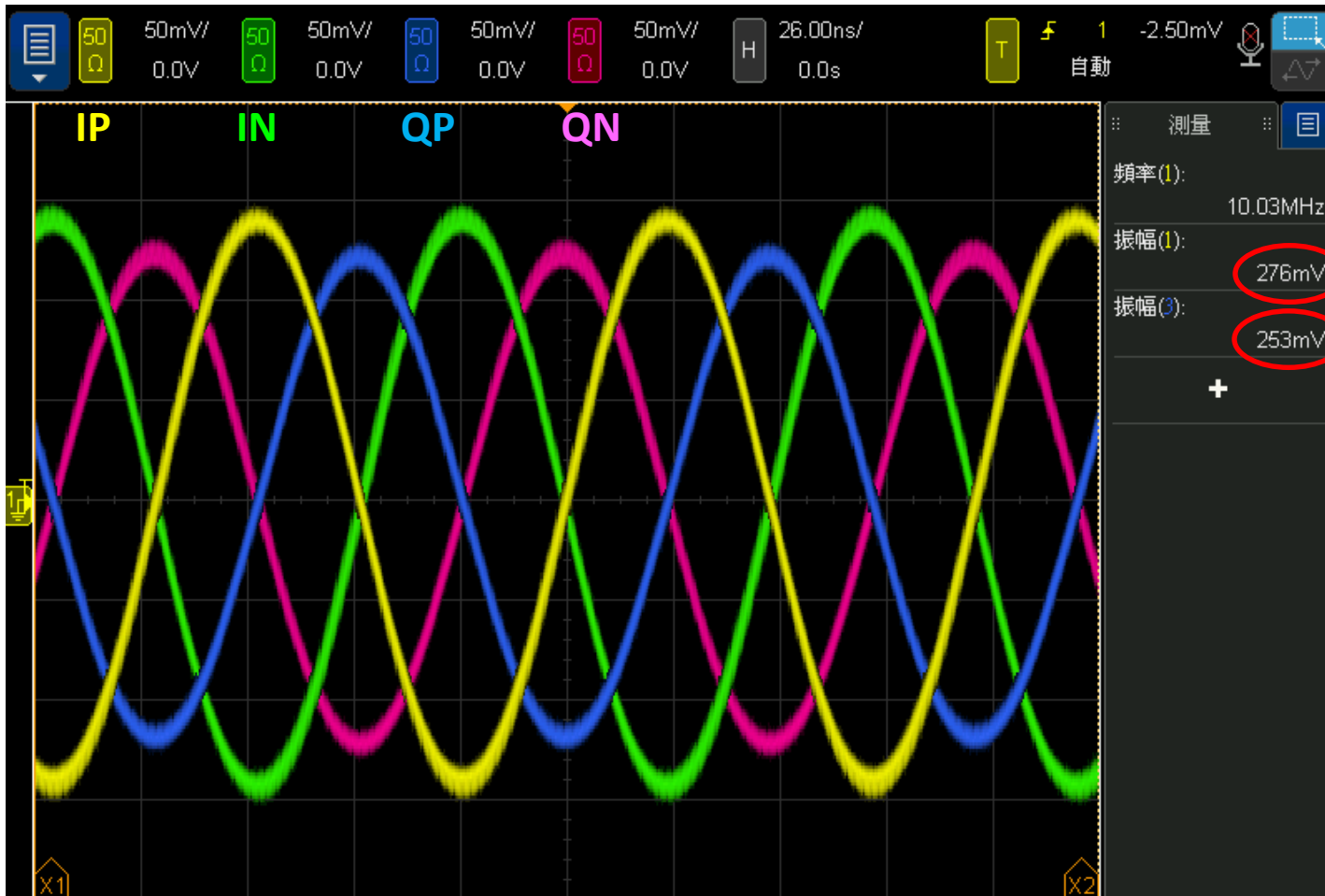
```

0x05:0x0000
0x01:0xde7f
0x01:0xde7f
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x20:0x0026
0x20:0x0026
0x05:0x0000
0x05:0x0000
0x21:0x0003
0x22:0x0002
    
```

Buttons: Update GUI, Save Register File, Open Register File, Clear

# Test 2 (3/3)

## IQ Output



# Test 3 (1/3)

## HW Settings :

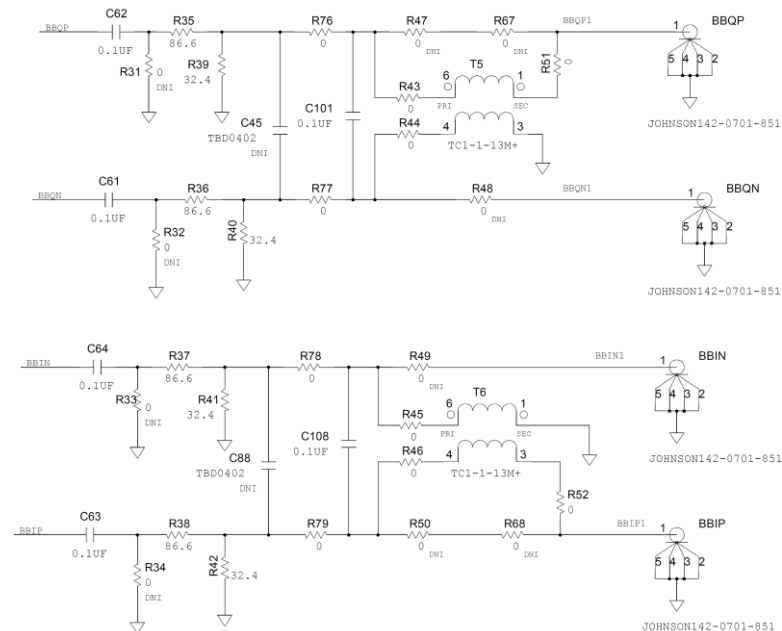
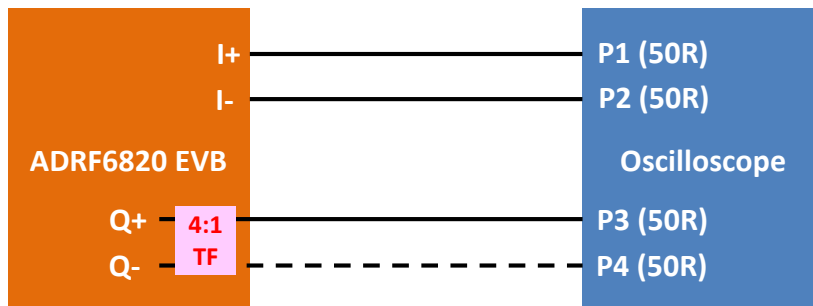
1. I path connected with oscilloscope directly and **Q path added a 4:1 impedance transformer (TC4-1W+).**

- R35/R36/R37/R38 changed to 0R
- R39/R40/R41/R42 changed to DNI
- C45/C88/C101/C108 changed to DNI
- T5 changed to TC4-1W+, T6 changed to DNI
- R43/R44/R51 changed to 0R, R45/R46/R52 changed to DNI
- R47/R48/R67 changed to DNI, R49/R50/R68 changed to 0R

2. Oscilloscope set to 50R for each port.

3. RF (RF0 port) : 1960MHz, -1.95dBm

LO (LO IP port) : 1950MHz, -1.25dBm





# Test 3 (2/3)

## SW Settings :

1. Control SW set to "EXT VCO/LO", "Polyphase Filter" and "BWSEL=0".

ADRF6820 Engineering

BWSEL	Gain	BW
0	High	High
1	High	Low
2	Low	High
3	Low	Low

Key Settings:

- BWSEL:** 0 (Red box)
- BB\_BIAS:** 10 mA
- Polyphase Filter:** Polyphase Filter F (Red box)
- VCO\_SEL:** EXT VCO/LO (Red box)
- PFD FREQ (MHz):** 38.4 (Yellow box)
- VCO FREQ (MHz):** 4000 (Yellow box)
- PLL REF IN (MHz):** 153.6 (Green box)
- PLL REF DIVIDER:** DIV4 (Green box)
- LO FREQ (MHz):** 2000 (Green box)
- STEP SIZE (kHz):** 25 (Green box)
- STEP SIZE MULT:** 1 (Green box)

Register Write Log:

```

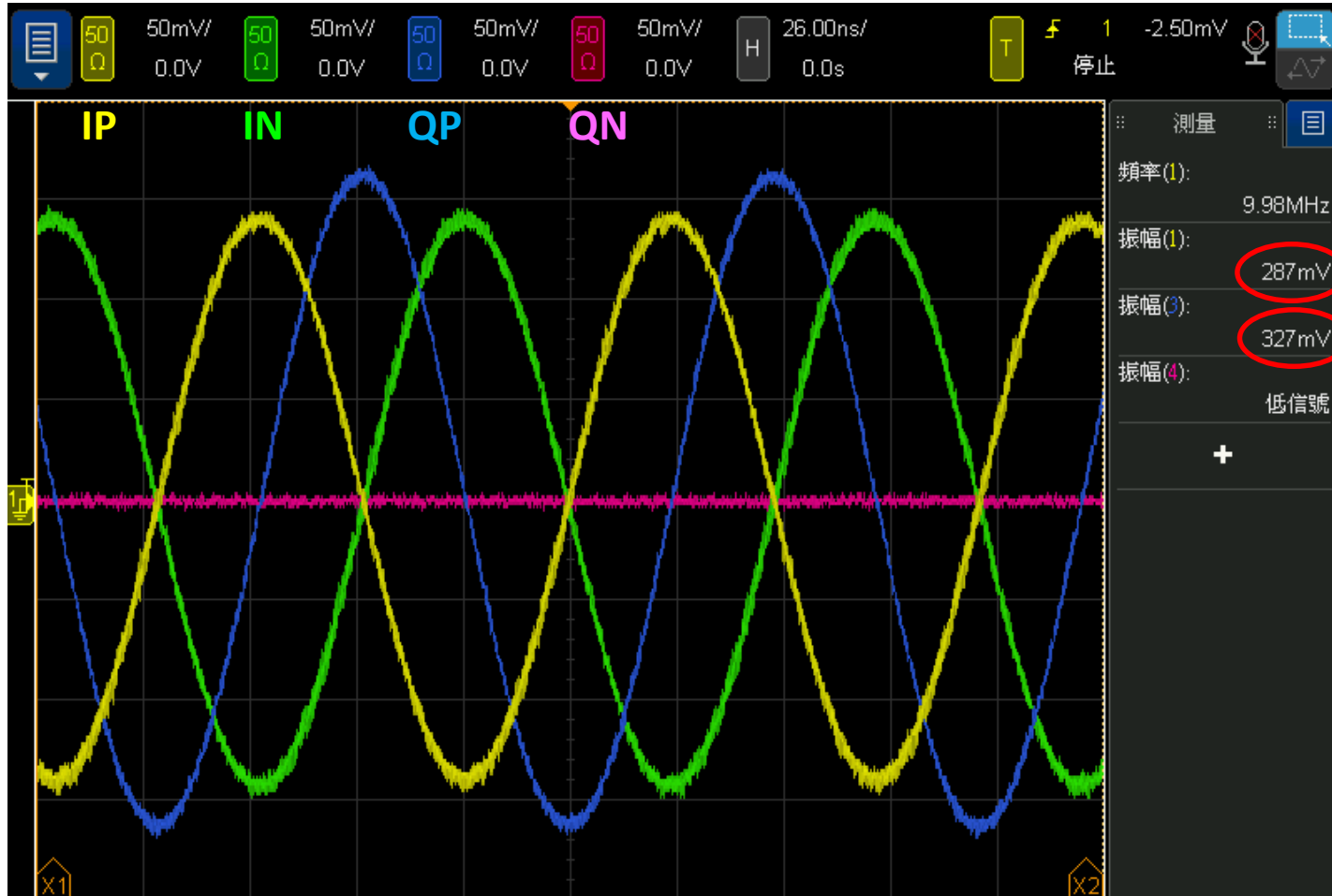
0x05:0x0000
0x01:0xde7f
0x01:0xde7f
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x05:0x0000
0x20:0x0026
0x20:0x0026
0x05:0x0000
0x05:0x0000
0x21:0x0003
0x22:0x0002
    
```

Buttons: Update GUI, Save Register File, Open Register File, Clear



# Test 3 (3/3)

## IQ Output



# Test 4 (1/3)

## HW Settings :

### 1. I path returned to EVB setting (using 1:1 transformer TC1-1-13M+)

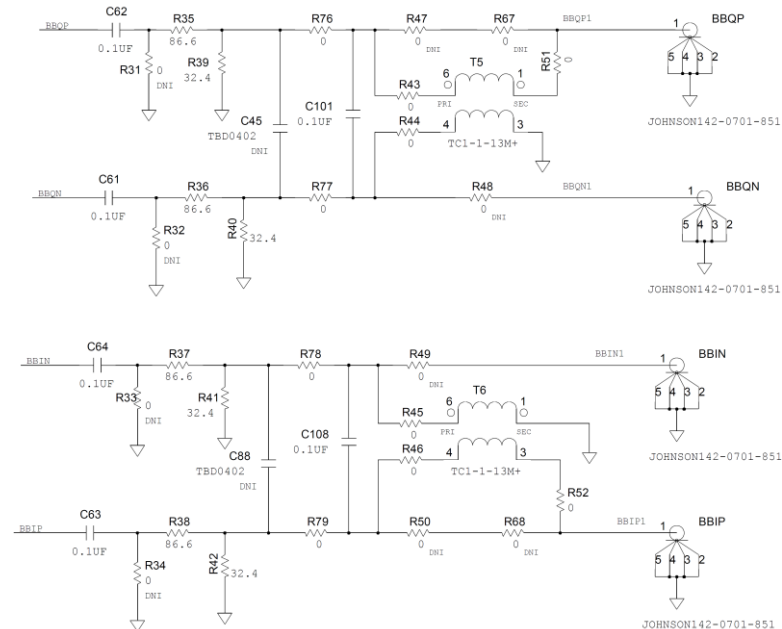
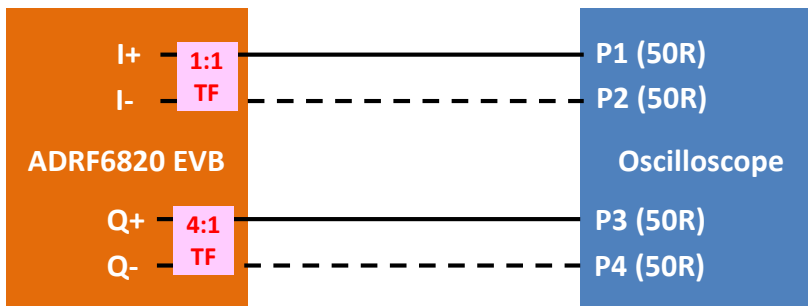
and Q path used a 4:1 impedance transformer (TC4-1W+).

- R35/R36 changed to 0R, R37/R38 changed to 86.6R
- R39/R40 changed to DNI, R41/R42 changed to 32.4R
- R43/R44/R45/R46/R51/R52 changed to 0R
- R47/R48/R49/R50/R67/R68 changed to DNI
- C45/C88/C101/C108 changed to DNI
- T5 changed to TC4-1W+, T6 changed to TC1-1-13M+

### 2. Oscilloscope set to 50R for each port.

3. RF (RF0 port) : 1960MHz, -1.95dBm

LO (LO IP port) : 1950MHz, -1.25dBm



# Test 4 (2/3)

## SW Settings :

1. Control SW set to "EXT VCO/LO", "Polyphase Filter" and "BWSEL=0".

ADRF6820 Engineering

BWSEL	Gain	BW
0	High	High
1	High	Low
2	Low	High
3	Low	Low

PLL Reference Input  
PLL REF IN (MHz) 153.6  
PLL REF DIVIDER DIV4

Charge Pump  
CSCALE 500 uA  
BLEED up 93.75 u  
ABLDLY 0 nsec  
CPCTRL PFD  
CLKEDGE Div \, Ref \

Register Write Log  
0x05:0x0000  
0x01:0xde7f  
0x01:0xde7f  
0x05:0x0000  
0x05:0x0000  
0x05:0x0000  
0x05:0x0000  
0x20:0x0026  
0x20:0x0026  
0x05:0x0000  
0x05:0x0000  
0x21:0x0003  
0x22:0x0002

Update GUI  
Save Register File  
Open Register File  
Clear

# Test 4 (3/3)

## IQ Output

