










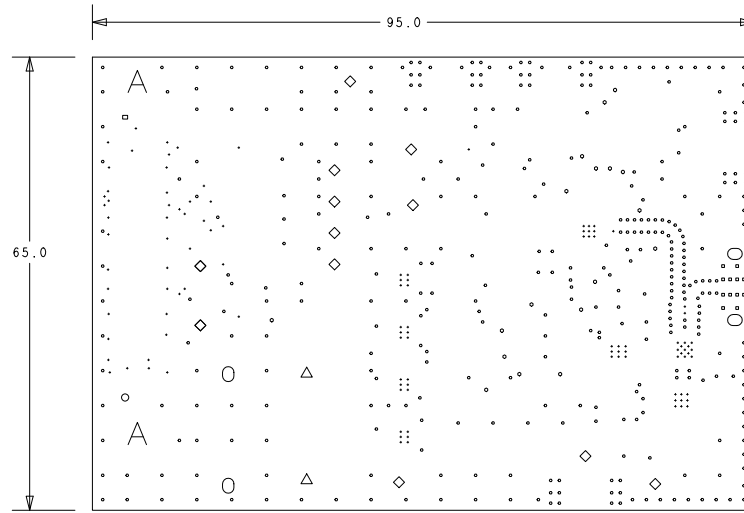


PRIMARY SIDE

REVISION			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	25/08/15	R.Brennan

4 LAYER ROGERS R04003C/FR4 COMBINATION STACKUP
50 OHM IMPEDANCE CONTROLLED STACKUP (1.6mm +/- 10%)

1.6mm +/- 10%		Primary Side Silkscreen
		Primary Side Soldermask
		Primary side 53um (1.5oz) Finished Copper
		0.2032mm (ROGERS R4003C 8mil core 0.5oz/0.5oz) Er 3.38
		0.018 (0.5oz) Copper
		FR4 Prepreg
1.6mm +/- 10%		0.018 (0.5oz) Copper
		0.2032mm (ROGERS R4003C 8mil core 0.5oz/0.5oz) Er 3.38
		Secondary side 53um (1.5oz) Finished Copper
		Secondary Side Soldermask
		Secondary side Silkscreen



Fabrication Drawing

FABRICATION NOTES:

- Material: Four layer, R04003C/FR4 combination - See stackup diagram above. Board to be fabricated per IPC-6012A, CLASS 2.
- Plated thru holes and conductive pattern electroplated with 0.255mm min. thick copper. Terminal areas and plated thru holes to be ENIG plated.
- Processing tolerance:
 - A. Conductive pattern front to back registration within 0.125mm total.
 - B. Minimum annular ring surrounding holes 0.05mm.
 - C. Finished conductive pattern to be within 0.05mm of true size.
 - D. Minimum feature size 0.1mm
 - E. Minimum air gap 0.15mm
- Warp and twist within 0.1875mm per 25mm (0.75%)
- Dimensions are for the finished part.
- SOLDERMASK: liquid Photo Imageable soldermask over bare copper (SMOBC), colour GREEN both sides using the pattern provided. No mask is permitted on the terminal areas. Soldermask to etch registration within 0.125mm total.
- SCREENING: Screen component outlines and nomenclature using indelible white ink on both sides. Nomenclature shall be legible. Screen to etch registration within 0.15mm total.
- Electrically test 100%.
- Break all sharp edges 0.35mm Radius max.
- The stackup and trace/gap widths are designed to achieve 50-ohm impedance controlled traces on Layer 1 using "Grounded Co-Planar Waveguide" technology.
 - Trace Width: 0.381mm traces on Layer 1 (Component Side).
 - Trace/Copper gap: 0.310mm
 - Dielectric Material - 0.008" Rogers 4003C
 - Er of Material: 3.38
- The bare board manufacturer shall provide proof of measurement of impedance
- Manufacturer UL and Date codes on the bottom side as soldermask relief as indicated.

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	FINISHED SIZE	PLATED	QTY
.	0.254	PLATED	114
-	0.4064	PLATED	14
-	0.4064	PLATED	363
-	0.508	PLATED	18
o	0.9906	PLATED	2
o	1.6002	PLATED	12
Δ	1.905	PLATED	2
o	2.1082	PLATED	2
o	2.159	PLATED	2
-	0.7112	NON-PLATED	1
o	1.0922	NON-PLATED	1
A	3.175	NON-PLATED	2

HOLE TOLERANCE
UNLESS SPECIFIED
PLATED: +/- 0.0762mm
NON PLATED: +/- 0.0254mm

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX +/- .010 +/- .1/32 +/- 2 ° ± .005	FABRICATION		ANALOG DEVICES		ANALOG INC. Raheen Business Park Raheen, LIMERICK IRELAND	
	MATERIAL	APPROVAL DRAWN BY P. Daignan DESIGNED Dean Young CHECKED	DATE 13/10/17 13/10/17	TITLE EV-ADF41513SD2Z		
FINISH	APPROVED WFO ENGINEER	SIZE C	FSCM NO	DRAWING NUMBER 09-048052-01	REV A	
DO NOT SCALE DWG		SCALE NTS		SHEET 1 OF 1		