Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers

by Kagan Kaya

INTRODUCTION

Radio frequency (RF) and microwave amplifiers deliver optimum performance when their biasing is well controlled. The quiescent current established by the biasing circuitry affects critical performance metrics such as linearity and efficiency. While some amplifiers are self biased, many devices require external biasing using multiple supplies that must be sequenced properly for safe operation.

This application note provides an overview of bias sequencing requirements and the effects of using various biasing schemes. It presents an elegant solution for biasing amplifiers using active bias controllers such as the HMC980, HMC980LP4E, HMC981, HMC981LP3E, HMC920LP5E.

TABLE OF CONTENTS

REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Change to Figure....7
Change to Figure....8
Change to Figure....9
Change to Figure....13

7/2016—Revision 0: Initial Version

AMPLIFIER BIASING

POWER SUPPLY SEQUENCING

Power supply sequencing is critical when operating externally biased amplifiers for a number of reasons:

- Failing to follow the proper power supply sequencing can result in damage. Exceeding breakdown voltage levels can result in instant failure. Long term reliability degrades when out-of-bound conditions are repeated multiple times. In addition, continually violating the sequencing pattern damages the on-chip protection circuitry and can result in long term damage, which can result in a failure during field operation.
- Optimizing the bias level not only during power up and power down but also during regular operation can improve the performance of the RF amplifier, depending on the configuration and the application requirements.

Analog Devices, Inc. offers a wide selection of RF amplifiers. Many of these devices are designed on depletion mode, pseudo-morphic, high electron mobility transfer (pHEMT) technology. The transistors used in this process typically require voltage supplies for the drain pins and gate pins. This quiescent drain current is a function of the gate voltage. See Figure 1 for the IV characteristics of a typical field effect transistor (FET) process.

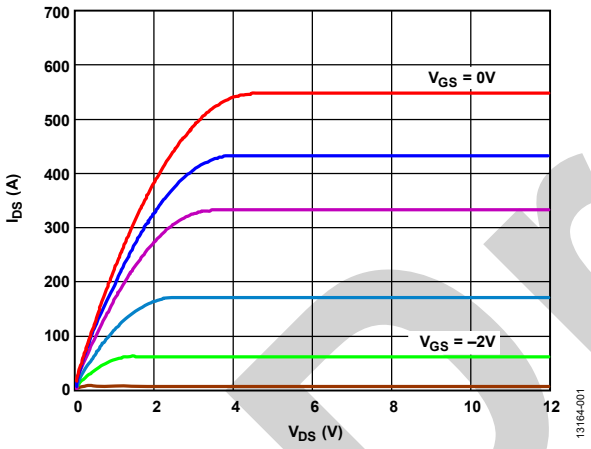


Figure 1. Typical IV Characteristics of a Typical FET Process

As the gate to source voltage (V_{GS}) increases, more electrons enter the channel, resulting in a higher drain to source current (I_{DS}).

Additionally, as the drain to source voltage (V_{DS}) increases, the drain to source current also increases (in the linear region) due to the higher field force pulling the electrons.

In real-world amplifiers, due to effects like channel length modulation, these amplifiers can be broadly categorized into two categories: self biased and externally biased amplifiers.

SELF BIASED AMPLIFIERS

Self biased amplifiers have an internal circuit that sets the optimal bias point suitable for operation. These amplifiers tend to be best suited for broadband, low powered applications. See Figure 2 for a typical pinout of a self biased amplifier.

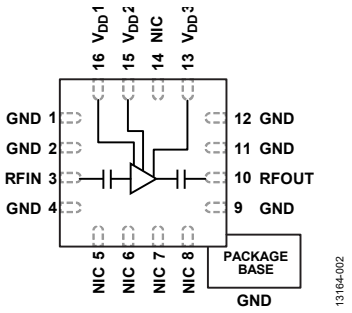


Figure 2. Typical Pinout for a Multistage Self Biased Amplifier with Multiple Bias Pins

EXTERNALLY BIASED AMPLIFIERS

Externally biased amplifiers tend to provide higher performance than self biased amplifiers under specific bias conditions. The quiescent drain current of the amplifier affects parameters such as power compression point, gain, noise figure, intermodulation products, and efficiency. For these high performance externally biased amplifiers, correctly sequencing the supplies is crucial for safe and optimal performance.

This procedure also applies to some other radio frequency integrated circuits (RFICs), such as frequency multipliers, upconverters, and downconverters. These products require similar biasing techniques.

Figure 3 shows the typical connections for the pins of an externally biased amplifier and the corresponding transistor pins. The pin mapping in Figure 3 is a simplified representation of the amplifier.

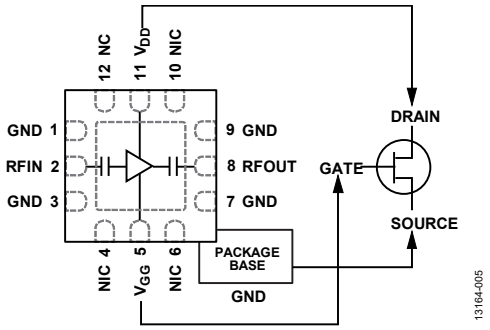


Figure 3. Typical Connections of an Externally Biased Amplifier

Many externally biased amplifiers have multiple stages to meet the required gain, bandwidth, and RF power. Figure 4 shows a typical block diagram of the HMC1131, which is a multistage externally biased amplifier.

AMPLIFIER BIASING

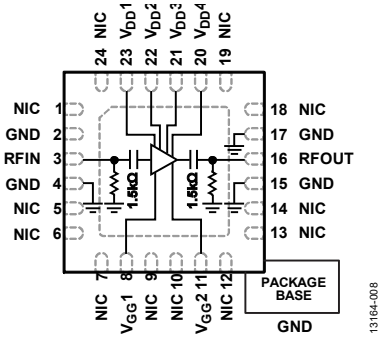


Figure 4. HMC1131 Multistage Externally Biased Amplifier

HMC1131 Biasing and Sequencing Requirements

The HMC1131 is a gallium arsenide (GaAs), pHEMT, monolithic microwave integrated circuit (MMIC), medium power amplifier. It operates from 24 GHz to 35 GHz. The 4-stage design typically provides a 22 dB gain, 23 dBm output power for 1 dB compression (P1dB), and 27 dBm saturated output power (P_{SAT}) under the bias conditions of V_{DD} = 5 V and I_{DQ} = 225 mA, where V_{DD} is the drain bias voltage and I_{DQ} is the quiescent drain current. The electrical specifications table of the HMC1131 data sheet, for the 24 GHz to 27 GHz frequency range, gives this information. Figure 4 shows the pin connections of the HMC1131.

To achieve a target quiescent drain current (I_{DQ}) of 225 mA, set the voltage of the gate bias pins ($V_{GG}1$ and $V_{GG}2$) between 0 V and −2 V. To set that negative voltage without damaging the amplifier, follow the recommended biasing sequence during power up and power down.

The recommended bias sequence during power up for the HMC1131 is the following:

1. Connect to ground.
2. Set $V_{GG}1$ and $V_{GG}2$ to −2 V.
3. Set $V_{DD}1$ through $V_{DD}4$, the drain voltage bias pins, to 5 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to achieve an I_{DQ} of 225 mA.
5. Apply the RF signal

The recommended bias sequence during power down for the HMC1131 is the following:

1. Turn the RF signal off.
2. Decrease $V_{GG}1$ and $V_{GG}2$ to −2 V to achieve an I_{DQ} of approximately 0 mA.
3. Decrease $V_{DD}1$ through $V_{DD}4$ to 0 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to 0 V.

When the gate voltage ($V_{GG}x$) is −2 V, the transistors are pinched off. Therefore, I_{DQ} is typically close to zero.

In general, the recommended biasing sequence is similar for most externally biased amplifiers. I_{DQ}, $V_{DD}x$, and $V_{GG}x$ values are different for different devices. For GaAs devices, V_{GG} is generally set to −2 V or −3 V to turn off the amplifier, while that voltage can be −5 V to −8 V for gallium nitride (GaN) amplifiers. Similarly, $V_{DD}x$ can reach 28 V, even 50 V, for GaN devices, while it is usually less than 13 V for GaAs amplifiers.

In general, for multistage amplifiers, the V_{GG} pins are connected and biased together. By following the same procedure, a user can get the typical performance results provided on the data sheet. Operating the amplifier under different bias conditions may provide different performance.

Figure 5 shows the P1dB vs. the frequency at various supply currents, and Figure 6 shows the output third order intercept (IP3) performance vs. the frequency at various supply currents for the HMC1131.

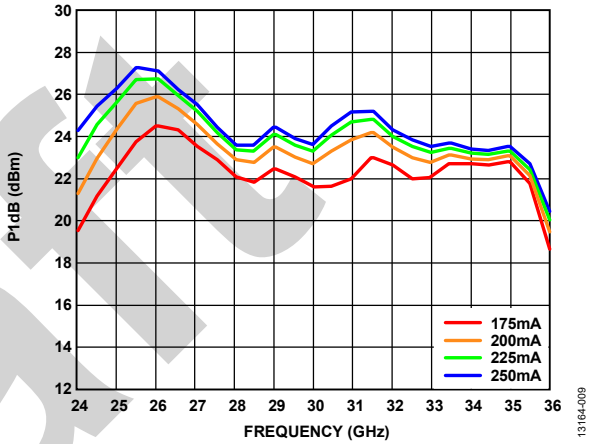


Figure 5. P1dB vs. Frequency at Various Supply Currents

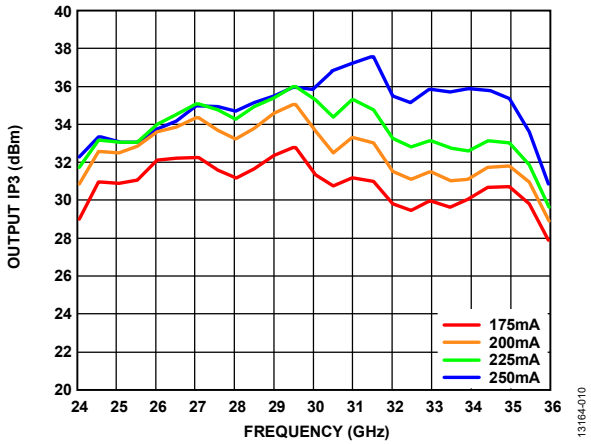


Figure 6. Output IP3 vs. Frequency at Various Supply Currents, P_{OUT}/Tone = 10 dBm

CASCODE AMPLIFIERS

Analog Devices' wideband distributed amplifiers often use a cascode architecture to extend their frequency range. The cascode distributed amplifier uses a fundamental cell of two FETs in series,

AMPLIFIER BIASING

source to drain. This fundamental cell is duplicated a number of times. This duplication increases the operation bandwidth. Figure 7 shows a simplified schematic for the fundamental cell.

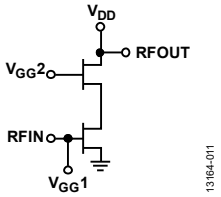


Figure 7. Simplified Fundamental Cascode Cell Schematic

With some exceptions, these cascode-based wideband amplifiers are externally biased.

The HMC637A is a wideband amplifier that uses this cascode topology. The HMC637A is a GaAs, MMIC, metal semiconductor field effect transistor (MESFET) distributed power amplifier that operates between dc and 6 GHz. Figure 8 shows the pin connections for the HMC637A.

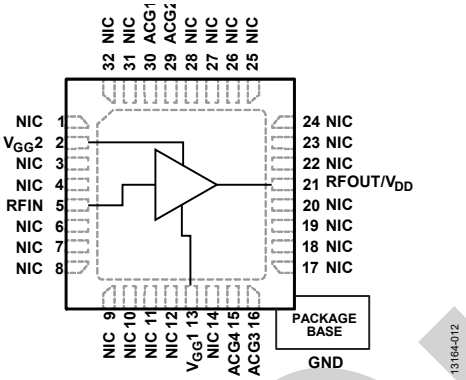


Figure 8. HMC637A Pin Connections

The amplifier provides 14 dB of gain, 43 dBm of output IP3, and 30.5 dBm of output power at a 1 dB gain compression under the bias conditions of V_{DD} = 12 V, $V_{GG}2$ = 6 V, and I_{DQ} = 400 mA. The electrical specifications table of the HMC637A data sheet provides more information.

To achieve the recommended quiescent drain current of 400 mA, $V_{GG}1$ must be somewhere between 0 to −2 V. To set the desired negative voltage, follow the recommended bias sequence during power up and power down.

The recommended bias sequence for the HMC637A during power up follows:

1. Connect to ground.
2. Set $V_{GG}1$ to −2 V.
3. Set V_{DD} to 12 V.
4. Set $V_{GG}2$ to 6 V ($V_{GG}2$ can be generated using a resistor divider derived from V_{DD}).
5. Increase $V_{GG}1$ to achieve a typical quiescent current (I_{DQ}) of 400 mA.
6. Apply the RF signal.

The recommended bias sequence for the HMC637A during power down follows:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −2 V to achieve I_{DQ} = 0 mA.
3. Decrease $V_{GG}2$ to 0 V.
4. Decrease V_{DD} to 0 V.
5. Increase $V_{GG}1$ to 0 V.

USING ACTIVE BIAS CONTROLLERS TO BIAS DEPLETION MODE RF AMPLIFIERS

There are two popular approaches used to externally bias RF amplifiers:

- Constant Gate Voltage Biasing. In this approach, the gate voltage is set to achieve the desired quiescent current (I_{DQ}). This gate voltage value is then kept constant during operation, which typically results in a variable drain current (I_{DD}) under the RF drive.
- Constant Drain Current Biasing. In this approach, the gate voltage value is varied to achieve the desired drain current. The drain current is monitored and the gate voltage is adjusted to main a constant drain current for different RF drive levels. This technique is generally referred to as Active Bias Control.

Another approach, a subset of the constant drain current approach. This consists of following the constant I_{DD} approach and switching in between multiple constant I_{DD} levels when necessary due to various field scenarios. For instance, a user might bias a power amplifier for high current levels during rainy weather to compensate for the additional rain attenuation. Similarly, a user might bias the same power amplifier for low current levels during clear weather to reduce the power consumption.

Analog Devices RF amplifiers are generally characterized with a constant gate voltage, using bench top power supply units.

Designing bias circuits for amplifiers that keep the drain current constant and provide necessary sequencing can be cumbersome. Such control circuits are complicated and require not only multiple external components such as low drop out regulators (LDOs), charge pumps, voltage sequencing, and protection circuits, but also calibration cycles. Such implementations can occupy a large printed circuit board (PCB) area that is often much larger than the amplifier itself.

The HMC981LP3E, HMC980LP4E, and HMC920LP5E are 3 mm × 3 mm, 4 mm × 4 mm, and 5 mm × 5 mm plastic packaged active bias controllers. Figure 9 shows the PCB area required for a typical application, including external passive components.

AMPLIFIER BIASING

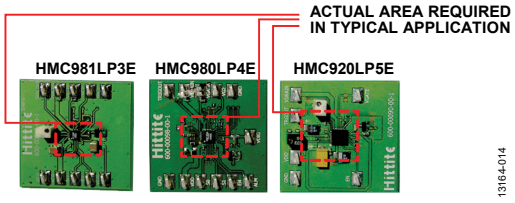


Figure 9. PCB Area Required in Typical Application

The Analog Devices active bias controller family offers some key benefits:

- Internal voltage generators generate the required negative voltage required by depletion mode amplifiers. These generators eliminate the need for external negative voltage inverters and reduce external component count, PCB space and system cost.
- Continuous gate voltage adjustment ensures a constant RF Amplifier drain current.
- Bias accuracy improves due to the reduction of device to device variation effects. The gate voltage required to obtain a desired drain current will vary from part to part. Active bias controllers adjust the gate voltage level separately for each individual device and reduce the performance difference introduced by device to device variation.
  - Figure 10 and Figure 11 show typical variations in drain current when constant gate voltage and constant drain current biasing are used. The plots indicate that constant drain current biasing results is smaller part-to-part variation in drain current and lower drift of the drain current vs temperature.

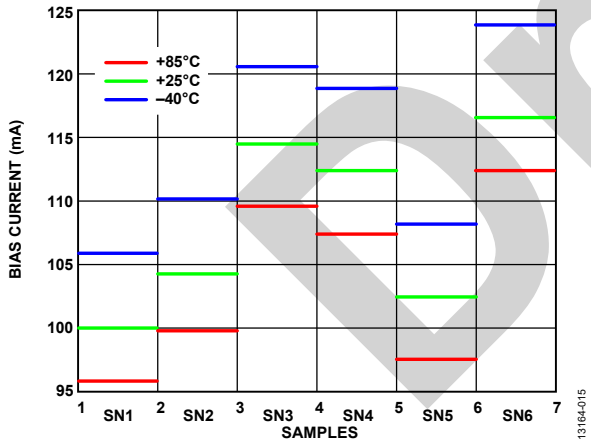


Figure 10. Typical Part-to-Part Drain Current Variation of an RF Amplifier with constant gate voltage bias (6 devices)

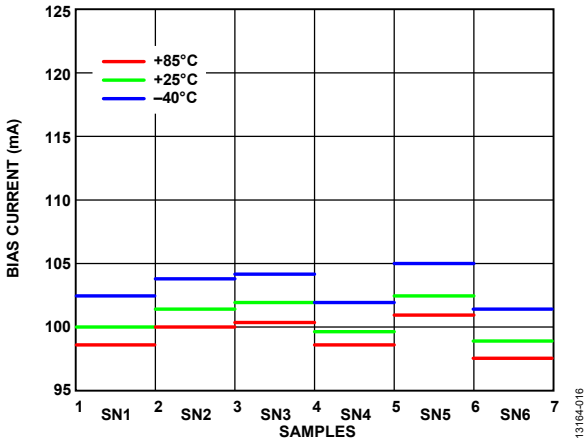


Figure 11. Typical Part-to-Part Drain Current Variation of an RF Amplifier with constant drain current bias control from HMC920LP5E (6 devices)

AMPLIFIER BIASING

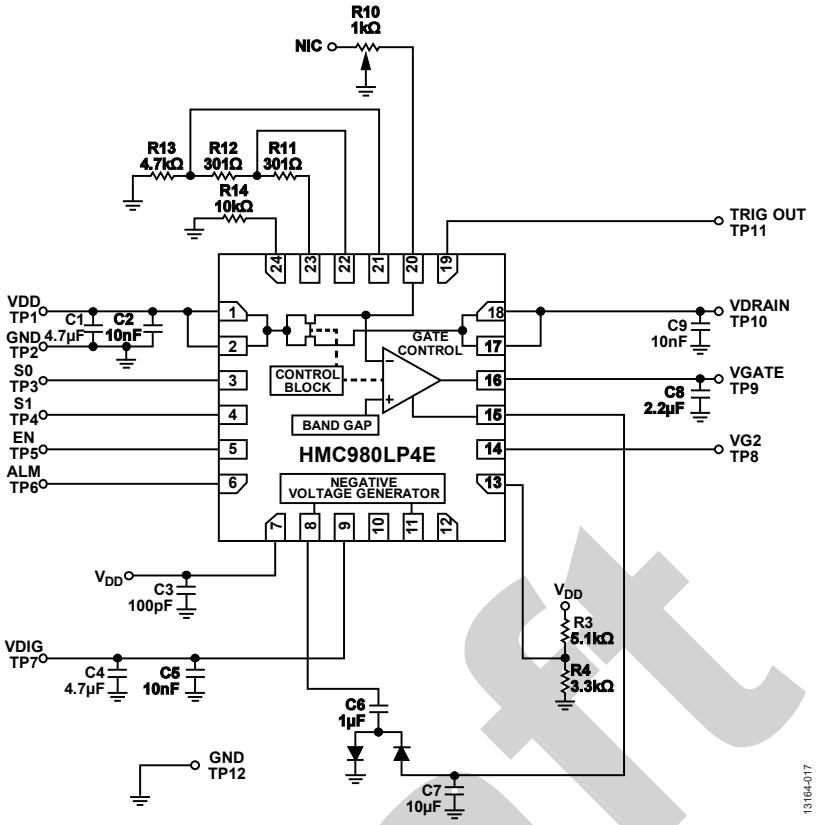


Figure 12. Typical Application Circuit for the HMC980LP4E

Table 1. Selected Features of Active Bias Controllers

Device Number	Supply Range (V)	VDRAIN (V)	IDRAIN (mA)	IGATE (mA)	Over/Under Current Alarm	Short-Circuit Protection	VDRAIN LDO	Negative Voltage Generator
HMC920LP5E	5 to 16.5	3 to 15	0 to 500	−4 to +4	Yes	Yes	Yes	Yes
HMC980LP4E	5 to 16.5	5 to 16.5	50 to 1600	−4 to +4	Yes	Yes	No	Yes
HMC981LP3E	4 to 12	4 to 12	20 to 200	−0.8 to +0.8	No	Yes	No	Yes

With an internal feedback loop, the gate voltage varies to maintain a constant drain current through the amplifier under bias, independent of the temperature and amplifier threshold variations. The drain current setpoint is adjusted with an external resistor. Figure 12 shows the R_{SENSE} resistor (R10) connected to Pin 20 of the HMC980LP4E.

Further details on how to calculate the R_{SENSE} and V_{DD} values can be found on the active bias controller data sheets.

Analog Devices offers three active bias controllers: HMC920LP5E, HMC980LP4E, and HMC981LP3E. Table 1 details selected features of these active bias controllers.

The HMC980LP4E provides the ability to source high drain currents, while the HMC981LP3E is best suited for devices that require lower drain currents. In addition to the negative voltage generator, the HMC920LP5E integrates a positive voltage regulator, providing the ability to source drain pins.

OPERATING PRINCIPLES

For externally biased amplifiers, Analog Devices data sheets highlight the biasing requirements for V_{GG} and IDD at the bottom of electrical specifications table. For instance, the HMC637A requires its VGG1 pin to be adjusted from −2 V to 0 V to obtain a typical IDQ of 400 mA. In addition, the recommended power-up and power-down sequencing must be followed to avoid damaging the part.

The HMC980LP4E employs integrated control circuitry to manage safe power-up and power-down sequencing.

During power up, the VDD and VDIG supplies of the bias controller turn on (VDIG should turn on before VDD), and then the voltage on VNEG is generated by the internal negative voltage generator (NVG). V_{NEG} starts to decrease and stops when it reaches its default value (typically −2.46 V). The V_{GATE} output voltage also starts to decrease, following V_{NEG}. Once V_{NEG} = −2.46 V and V_{GATE}

AMPLIFIER BIASING

= −2.1 V, the VDRAIN output pin is enabled, and V_{GATE} begins to increase toward 0 V to until the setpoint IDD value is reached.

Similar power-down protection circuitry also provides safe power down. During power down, the VGATE output pin always shuts down after VDD, even if there is a short circuit on the VDD pins or on the VGG pins of the amplifier. This feature introduces advanced protection of the amplifier, under excessive drain current scenarios.

ADJUSTING THE DEFAULT VNEG AND VGATE THRESHOLD (STOPPED EDITING AT THE END OF THIS SECTION) VALUES

The default value for V_{NEG} (−2.46 V), is seen in Figure 13. Due to the internal logic that exists inside HMC980LP4E, this value of the VNEG voltage limits the HMC980LP4E's VGATE output voltage range. With the default configuration, the typical VGATE output swing is in between −2.1 V and 0 V, that is, there approximately 400 mV of headroom between V_{NEG} and the most negative voltage that V_{GATE} can reach.

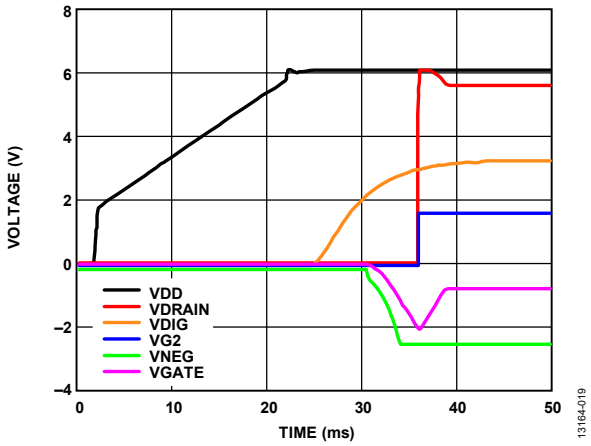


Figure 13. Default VNEG Value

For some RF amplifiers, gate voltages that are more negative than −2.1 V are required. Also, some RF amplifiers have a gate voltage absolute maximum rating (AMR) that is greater (more positive) than −2.1 V. The default value of VNEG (-2.46 V) and the VGATE threshold value (VGATE_THRESHOLD = -2.1V) can be adjusted using external resistors (R5, R6, R7 and R8) as shown in Figure 14 (VGATE_THRESHOLD is the voltage at which the negative going VGATE reaches its most negative value and starts tending positive).

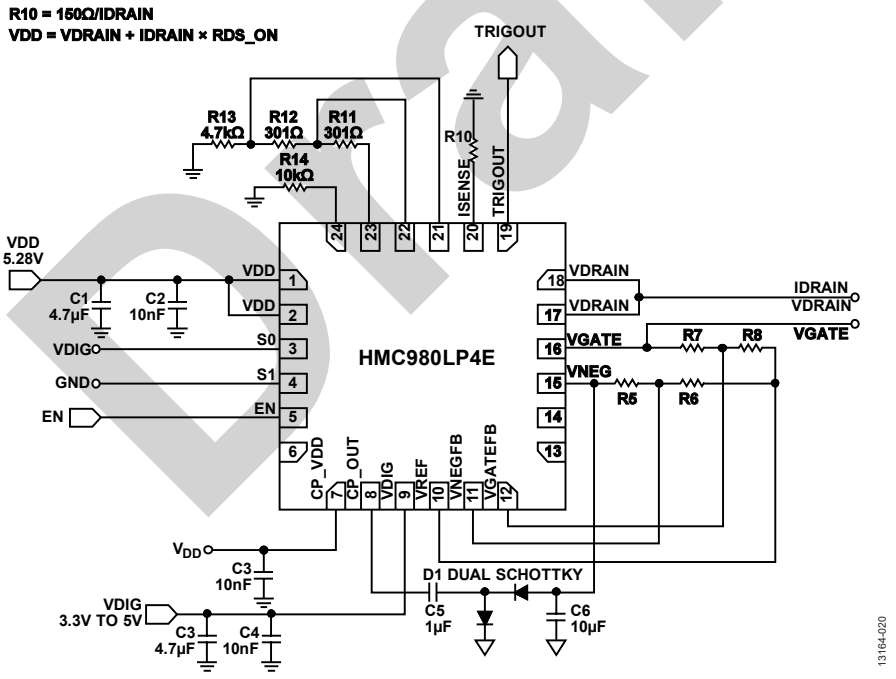


Figure 14. External Resistors for Adjusting Default VNEG and VGATE Values

VNEG can be either decreased or increased. As VNEG is adjusted, the value of VGATE_THRESHOLD must also be adjusted and should be at least 0.3 V greater (more positive) than VNEG. For example, if VNEG is going to be reduced to -2.5V, VGATE_THRESHOLD should be reduced to -2.2 V or greater (more positive). The external resistors for setting VNEG and VGATE_THRESHOLD are set according to the following equations.

If the desired VNEG < −2.46 V

R5 (kΩ) = open

AMPLIFIER BIASING

R6 (kΩ) = 50/(50 × (V_{NEG} − 0.815)/(262 × (0.815 − 1.44)) − 1).

R7 (kΩ) = open

R8 (kΩ) = 50/(50 × ($V_{GATE\_THRESHOLD}$ − 0.815)/(262 × (0.815 − 1.44)) − 1).

For example, if the desired V_{NEG} = −3.2 V, $V_{GATE\_THRESHOLD}$ should be = −2.9 V,

R6 = 221 kΩ,

R8 = 372 kΩ, and

R5 = R7 = open.

If the desired V_{NEG} > −2.46 V,

R6 (kΩ) = open.

R5 (kΩ) = 262/(262 × (1.44 − 0.815)/(50 × (0.815 − V_{NEG})) − 1),

R8 (kΩ) = open.

R7 (kΩ) = 262/(262 × (1.44 − 0.815)/(50 × (0.815 – $V_{GATE\_THRESHOLD}$)) − 1),

For example, if the desired VNEG = −1.5 V, $V_{GATE\_THRESHOLD}$ should be set to = −1.2 V,

R5 = 631 kΩ,

R7 = 419 kΩ, and

R6 = R8 = open.

REDUCING THE RISE TIME OF THE V_{GATE} VOLTAGE

A delay exists between the moment that the enable signal reaches the enable pin of the active bias controller and the moment that the voltage level at the RF amplifier's VGATE input pin settles to the desired value. This delay is due to the combination of the internal propagation delay of the bias controller and the settling time of the V_{GATE} voltage. The V_{GATE} settling time is affected by the shunt capacitors used on the connection between the active bias controller's VGATE output pin and the RF amplifier's VGATE input pin. The HMC980LP4E typical enable waveform (see Figure 15) shows a V_{GATE} settling time of greater than 1 ms.

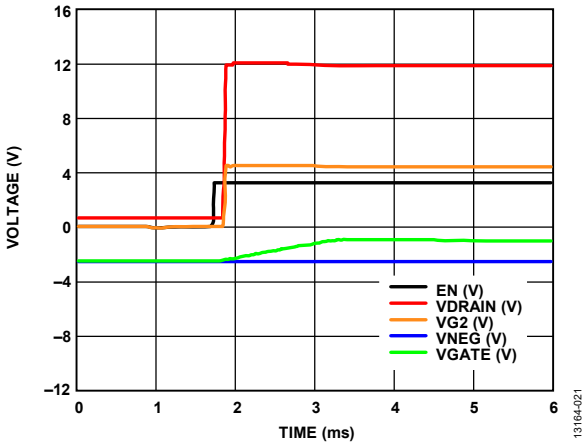


Figure 15. HMC980LP4E Typical Enable Waveform

The external circuitry affects the gate rise time but not the propagation delay. Figure 16 shows a typical connection between the HMC980LP4E and an RF amplifier. Generally, a shunt capacitor is added to the VGG pins. For stability, a resistor is sometimes placed in series with this capacitor in (R1 in Figure 16)

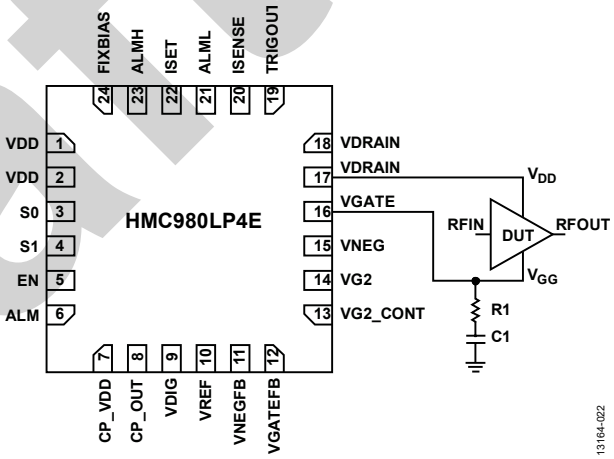


Figure 16. VGATE Connection Circuitry Between the HMC980LP4E and the DUT

When C1 = 10 µF and R1 = 0 Ω, the typical rise time is greater than 1.5 ms (see Figure 17). Reducing C1 to 1 µF reduces the rise time to 131 µs (see Figure 18).

AMPLIFIER BIASING

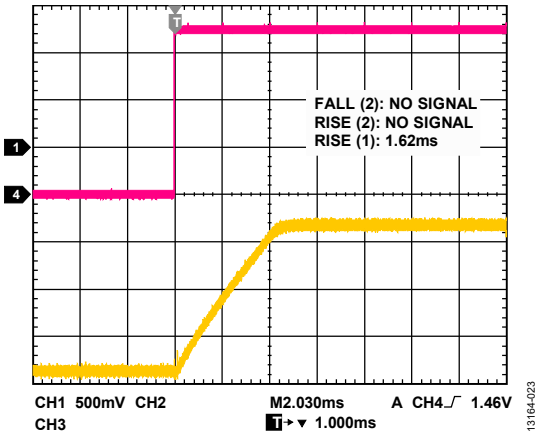


Figure 17. Typical VGATE Rise Time with C1 = 10 µF

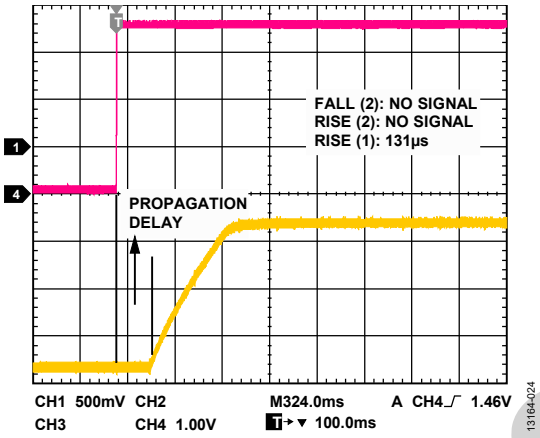


Figure 18. Typical VGATE Rise Time with C1 = 1 µF

When C1 = 100 nF, the V_{GATE} rise time is reduced to 15.5 µs, but the signal has overshoot and ringing (see Figure 19). Adding a series resistor, R1, with a value of 68 Ω to C1 = 100 nF improves the response and keeps the rise time within a similar level (see Figure 20).

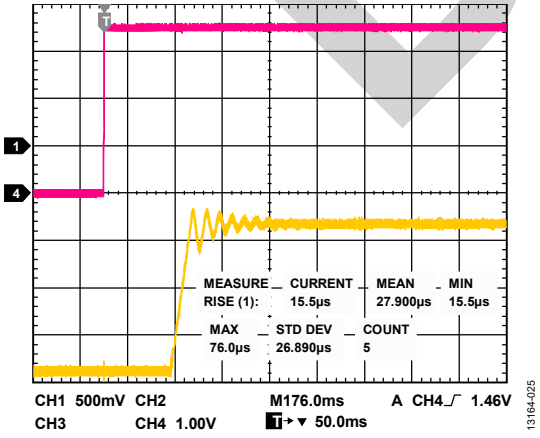


Figure 19. Typical V_{GATE} Rise Time with C1 = 100 nF

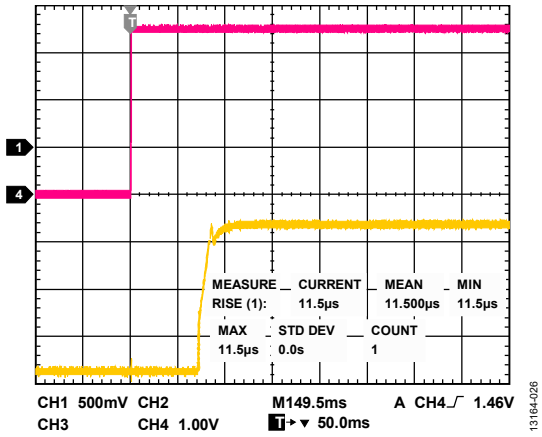


Figure 20. Typical V_{GATE} Rise Time with C1 = 100 nF and R1 = 68 Ω

DAISY-CHAIN OPERATION

Where multiple active bias controllers are controlling multiple cascaded RF amplifiers, they can be used in a daisy-chain configuration. The TRIGOUT output of the active bias controller activates when the V_{DRAIN}, V_{G2}, and V_{GATE} output voltages settle. Using the TRIGOUT signal to enable another bias controller with the enable pin (EN), improves system safety. A daisy-chain configuration has many applications, Figure 21 and Figure 22 show two applications. The number of amplifier stages and bias controllers can be increased.

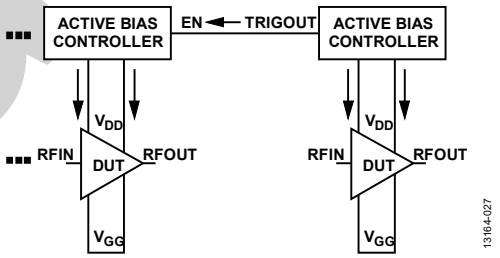


Figure 21. Daisy-Chain Configuration with Two Amplifiers in Cascade Configuration

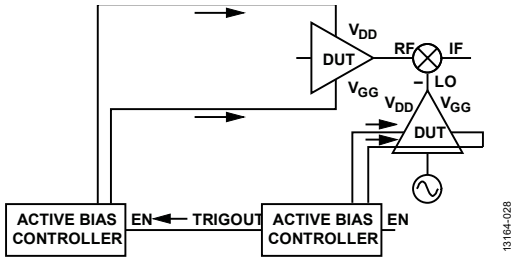


Figure 22. Daisy-Chain Configuration Where Amplifiers Are in Different Signal Paths

Figure 23 shows the V_{DRAIN} and V_{GATE} responses of two active bias controllers in a daisy-chain configuration, powering two amplifiers individually. The second bias controller is enabled by the trigger

AMPLIFIER BIASING

signal from the first bias controller. This architecture ensures that the second amplifier enables after the first.

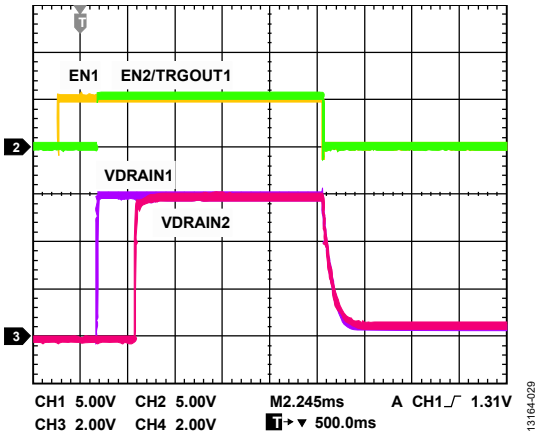


Figure 23. V_{DRAIN} Responses of Two Active Bias Controllers in a Daisy-Chain Configuration, Powering Two Amplifiers Individually

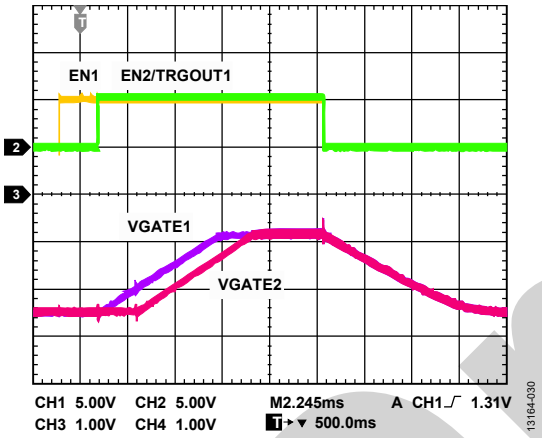


Figure 24. V_{GATE} Responses of Two Active Bias Controllers in a Daisy-Chain Configuration, Powering Two Amplifiers Individually

TESTING THE FUNCTIONALITY OF AN ACTIVE BIAS CONTROLLER

Without the active bias controller connected to an RF amplifier, it is difficult to test the device's full functionality. However some useful diagnostic checks can be carried on out the stand-alone device.

- When IDD = 0 mA, there should be a a negligible voltage drop across between the VDD input pin and the VDRAIN output pin. Therefore, V_{DRAIN} should be almost equal to V_{DD}.
- VNEG is typically −2.46 V.
- VGATE hits a maximum value of VNEG + 4.5 V, which is typically 2.04 V.

These numbers apply to HMC980. For the HMC981 and HMC920 controllers, the correct values can be obtained from the device datasheets.

BIASING MULTIPLE RF AMPLIFIERS WITH A SINGLE ACTIVE BIAS CONTROLLER

It is possible to bias two or more amplifiers using a single active bias controller. To do so, calculate the RSENSE value based on the total combined drain current of the two amplifiers.

Note, however, that using this approach limits the benefits that an active bias controller offers for the following reasons:

- An active bias controller is not able to compensate device-to-device gate voltage variation that is common with GaAs devices. As a result, two devices that are being be biased using one gate voltage, may have different drain currents (the gate voltage will be adjusted so that the combined drain currents are equal to the setpoint current.
- If one of the amplifiers draws excessive current due to a short circuit or other terms of failure, the bias controller shuts down all amplifiers under bias. Although this does not damage the devices, it limits system functionality.

TYPICAL ACTIVE BIAS CONTROLLER APPLICATION CIRCUITS

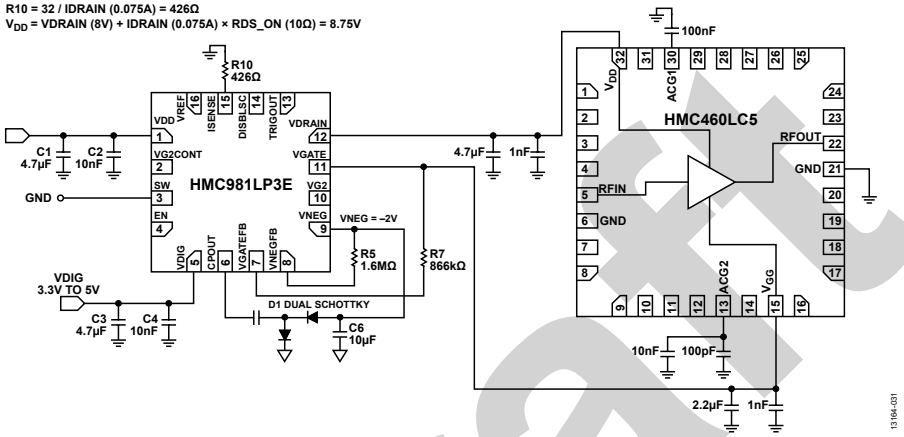
Biasing the HMC460LC5 with the HMC981LP3E

To bias the HMC460LC5 with the HMC981LP3E, do the following:

- Set R10 to 426 Ω to set I_{DD} = 75 mA for the HMC981LP3E. A common resistor value of 430 Ω can be used.
- Calculate a V_{DD} value (8.75 V).
- Use R4 and R6 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC981LP3E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold (stopped editing at the end of this section) Values section for details.
- The shunt V_{GG} capacitor values can be reduced to increase the rise time (see HMC460LC5 in Figure 25). Refer to the Reducing the Rise Time of the VGATE Voltage section for further details.

Figure 25.

AMPLIFIER BIASING



Application Circuit for Biasing the HMC460LC5 with the HMC981LP3E

AMPLIFIER BIASING

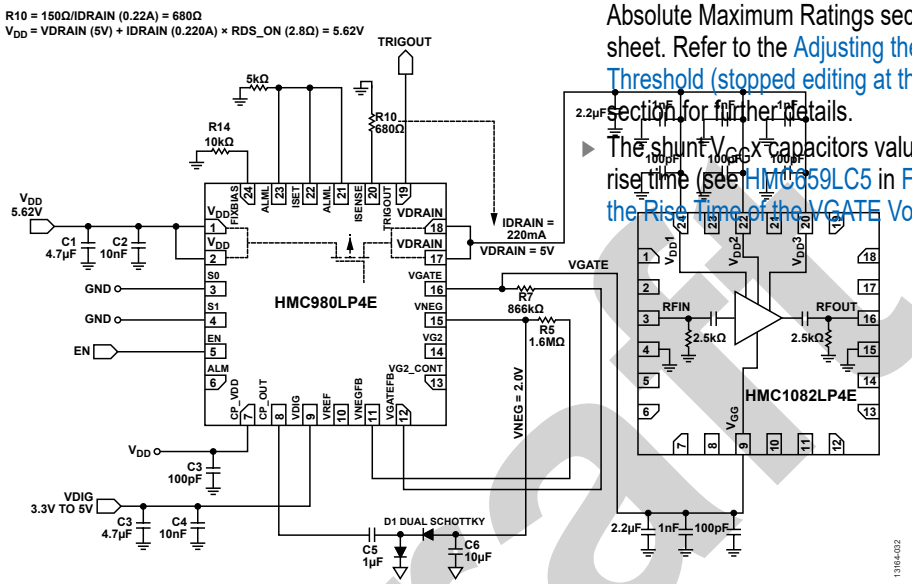
Biasing the HMC1082LP4E with the HMC980LP4E

To bias the HMC1082LP4E with the HMC980LP4E, do the following:

- Set R10 to 680 Ω to set IDD = 220 mA for the HMC980LP4E
- Calculate a V_{DD} value of 5.62 V.
- Use R5 and R7 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC980LP4E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold (stopped editing at the end of this section) Values section for details.
- The shunt VGG capacitor values can be reduced to increase the rise time (see HMC1082LP4E in Figure 26). Refer to the Reducing the Rise Time of the VGATE Voltage section for further details.

Figure 26.

AMPLIFIER BIASING



Application Circuit for Biasing the HMC1082LP4E with the HMC980LP4E

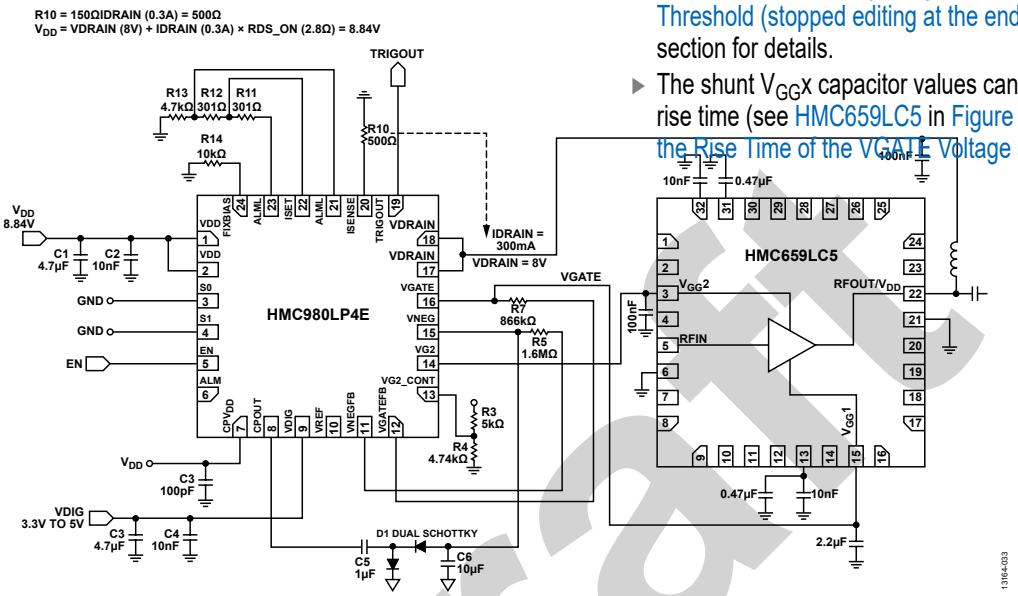
Biasing the HMC659LC5 with the HMC980LP4E

To bias the HMC659LC5 with the HMC980LP4E, do the following:

- Set R10 to 500 Ω to set I_{DD} = 300 mA for the HMC980LP4E.
- Use a common resistor value of 510 Ω.
- Calculate a V_{DD} value of 8.84 V.
- Use R3 and R4 to set $V_{GG}2$ for the HMC980LP4E.
- Use R5 and R7 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC980LP4E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold (stopped editing at the end of this section) Values section for further details.
- The shunt V_{DD}x capacitors value can be reduced to increase the rise time (see HMC659LC5 in Figure 27). Refer to the Reducing the Rise Time of the VGATE Voltage section for further details.

Figure 27.

AMPLIFIER BIASING



Application Circuit for Biasing the HMC659LC5 with the HMC980LP4E

Biasing the HMC659LC5 with the HMC920LP5E

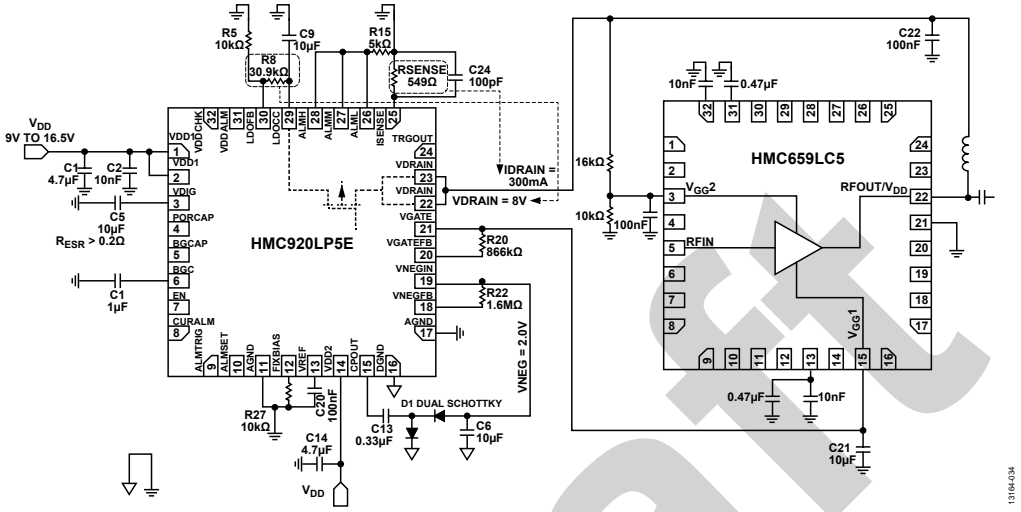
To bias the HMC659LC5 with the HMC920LP5E, do the following:

- Set R_{SENSE} to 549 Ω to set I_{DD} = 300 mA for the HMC920LP5E.
- Set R8 to 30.9 kΩ to set VDRAIN = 8 V.
- Use R20 and R22 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC920LP5E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold (stopped editing at the end of this section) Values section for details.
- The shunt V_{GG}x capacitor values can be reduced to increase the rise time (see HMC659LC5 in Figure 28). Refer to the Reducing the Rise Time of the VGATE Voltage section for further details.

Figure 28.

AMPLIFIER BIASING

Application Circuit for Biasing the HMC659LC5 with the HMC920LP5E



CONCLUSION

Operating RF amplifiers with an active bias controller ensures that the device is sequenced properly and at the desired level, reducing overall system variability.

The active bias controller family from Analog Devices can address the biasing requirements of externally biased RF/ microwave components, such as FETs, amplifiers, multipliers, optical modulator drivers and frequency converters. The gate voltages of the RF amplifiers are adjusted with a closed feedback loop for the desired drain current. The sequencing feature of the VGATE, VDRAIN, and VGG2 output pins of the bias controller during power up and power down ensures that the RF amplifier is protected.