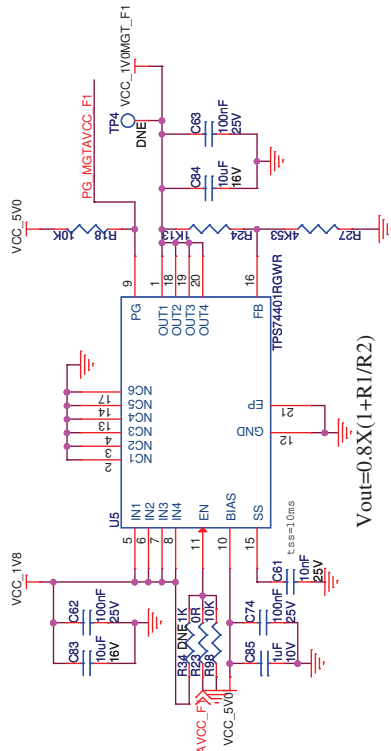
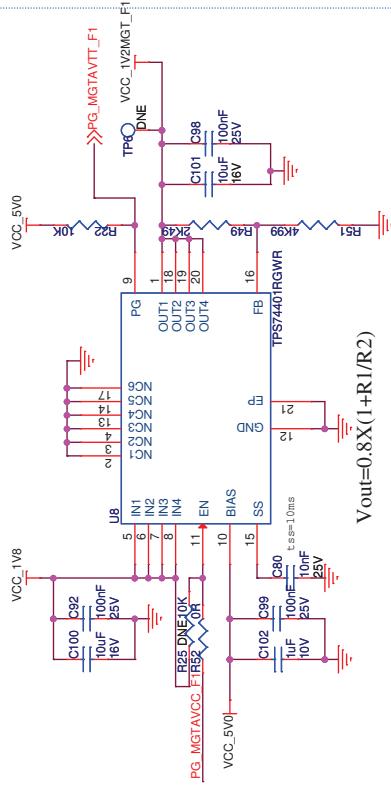


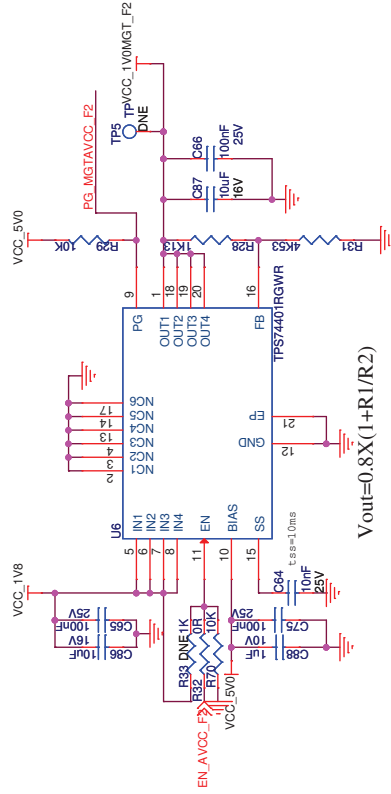
FPGA1 MGTAVCC 1.0V @ 3A



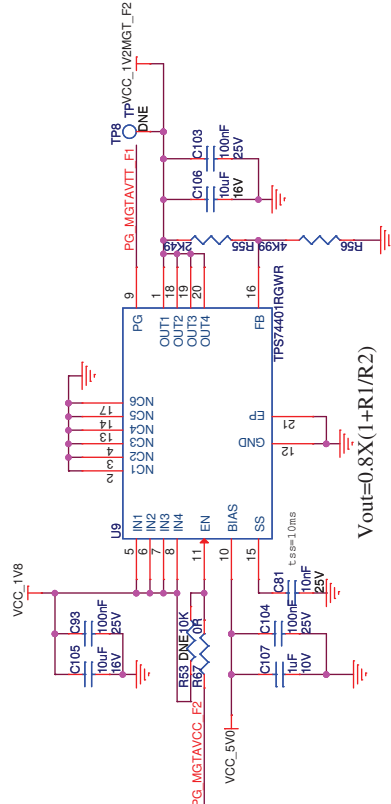
FPGA1 MGTAVTT 1.2V @ 3A



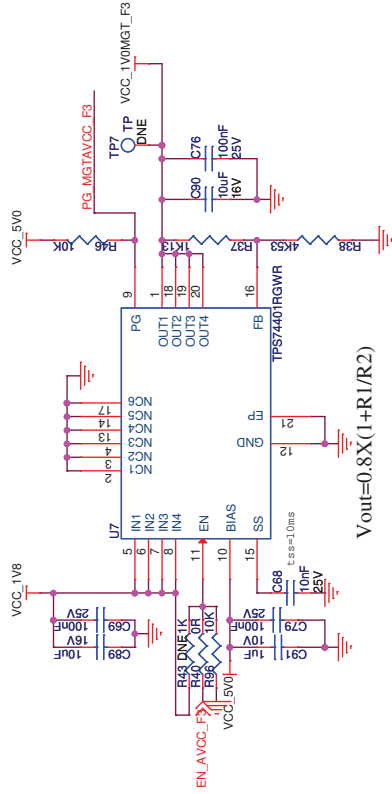
FPGA2 MGTAVCC 1.0V @ 3A



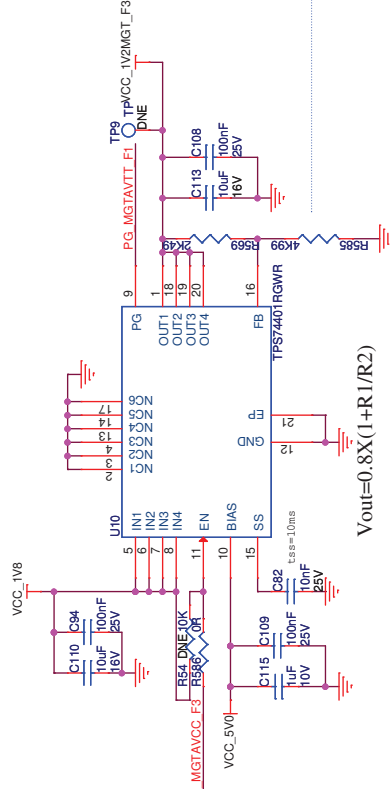
FPGA2 MGTAVTT 1.2V @ 3A



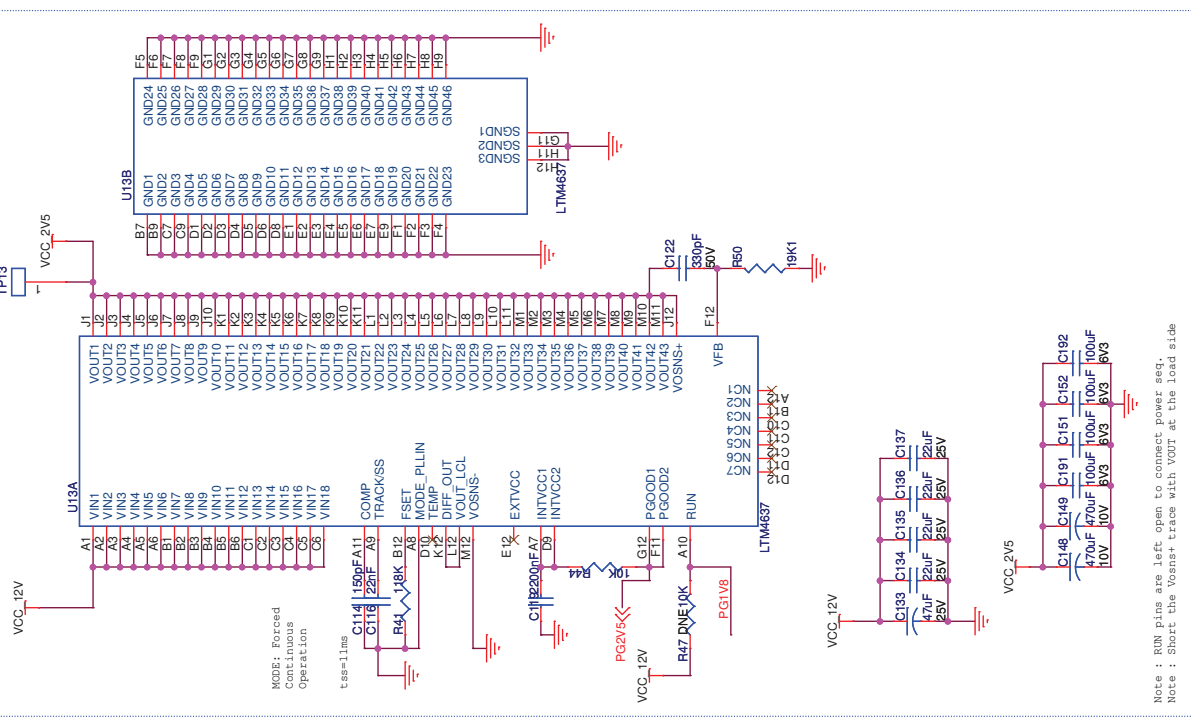
FPGA3 MGTAVCC 1.0V @ 3A



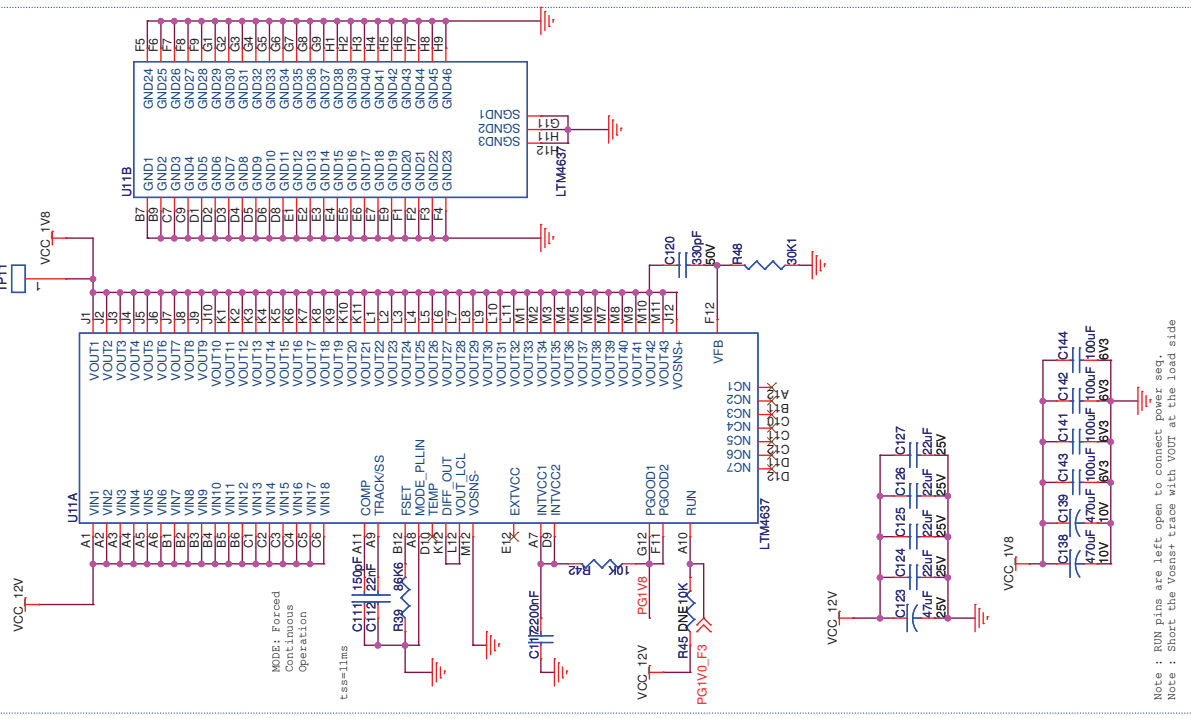
FPGA3 MGTAVTT 1.2V @ 3A



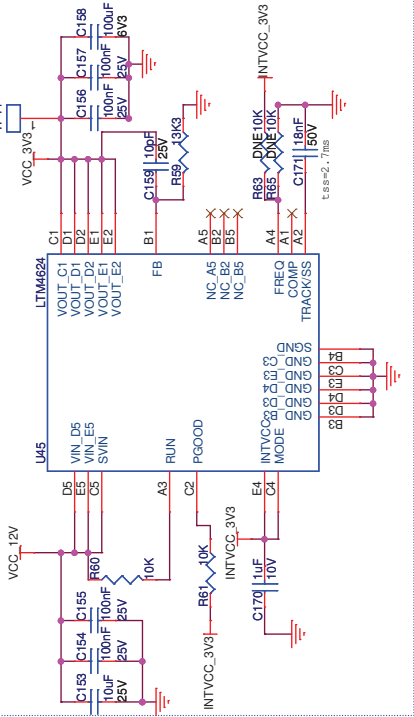
FPGA BANK 2.5V @ 20A



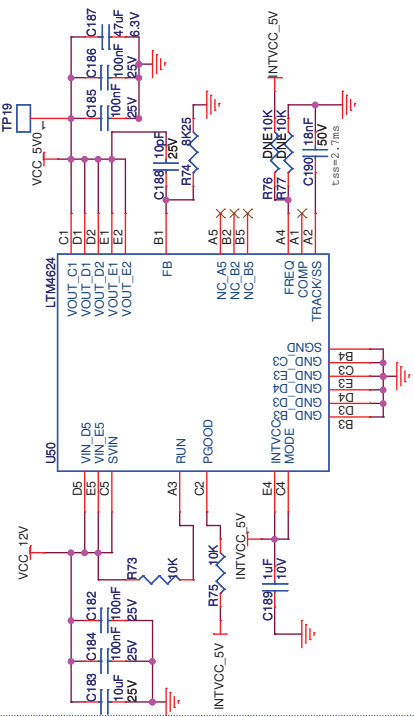
FPGA BANK 1.8V @ 20A



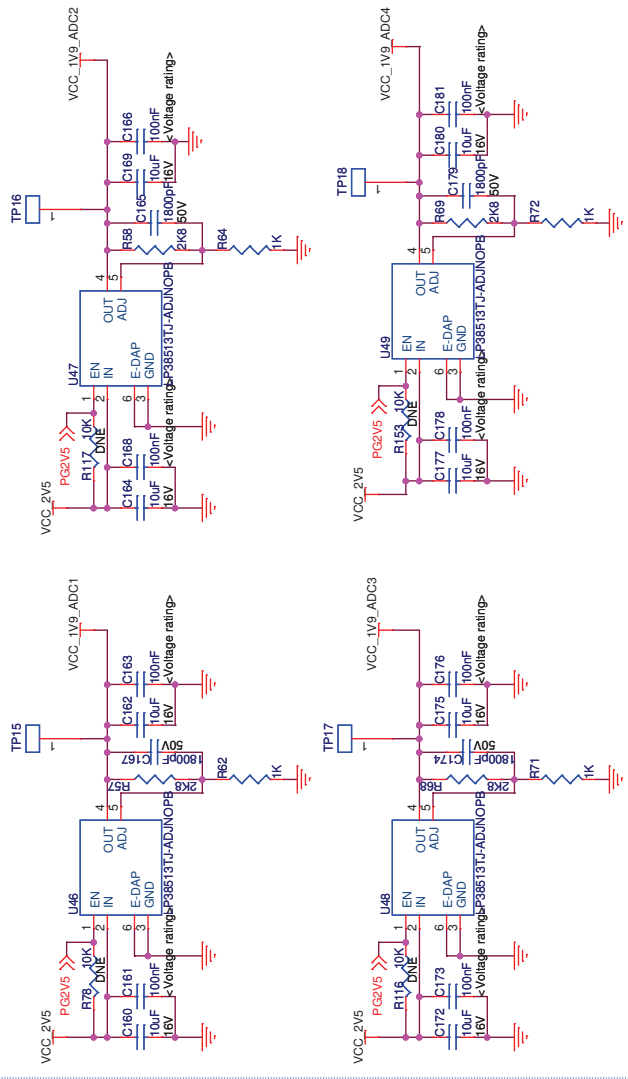
3.3V @ 4A



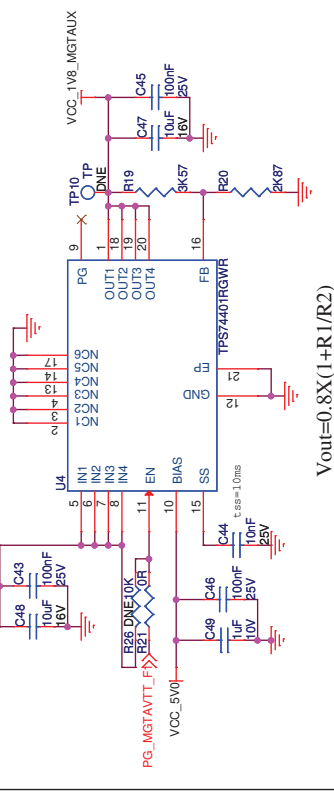
5V @ 4A



VCC_1V9 Generation (ADC)



FPGA MGTAUX 1.8V @ 3A



$$V_{out} = 0.8X(1 + R1/R2)$$