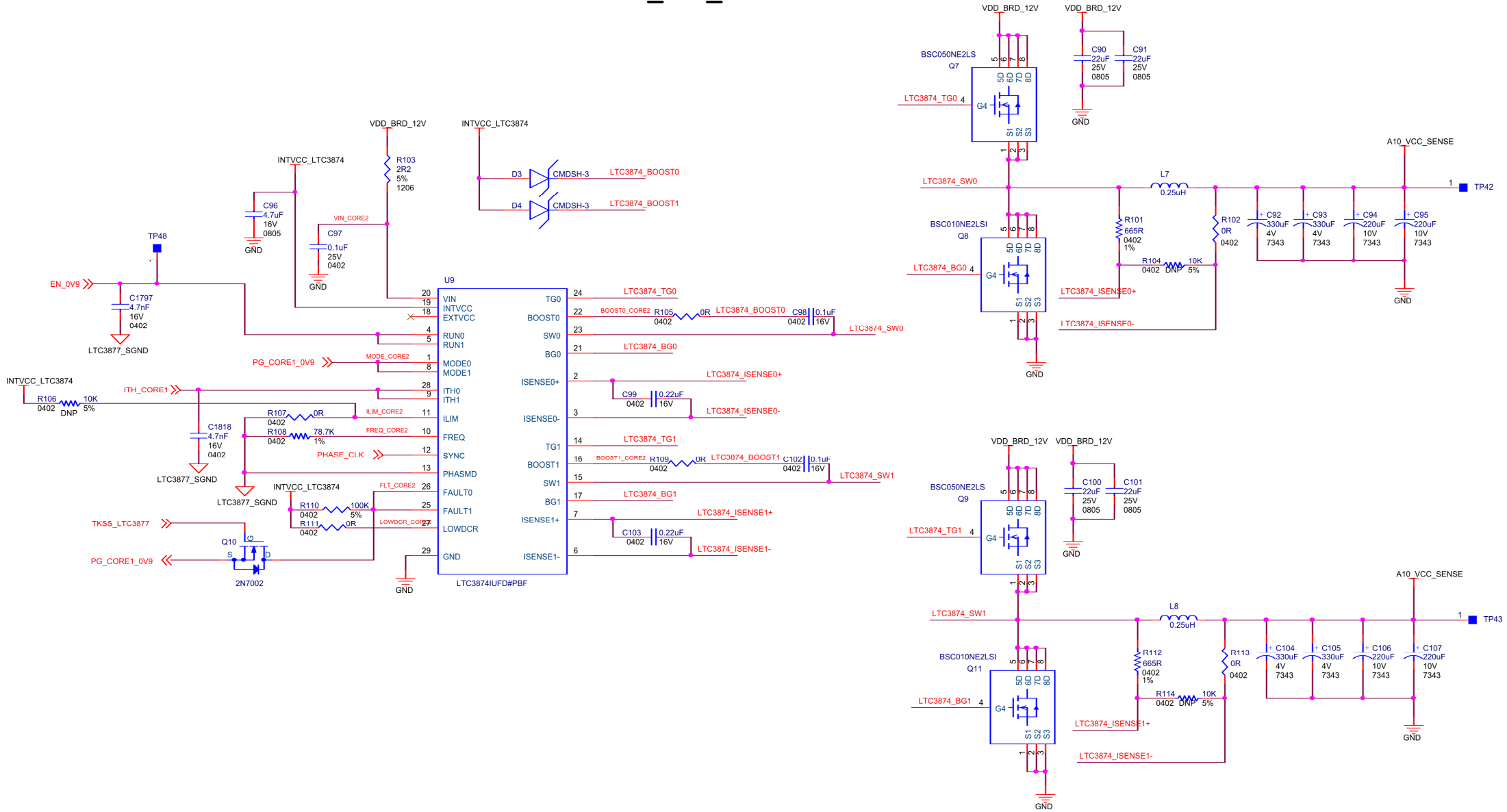


Place R89 and R100 side-by-side on top layer and route as kelvin sense to both resistors equally using star routing through the 1K resistors. The 1K resistors are for limiting eddie current backflow.

Title	FPGA MASTER BOARD	
Size	Document Number	Rev
A3	<Doc>	A
Date:	Tuesday, November 02, 2021	Sheet 10 of 43

A10_0V9_POWER2



Title		
FPGA MASTER BOARD		
Size	Document Number	Rev
A3	<Doc>	A
Date:	Tuesday, November 02, 2021	Sheet 11 of 43