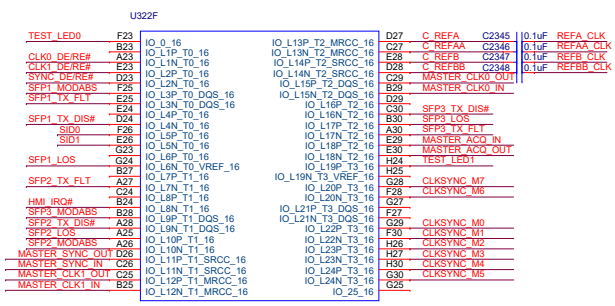
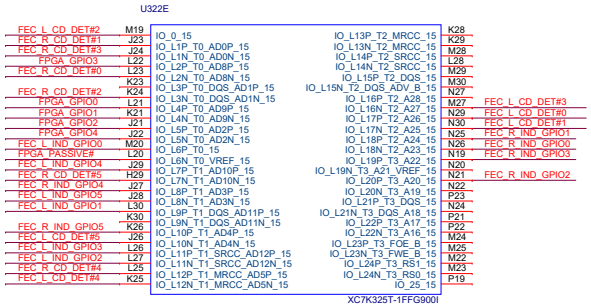
SFP CONTROL, PARALLEL IOS & SYNC CONTROL

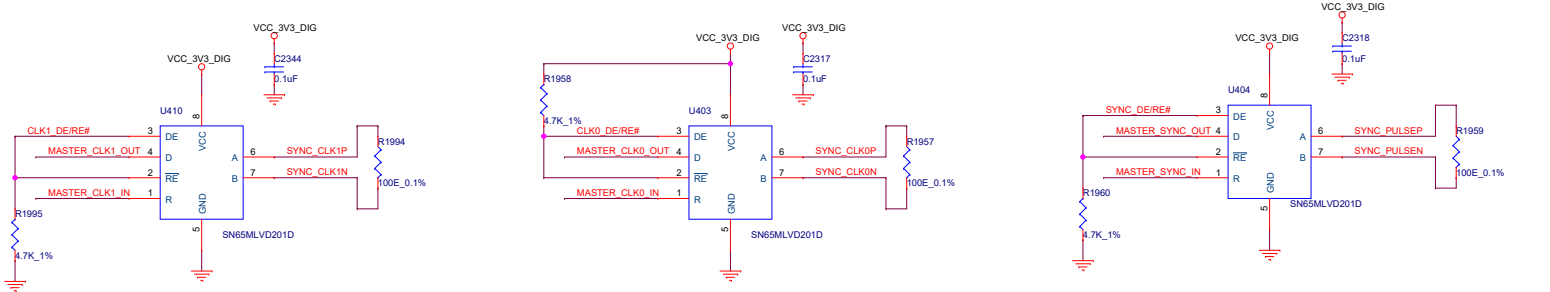
BANK 16 ; VCCO 3V3



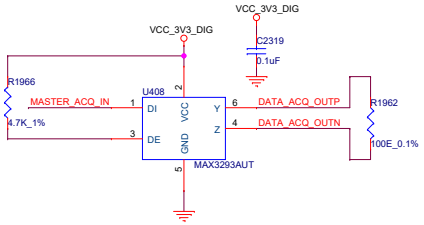
BANK 15 ; VCCO 1V8



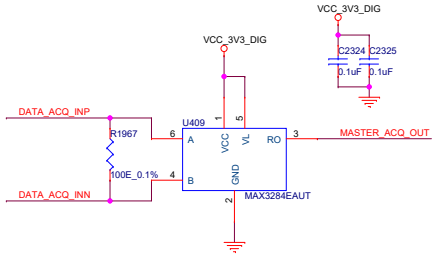
LVDS DRIVER AND RECEIVER



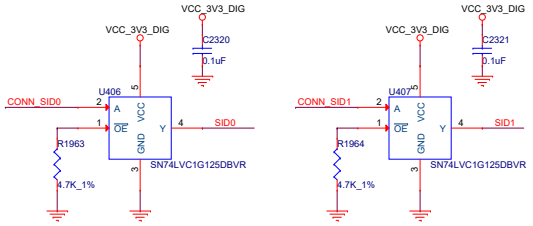
DATA-ACQ TRANSMITTER



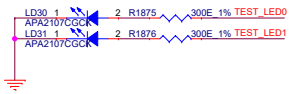
DATA-ACQ RECEIVER



SLOT-ID BUFFERS



Test LEDs



OFF PAGE CONNECTIONS

FEC_L_CD_DET#0 FEC_L_CD_DET#0 [12]
FEC_L_CD_DET#1 FEC_L_CD_DET#1 [12]
FEC_L_CD_DET#2 FEC_L_CD_DET#2 [12]
FEC_L_CD_DET#3 FEC_L_CD_DET#3 [12]
FEC_L_CD_DET#4 FEC_L_CD_DET#4 [12]
FEC_L_CD_DET#5 FEC_L_CD_DET#5 [12]

FEC_R_CD_DET#0 FEC_R_CD_DET#0 [12]
FEC_R_CD_DET#1 FEC_R_CD_DET#1 [12]
FEC_R_CD_DET#2 FEC_R_CD_DET#2 [12]
FEC_R_CD_DET#3 FEC_R_CD_DET#3 [12]
FEC_R_CD_DET#4 FEC_R_CD_DET#4 [12]
FEC_R_CD_DET#5 FEC_R_CD_DET#5 [12]

FEC_L_IND_GPIO5 FEC_L_IND_GPIO5 [12]
FEC_L_IND_GPIO4 FEC_L_IND_GPIO4 [12]
FEC_L_IND_GPIO3 FEC_L_IND_GPIO3 [12]
FEC_L_IND_GPIO2 FEC_L_IND_GPIO2 [12]
FEC_L_IND_GPIO1 FEC_L_IND_GPIO1 [12]
FEC_L_IND_GPIO0 FEC_L_IND_GPIO0 [12]

FEC_R_IND_GPIO5 FEC_R_IND_GPIO5 [12]
FEC_R_IND_GPIO4 FEC_R_IND_GPIO4 [12]
FEC_R_IND_GPIO3 FEC_R_IND_GPIO3 [12]
FEC_R_IND_GPIO2 FEC_R_IND_GPIO2 [12]
FEC_R_IND_GPIO1 FEC_R_IND_GPIO1 [12]
FEC_R_IND_GPIO0 FEC_R_IND_GPIO0 [12]

SFP1_TX_FLT SFP1_TX_FLT [20]
SFP1_MODABS SFP1_MODABS [20]
SFP1_LOS SFP1_LOS [20]
SFP1_TX_DIS# SFP1_TX_DIS# [20]

SFP2_TX_FLT SFP2_TX_FLT [20]
SFP2_MODABS SFP2_MODABS [20]
SFP2_LOS SFP2_LOS [20]
SFP2_TX_DIS# SFP2_TX_DIS# [20]

SFP3_TX_FLT SFP3_TX_FLT [20]
SFP3_MODABS SFP3_MODABS [20]
SFP3_LOS SFP3_LOS [20]
SFP3_TX_DIS# SFP3_TX_DIS# [20]

FPGA_PASSIVE# FPGA_PASSIVE# [12]

FPGA_GPIO0 FPGA_GPIO0 [12]
FPGA_GPIO1 FPGA_GPIO1 [12]
FPGA_GPIO2 FPGA_GPIO2 [12]
FPGA_GPIO3 FPGA_GPIO3 [12]
FPGA_GPIO4 FPGA_GPIO4 [12]

HMI_IRQ# HMI_IRQ# [19]

DATA_ACQ_INP DATA_ACQ_INP [22]
DATA_ACQ_INN DATA_ACQ_INN [22]

DATA_ACQ_OUTP DATA_ACQ_OUTP [22]
DATA_ACQ_OUTN DATA_ACQ_OUTN [22]

SYNC_CLK0P SYNC_CLK0P [22]
SYNC_CLK0N SYNC_CLK0N [22]

SYNC_CLK1P SYNC_CLK1P [22]
SYNC_CLK1N SYNC_CLK1N [22]

SYNC_PULSEP SYNC_PULSEP [22]
SYNC_PULSEN SYNC_PULSEN [22]

CONN_SID0 CONN_SID0 [22]
CONN_SID1 CONN_SID1 [22]

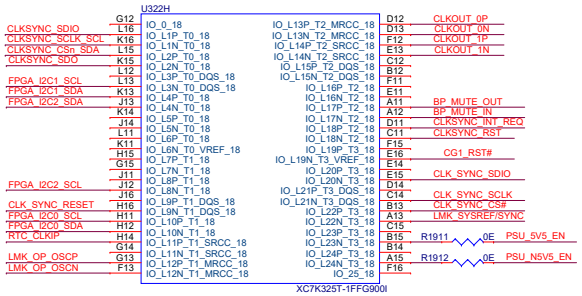
REFA_CLK REFA_CLK [18]
REFAA_CLK REFAA_CLK [18]

REFB_CLK REFB_CLK [18]
REFBB_CLK REFBB_CLK [18]

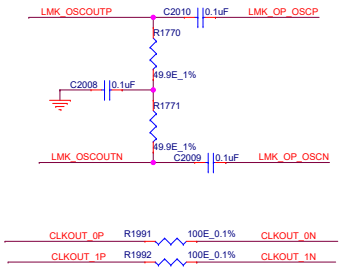
CLKSYNC_M0 CLKSYNC_M0 [18]
CLKSYNC_M1 CLKSYNC_M1 [18]
CLKSYNC_M2 CLKSYNC_M2 [18]
CLKSYNC_M3 CLKSYNC_M3 [18]
CLKSYNC_M4 CLKSYNC_M4 [18]
CLKSYNC_M5 CLKSYNC_M5 [18]
CLKSYNC_M6 CLKSYNC_M6 [18]
CLKSYNC_M7 CLKSYNC_M7 [18]

CLK SYNC CONTROL & I2C INTERFACE

BANK 18; VCCO 3V3

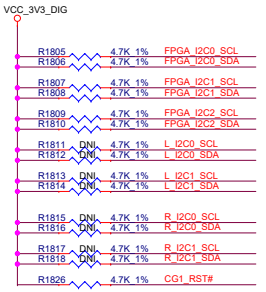


CLOCK TERMINATIONs

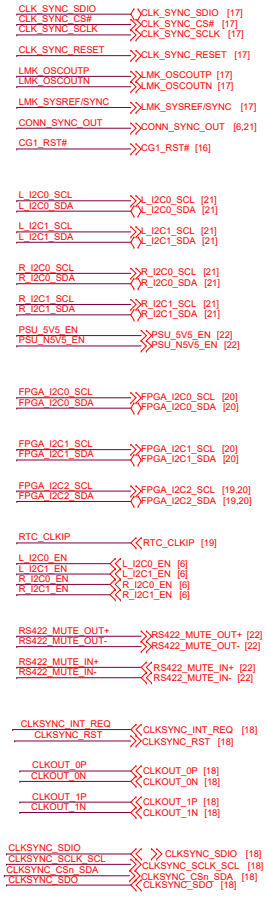


Cad Note: Place the terminations close to FPGA

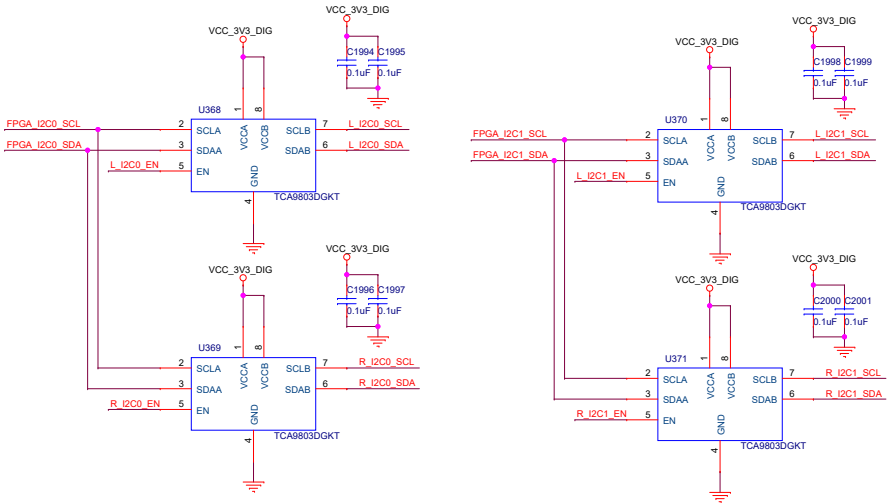
Default Pull- Ups



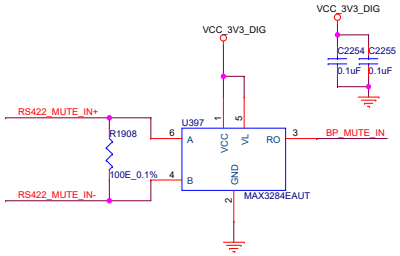
Off- Page Connections



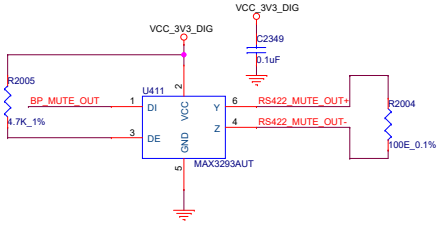
I2C BUFFERS



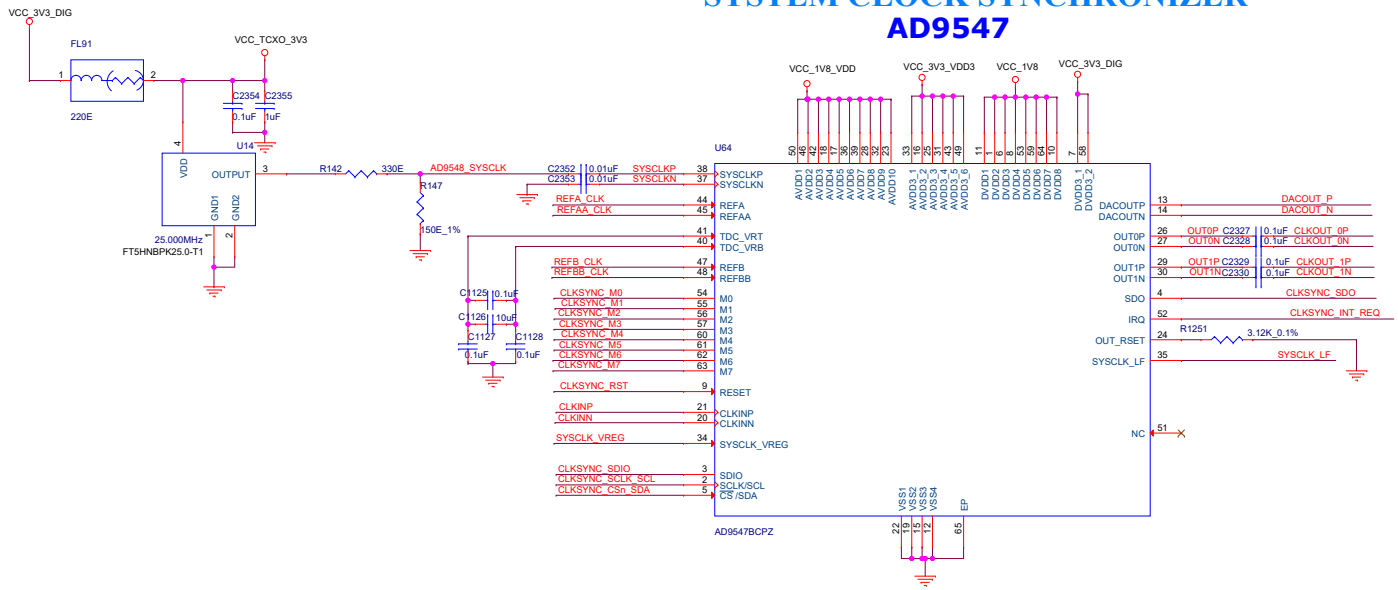
BACKPLANE MUTE IN



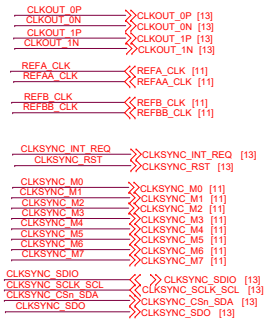
BACKPLANE MUTE OUT



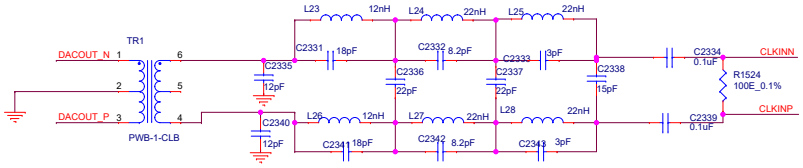
SYSTEM CLOCK SYNCHRONIZER
AD9547

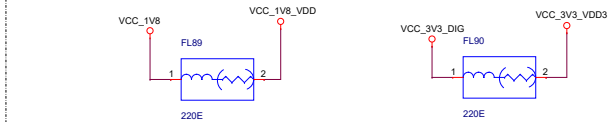


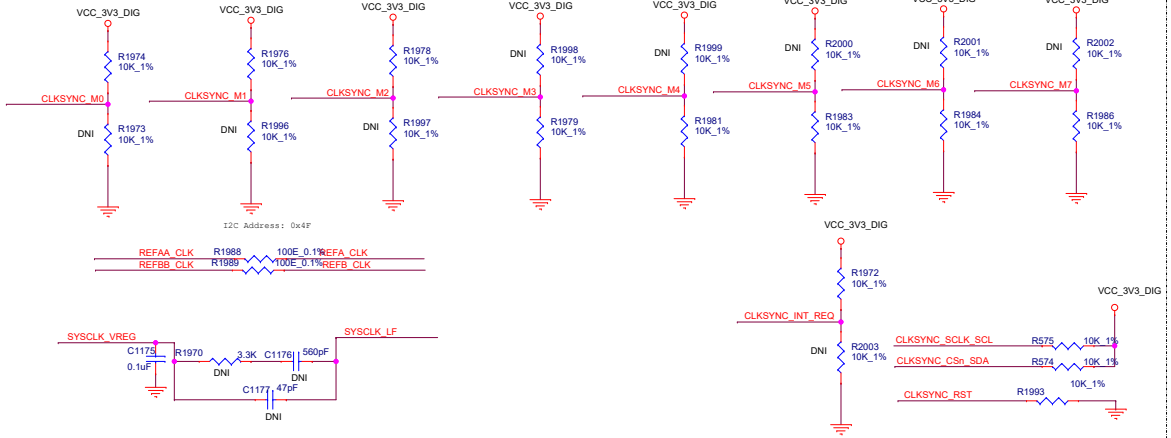
AD9547 Signals



FILTER







DECAPS