09/15/2021

AD9528 PLL1 Lock Status tests

I set the AD9528 as follows:

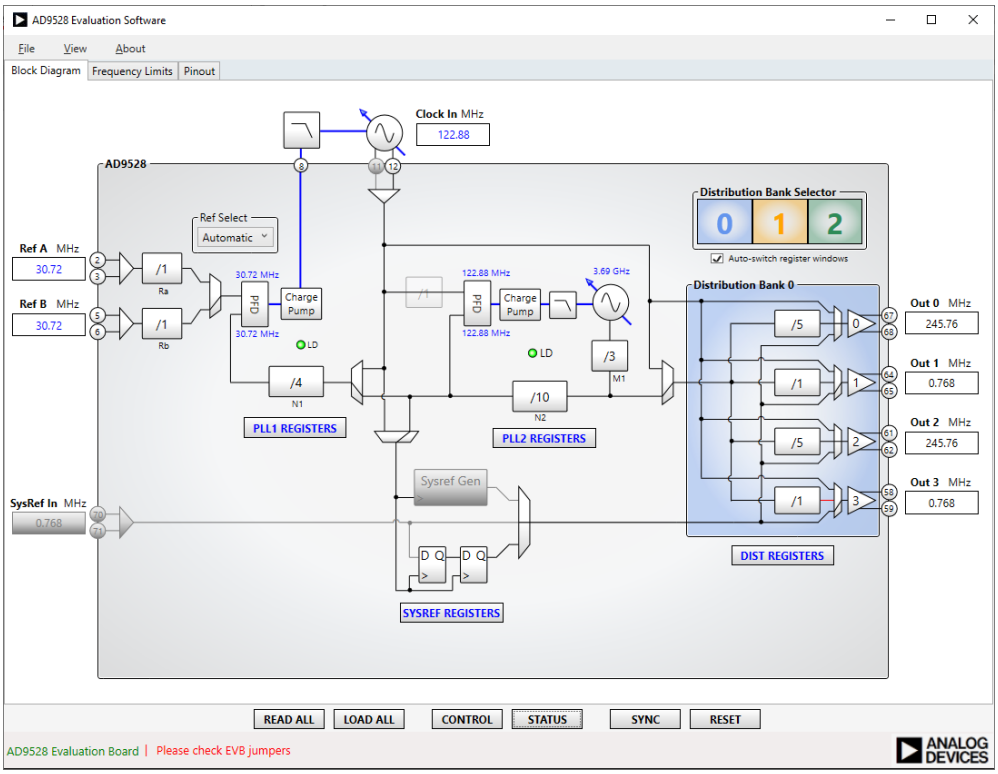

Figure 1. AD9528 setup used during the tests

I set the STATUS0 and STATUS1 outputs to go high when PLL1 is locked:

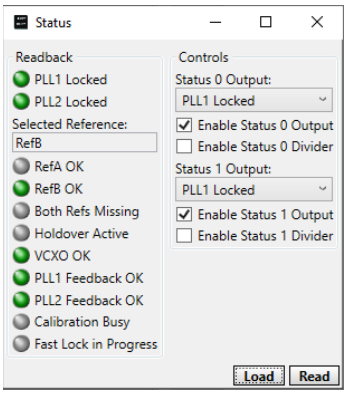

Figure 2. STATUS0 and STATUS1 are set to output PLL1 Locked status

I observed on the oscilloscope that STATUS0 and STATUS1 outputs are high (3.3V).

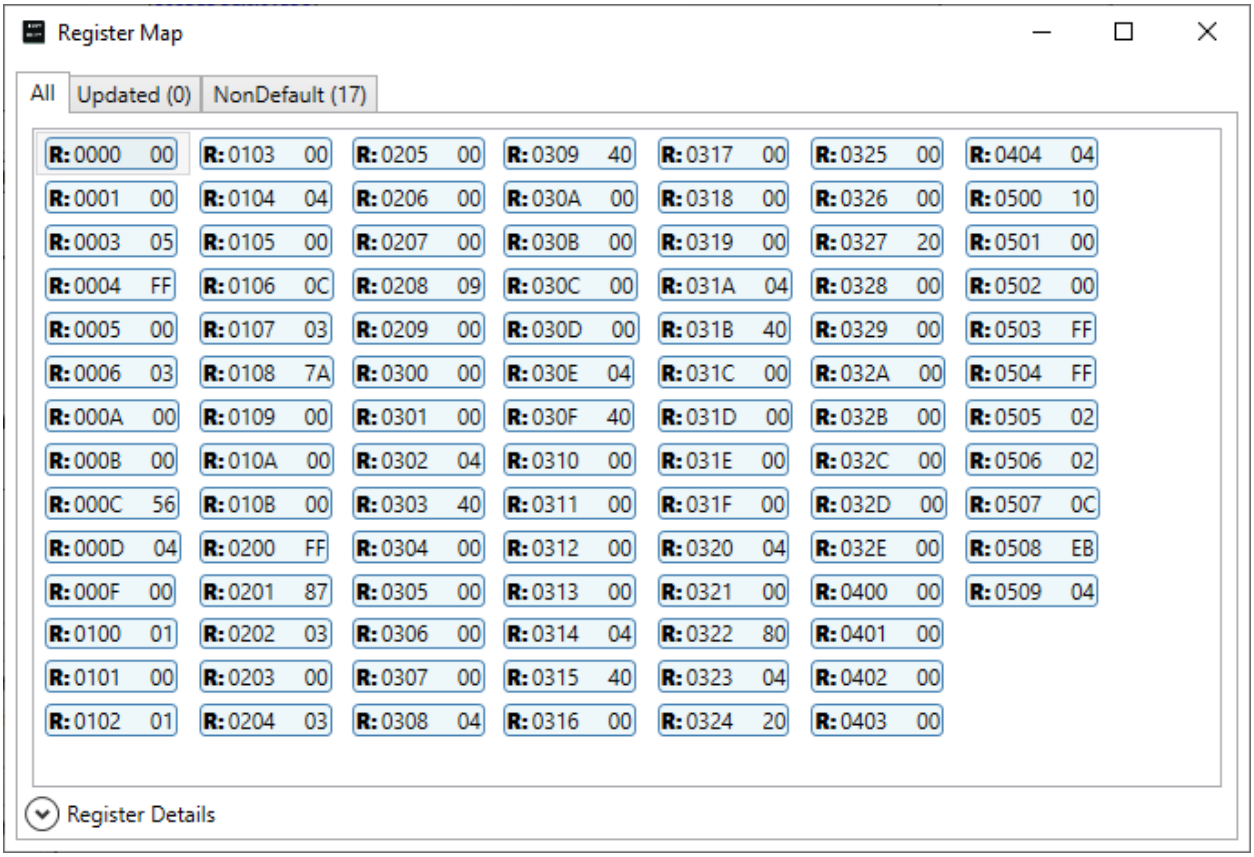

Figure 3. Register Map values

Table 68. Readback Registers (Readback 0 and Readback 1)

Address	Bits	Bit Name	Description
0x0508	7	PLL2 feedback status	1 = correct. 0 = off/clocks are missing.
	6	PLL1 feedback status	1 = correct. 0 = off/clocks are missing.
	5	VCXO status	1 = correct. 0 = off/clocks are missing.
	4	Both REFA/REFB missing	1 = off/clocks are missing. 0 = correct.
	3	REFB status	1 = correct. 0 = off/clocks are missing.
	2	REFA status	1 = correct. 0 = off/clocks are missing.
	1	PLL2 locked status	1 = locked. 0 = unlocked.
	0	PLL1 locked status	1 = locked. 0 = unlocked.

The register 0x508 has 0xEB, which shows bit 0 being 1. Because REFB is valid, the bit 4 is 0.

At this point I stopped REFB to be generated. PLL1 went unlocked on the green LED in the evaluation software:

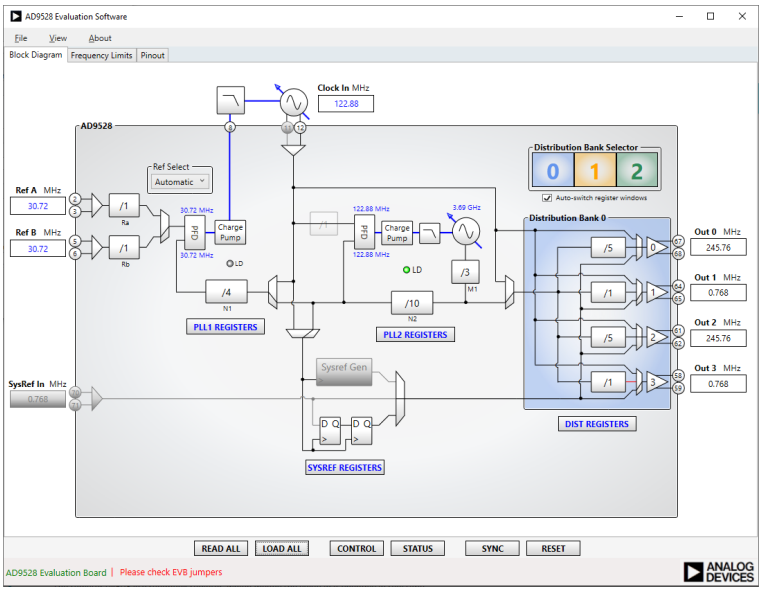

Figure 4. PLL1 went unlocked when I cut REFB

STATUS0 and STATUS1 outputs went low. The register 0x508 is not equal to 0xF2, as expected

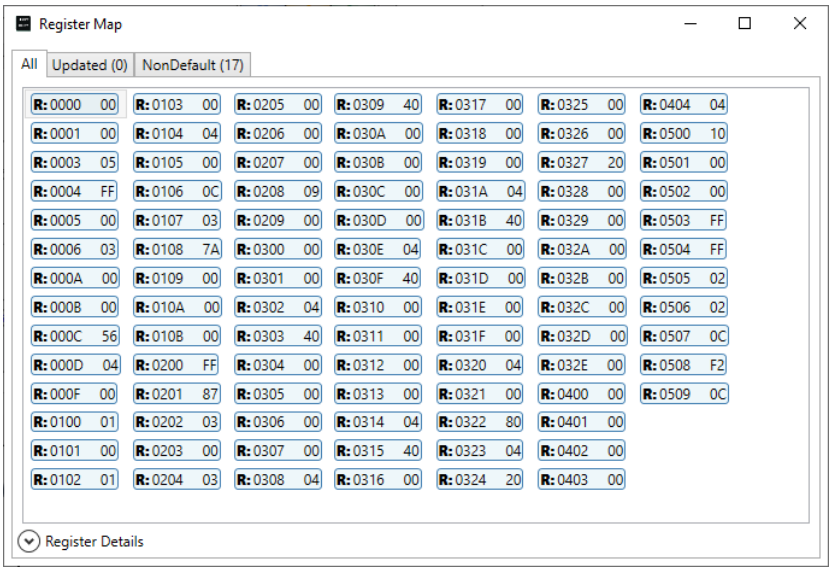

Figure 5. Register map window showing register 0x508 equal to 0xF2