

09/15/2021

AD9528 PLL1 Lock Status tests

I set the AD9528 as follows:

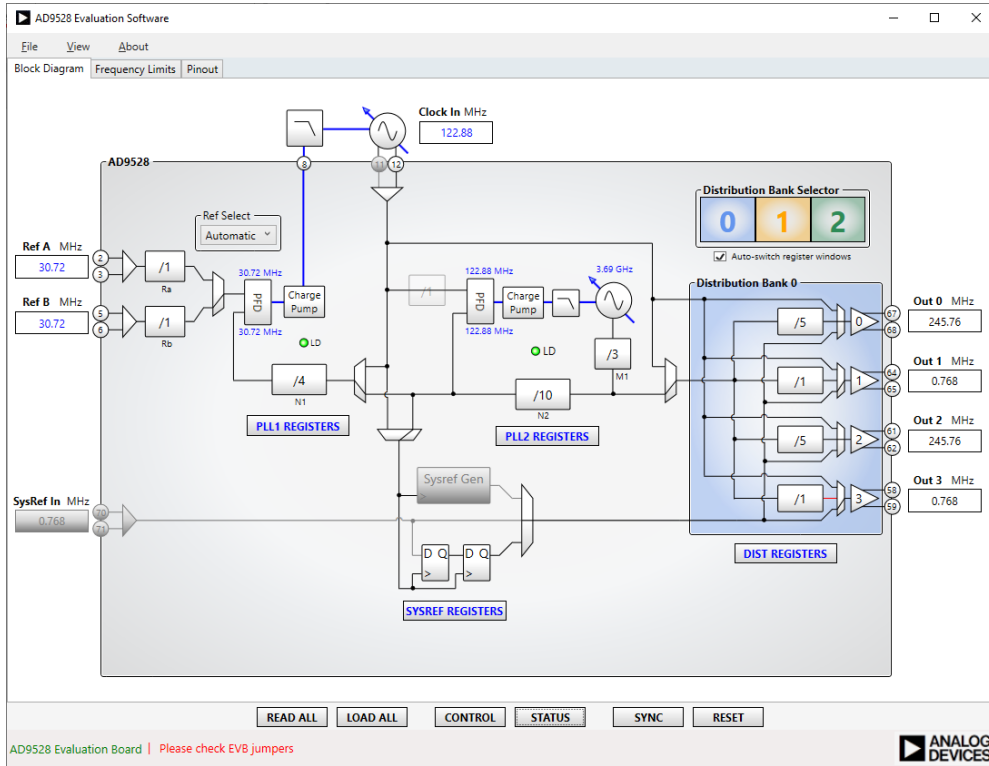


Figure 1. AD9528 setup used during the tests

I set the STATUS0 and STATUS1 outputs to go high when PLL1 is locked:

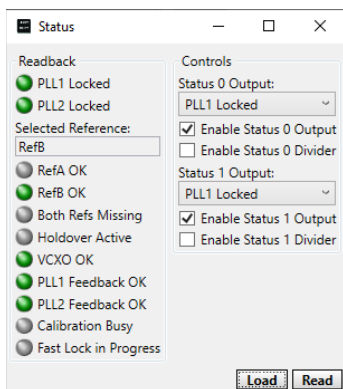


Figure 2. STATUS0 and STATUS1 are set to output PLL1 Locked status

I observed on the oscilloscope that STATUS0 and STATUS1 outputs are high (3.3V).

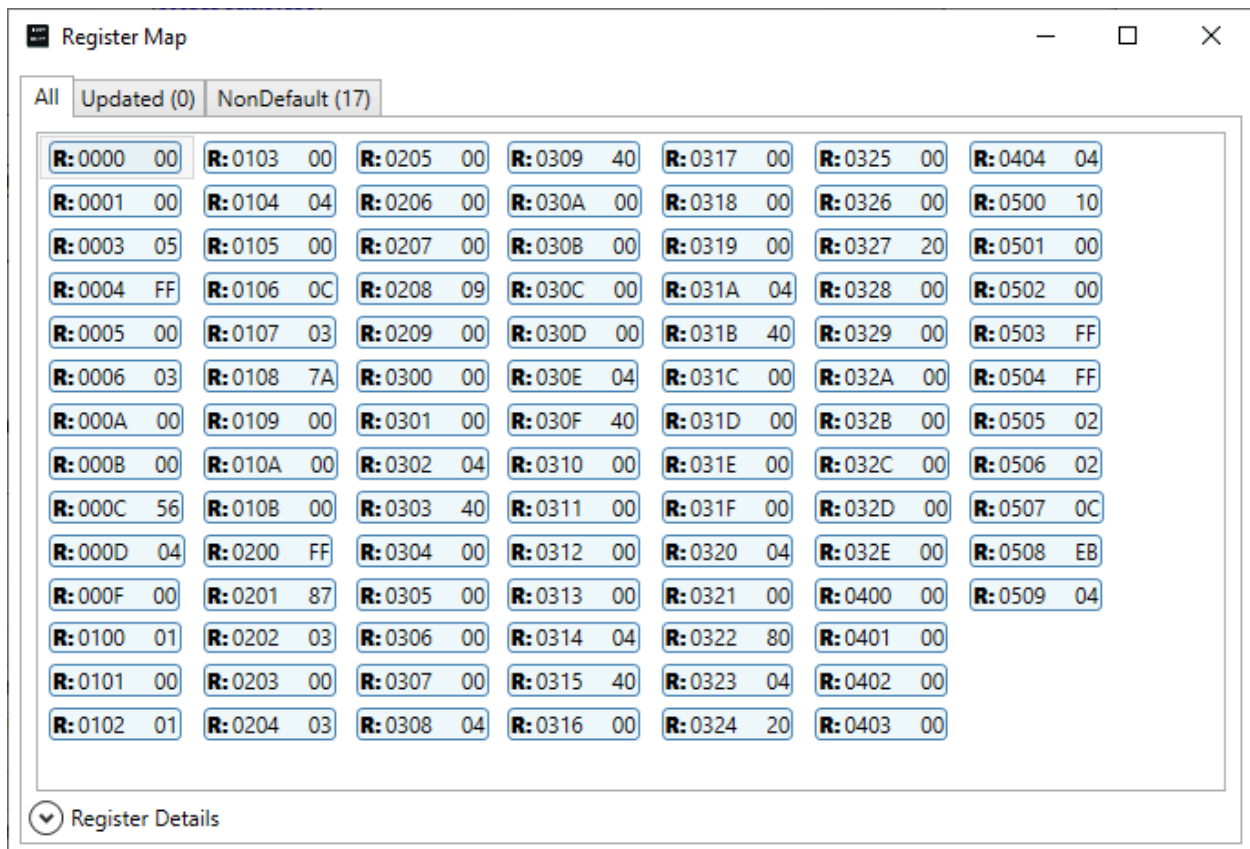


Figure 3. Register Map values

Table 68. Readback Registers (Readback 0 and Readback 1)

Address	Bits	Bit Name	Description
0x0508	7	PLL2 feedback status	1 = correct. 0 = off/clocks are missing.
	6	PLL1 feedback status	1 = correct. 0 = off/clocks are missing.
	5	VCXO status	1 = correct. 0 = off/clocks are missing.
	4	Both REFA/REFB missing	1 = off/clocks are missing. 0 = correct.
	3	REFB status	1 = correct. 0 = off/clocks are missing.
	2	REFA status	1 = correct. 0 = off/clocks are missing.
	1	PLL2 locked status	1 = locked. 0 = unlocked.
	0	PLL1 locked status	1 = locked. 0 = unlocked.

The register 0x508 has 0xEB, which shows bit 0 being 1. Because REFB is valid, the bit 4 is 0.

At this point I stopped REFB to be generated. PLL1 went unlocked on the green LED in the evaluation software:

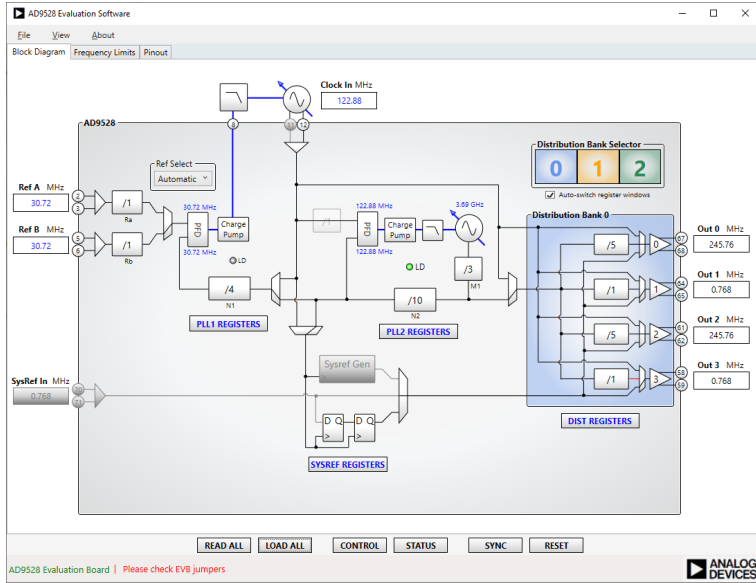


Figure 4. PLL1 went unlocked when I cut REFB

STATUS0 and STATUS1 outputs went low. The register 0x508 is not equal to 0xF2, as expected

The screenshot shows the Register Map window with a grid of registers. The registers are organized into columns and rows. Register 0x508 is highlighted with a value of F2. The registers are as follows:

R: 0000 00	R: 0103 00	R: 0205 00	R: 0309 40	R: 0317 00	R: 0325 00	R: 0404 04
R: 0001 00	R: 0104 04	R: 0206 00	R: 030A 00	R: 0318 00	R: 0326 00	R: 0500 10
R: 0003 05	R: 0105 00	R: 0207 00	R: 030B 00	R: 0319 00	R: 0327 20	R: 0501 00
R: 0004 FF	R: 0106 0C	R: 0208 09	R: 030C 00	R: 031A 04	R: 0328 00	R: 0502 00
R: 0005 00	R: 0107 03	R: 0209 00	R: 030D 00	R: 031B 40	R: 0329 00	R: 0503 FF
R: 0006 03	R: 0108 7A	R: 0300 00	R: 030E 04	R: 031C 00	R: 032A 00	R: 0504 FF
R: 000A 00	R: 0109 00	R: 0301 00	R: 030F 40	R: 031D 00	R: 032B 00	R: 0505 02
R: 000B 00	R: 010A 00	R: 0302 04	R: 0310 00	R: 031E 00	R: 032C 00	R: 0506 02
R: 000C 56	R: 0108 00	R: 0303 40	R: 0311 00	R: 031F 00	R: 032D 00	R: 0507 0C
R: 000D 04	R: 0200 FF	R: 0304 00	R: 0312 00	R: 0320 04	R: 032E 00	R: 0508 F2
R: 000F 00	R: 0201 87	R: 0305 00	R: 0313 00	R: 0321 00	R: 0400 00	R: 0509 0C
R: 0100 01	R: 0202 03	R: 0306 00	R: 0314 04	R: 0322 80	R: 0401 00	
R: 0101 00	R: 0203 00	R: 0307 00	R: 0315 40	R: 0323 04	R: 0402 00	
R: 0102 01	R: 0204 03	R: 0308 04	R: 0316 00	R: 0324 20	R: 0403 00	

Figure 5. Register map window showing register 0x508 equal to 0xF2