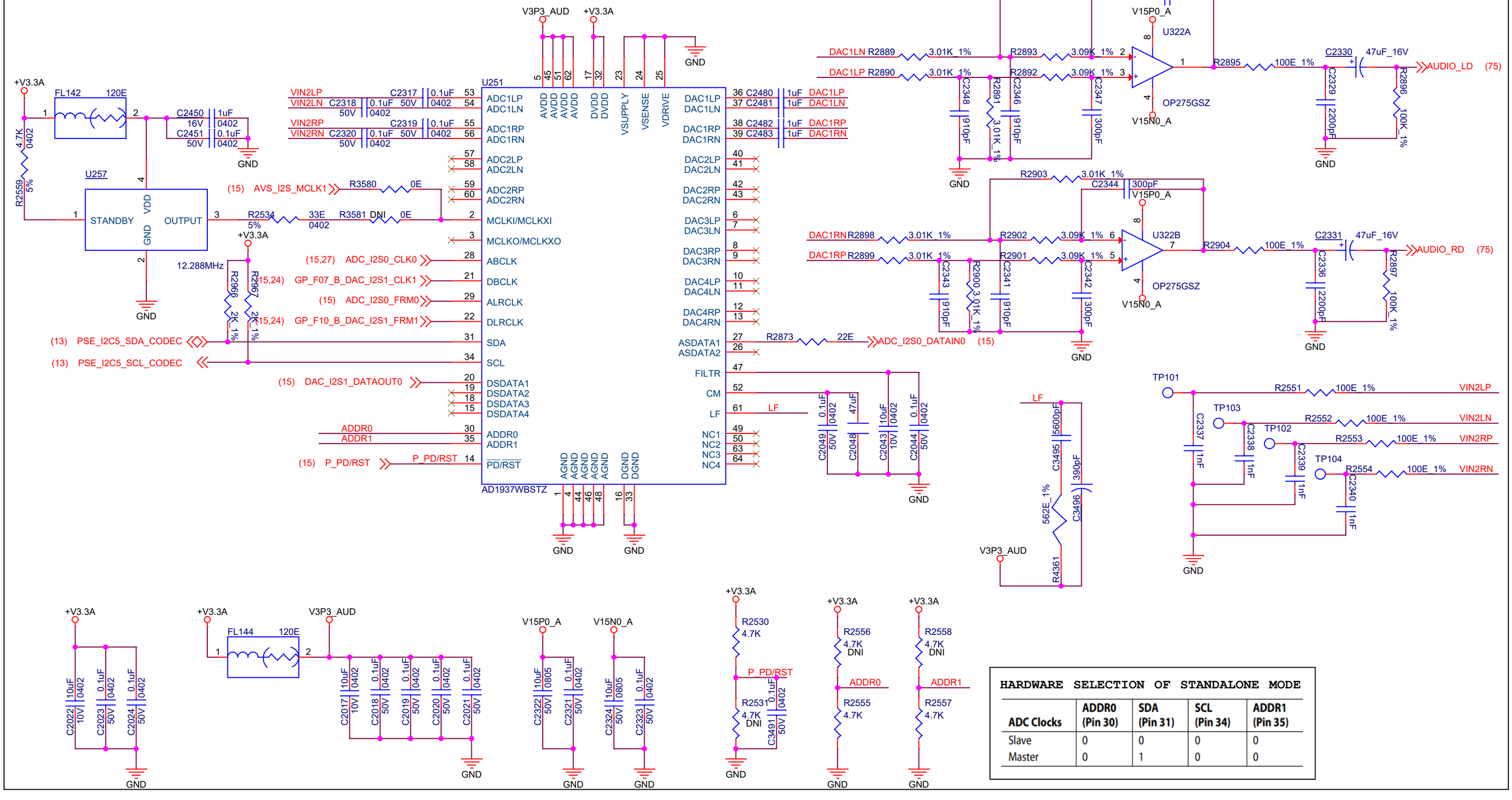
AUDIO_CODEC



HARDWARE SELECTION OF STANDALONE MODE				
ADC Clocks	ADDR0 (Pin 30)	SDA (Pin 31)	SCL (Pin 34)	ADDR1 (Pin 35)
Slave	0	0	0	0
Master	0	1	0	0

REV NO.	NATURE OF CHANGE	APPROVED BY	DATE

MISTRAL

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Drawn by:	Mistral Design Team	Approved by:	<Apprd by>
Date:	Tuesday, July 23, 2013	Date	Monday, February 12, 2024
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Title	AUDIO CODEC		
Size	Document Number		Rev
B	MS_DMP_REDESIGN_SCH_REVA		A
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