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<th>Revision</th>
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<td>Rev 1.0</td>
<td>Sep. 12, 2014</td>
<td>This is the first release of this document</td>
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1 Introduction

Analog Devices, Inc. (ADI) high-speed digital logic (HSDL) products use Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT), a proven and reliable process technology. The logic gates and interfaces are based on the Current-Mode Logic (CML) I/O logic interfacing standard. CML is the best choice for multi-gigabit high-speed digital signals.

Here are some of the features of CML I/O-based circuits:

- Limiting vs. linear response at output for normal input amplitudes
- Constant current maintained by tail current source in differential pair circuit for reduced power supply transients and noise.
- High-speed AC currents circulate at positive power supply (+V).
- Proven circuit topology; widely used for high-speed circuit design.
- Supports very high-speed operation (40+ Gb/s)
- Differential circuit:
  - High CMRR
  - Symmetrical, fully differential PCB layout possible for improved Signal Integrity
- Controlled Impedance – typically Zo = 50Ω

ADI's HSDL products operate at up to a data rate of 45 Gbps and up to 25-32 GHz in clock frequency, depending on application, specific part number and logic function.

There are however, many other I/O logic standards. Some examples are LVCMOS, LVDS, LVPECL, and LVTTL to name a few of the more commonly used standards.

This Application Note addresses interfacing ADI’s HSDL to some of the most common I/O logic standards.

Field Programmable Gate Arrays (FPGAs) are widely used in designs and systems today. FPGAs support a large number of I/O logic standards, including DDR memory interfacing. Most of these I/O standards only operate to approximately 2 Gbps, but 1.2V CML can operate up to 28 Gbps for the current state-of-the-art advanced FPGA series of products. ADI HSDL products can support these advanced FPGAs with proper interface circuits and techniques.
### 2 Summary of Selected I/O Logic Standards

There are many I/O logic standards for interfacing high-speed logic. Table 1 gives HI/LO logic level DC voltages for a selection of some of the more common I/O standards that are more frequently used.

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<th>I/O LOGIC STANDARD</th>
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<th>VIH (MIN)</th>
<th>VIH (MAX)</th>
<th>VOH (TYP)</th>
<th>VOH (MIN)</th>
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<td>0.700</td>
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**Table 1. Summary of Selected I/O Logic Standards: DC Voltage Levels, Numerical Table**

Most I/O Logic Standards values based on Xilinx FPGA data sheet values

Xilinx GTX/GTH Transceivers use 1.2V CMOS CML. Only FPGA I/O that supports > 2Gbps data rates

1.2V, 2.5V, 3.3V CMOS are only I/O logic standards that support >2Gbps
3 Logic Levels of Selected I/O Logic Standards

3.1 ADI CML input common-mode voltage (CMV) and maximum/minimum voltage ranges. Figures 3-1 and 3-2 show input voltage and CMV ranges for +3.3V (+V)/0V, and 0V/-3.3V (-V) power supply operation, both for differential and single-ended inputs.

Figure 3-1. +3.3V ADI CML: Input DC Voltage Levels

Figure 3-2. -3.3V ADI CML: Input DC Voltage Levels
3.2 Summary of Selected I/O Logic Standards: DC Voltage Levels, Graphical Format

![Diagram of DC Voltage Levels for Selected I/O Logic Standards]

Figure 3-3. Summary of Selected I/O Logic Standards: DC Voltage Levels, Graphical Format
3.3 Summary of Selected DDR Memory I/O Logic Standards: DC Voltage Levels, Graphical Format

Figure 3-4. Summary of Selected DDR Memory I/O Logic Standards: DC Voltage Levels, Graphical Format
4 Simplified Interface Schematics

4.1 ADI HSDL products operating at 32 Gbps or less generally support both positive and negative power supply operation. The first case is for use with +3.3V (+V)/0V power supplies, and the second is for use with 0V/-3.3V(-V) power supplies. The following eight figures show the different combinations for power supplies, AC- vs. DC-coupling at the input, and differential vs. single-ended operation.

+3.3V CML interfacing example: Differential input, DC-coupled input.

![Figure 4-1. +3.3V, differential input, DC-coupled input](image)

+3.3V CML interfacing example: Differential input, AC-coupled input.

![Figure 4-2. +3.3V, differential input, AC-coupled input](image)
+3.3V CML interfacing example: Single-Ended input, DC-coupled

![Diagram of +3.3V, Single-ended input, DC-coupled input]

Figure 4-3. +3.3V, Single-ended input, DC-coupled input

+3.3V CML interfacing example: Single-ended input, AC-coupled

![Diagram of +3.3V, Single-ended input, AC-coupled input]

Figure 4-4. +3.3V, Single-ended input, AC-coupled input
-3.3V CML interfacing example: Differential input, DC-coupled

Figure 4-5. -3.3V, Differential input, DC-coupled input

-3.3V CML interfacing example: Differential input, AC-coupled

Figure 4-6. -3.3V, Differential input, AC-coupled input
-3.3V CML interfacing example: Single-ended input, DC-coupled

Figure 4-7. -3.3V, Single-ended input, DC-coupled input

-3.3V CML interfacing example: Single-ended input, AC-coupled

Figure 4-8. -3.3V, Single-ended input, AC-coupled input
4.2 ADI HSDL products can also interface to a variety of other I/O logic standards, including LVPECL, LVDS, and SSTL, to name a few. The simplified schematics in the following figures provide interfacing examples to some of the more common I/O logic standards.

LVPECL-to-CML interfacing example: Differential input, DC-coupled

CML-to-LVPECL interfacing example: Differential input, AC-coupled (a)
CM-to-LVPECL interfacing example: Differential input, AC-coupled (b)

![CM-to-LVPECL interfacing example](image)

Figure 4-10b. CML-to-LVPECL interfacing example: Differential input, AC-coupled

LVDS-to-CML example: Differential, AC-coupled (a)

![LVDS-to-CML example](image)

Figure 4-11a. LVDS-to-CML example: Differential, AC-coupled
LVDS-to-CML example: Differential, AC-coupled (b)

Figure 4-11b. LVDS-to-CML example: Differential, AC-coupled

CML-to-LVDS example: Differential, AC-coupled

Figure 4-12. LVDS-to-CML example: Differential, AC-coupled
3.3V CMOS-to-CML example: Single-ended, DC-coupled, single and double inputs

![CMOS-to-CML example: Single-ended, DC-coupled, single and double inputs](image)

Figure 4-13a,b. CMOS-to-CML example: Single-ended, DC-coupled, single and double inputs

SSTL-2-to-CML example: Differential, DC-coupled (a)

![SSTL-2-to-CML example: Differential, DC-coupled](image)

Figure 4-14a. SSTL-2-to-CML example: Differential, DC-coupled
SSTL-2-to-CML example: Single-ended, DC-coupled (b)

Figure 4-14b. SSTL-2-to-CML example: Single-ended, DC-coupled
5 Application Circuit Examples: Description and Schematics

The following figures show some typical applications of HSDL products in practice. FPGA interfacing can be implemented with either AC-coupling or DC-coupling, depending on the data format and power supplies available.

HMC854LC5 28 Gbps 4:1 MUX + HMC855LC5 28 Gbps 1:4 DEMUX interfacing to Xilinx Virtex-5 FPGA with LVDS_25 I/O Logic Standard, split power supplies, Differential I/O, DC-coupled

![Figure 5-1: HSDL interfacing example 1](image1)

HMC745LC3C 14 Gbps XOR Gate interfacing to Xilinx Virtex-5 FPGA with LVDS_25 I/O Logic Standard, split power supplies, Differential I/O, DC-coupled

![Figure 5-2: HSDL interfacing example 2](image2)
HMC854LC5 28 Gbps 4:1 MUX + HMC855LC5 28 Gbps 1:4 DEMUX interfacing to a Fiber-Optic serial data link at 25-32 Gbps.

Figure 5-3: HSDL interfacing example 3

HMC854LC5 28 Gbps 4:1 MUX + HMC855LC5 28 Gbps 1:4 DEMUX interfacing to a serial data link at 25.6 Gbps using SSTL12 or SSTL15 I/O logic standard interfacing to FPGAs. Single-ended or differential operation, DC-coupled.

Figure 5-4: HSDL interfacing example 4
6 VR Output Voltage Control Pin Usage

Adjustable output amplitude (Vout p-p) is a feature available on most HSDL products. This allows the user to 1) increase the output signal swing in order to compensate for PCB attenuation and other losses, or 2) reduce the output signal swing for power savings, or improved matching to input levels at the following stage. The adjustable output swing function, when available, can be used on HSDL parts operating on either +3.3V/0V, or 0V/-3.3V power supplies.

VR output voltage swing adjustment range: Fig. 6-1a: +3.3V/0V power supplies. Fig. 6-1b: 0V/-3.3V power supplies.

![VR output voltage swing adjustment range for +3.3V/0V and 0V/-3.3V power supplies](image)

Example circuits for driving the VR pin. Note that a resistor divider network is not recommended due to VR input current requirements of typically 3mA. A minimum op amp output current drive capability of 5mA is recommended.

![Example circuits for driving the VR pin](image)
7 Summary and Conclusions

ADI HSDL products can support interfacing to many I/O logic standards using the methods described in this Application Note. Interfaces are either AC-coupled or DC-coupled, depending on the data format or clock signal used in the application.

Typically the simplest interfacing method is AC-coupling to other digital signals. This can be done for balanced, scrambled, or coded data that is continuous and maintains a mark density or duty cycle of approximately 50%. This coupling method can also be easily used for continuous clock signals. AC-coupling, or interfacing with a DC-blocking capacitor simplifies the interface resulting from any common-mode DC voltage mismatch that are typical for the many different I/O logic standards.

When data is “bursty”, non-continuous, or is of low mark density or duty cycle, then DC-coupling is preferred due to the lack of AC time constants from the termination resistors and AC-coupling capacitors. DC-coupling may require external resistor networks, or split power supplies in order to bridge the mismatch between common-mode DC voltages for different I/O logic standards.

Please contact Analog Devices Applications Engineering with any questions about your specific requirements for interfacing to HSDL products in your unique system configuration.

8 References

http://www.altera.com/literature/lit-an.jsp
http://www.xilinx.com/support/index.htm

9 Acronyms

CML Current-Mode Logic
LVCMOS Low Voltage Complementary Metal-Oxide Semiconductor
DDR Double Data Rate (Memory)
FPGA Field Programmable Gate Array
HSDL High-Speed Digital Logic
HSTL High-Speed Transceiver Logic
LVDS Low Voltage Differential Signaling
LVPECL Low Voltage Positive Emitter-Coupled Logic
SiGe HBT Silicon-Germanium Heterojunction Bipolar Transistor
SSTL Stub-Series Terminated Logic
LVTTL Low Voltage Transistor to Transistor Logic