# LTC4015 and LTC4162 Hot-Swapping

Zachary Pantely

In any power system where sources will have the option of being hot-swapped, testing needs to be done in order to ensure that inrush currents and the resulting ringing are within a suitable range under the worst-case hot-swapping conditions.

**Hot-Swapping Issues:**
The term hot-swapping is often used to describe the application of power to a circuit from a source that is already enabled. More correctly, hot-swapping refers to the swapping of components with power still enabled, but the term's usage has spread to mean essentially the opposite. For example, connecting a battery to a powered-down system is often referred to as hot-swapping. This definition is what we are concerned with here.

The issue occurs due to capacitance in a circuit. With low-ESR capacitance drained to near 0V in a dead circuit, this instantaneously looks like a short to ground. Upon the application of power, a large instantaneous current (whose value is defined by ESR and other parasitics in the circuit) flows and can easily reach hundreds of amps.

The problems caused by hot-swapping are two-fold:

1. Inrush current. As previously mentioned, this is an instantaneous parasitically-controlled current that can easily instantaneously reach hundreds of amps.
2. Voltage transients / ringing. As a result of inrush current though any wire attaching the power supply to a board, or traces on the PCB, there will be voltage transients associated with inrush current. This is due to inherent inductance in any trace of wire. For longer wires, inductance is generally worse, and the voltage peaks can get higher.

**LTC4015 and LTC4162:**

When dealing with batteries, this can be extra troublesome because (1) batteries are always hot-plugged when being connected to anything and (2) batteries have a low source impedance, enabling them to output a large inrush current. As a result, inrush issues need extra care when dealing with battery charger circuits.

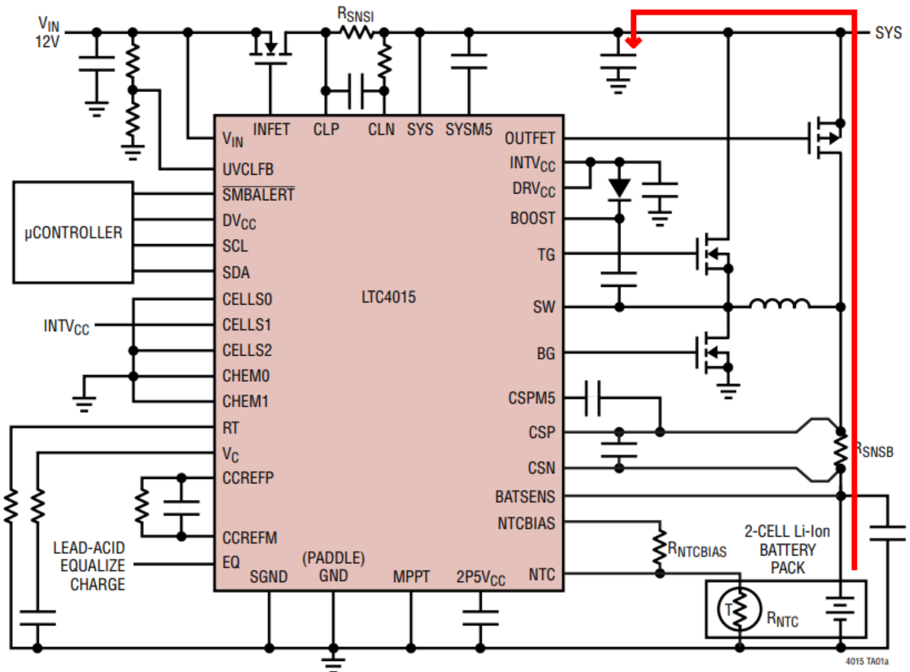


**Figure 1. LTC4015 Battery Hot-Swap Inrush Path.**

Figure 1 shows the problematic battery hot-swap path for inrush current on the LTC4015, which is the same for the LTC4162. The trouble here is that the inrush passes through a few low-impedance series components (the sense resistor and the FET) in order to get to the cap on the SYS rail. There will also be inrush into the cap that is in parallel with the battery, and this will contribute to voltage transients and ringing, but this often does not cause as much trouble as the inrush current to the system rail.

*The main cause of failure in hot-swapping VIN or BAT on LTC4015 and LTC4162 is violation of the 0.3V differential absolute maximum value of the current sense inputs as a result of inrush current across the sense resistor instantaneously generating a voltage greater than 0.3V.*

This cause of failure can often show visible damage on the IC, and sometimes even burn traces. Note that this can happen on either the input or battery sense inputs, but it is far more common on the battery side because input currents are often more controlled.

Also note that the battery PowerPath FET (OUTFET on LTC4015 or BATFET on LTC4162) plays an important role in mitigating voltage spikes during inrush events. This FET (or at least a diode in its place) is absolutely necessary because it bypasses the sneak path formed through the buck regulator to the SYS rail. Without the battery PowerPath FET installed, inrush current would flow through the sense resistor, inductor, top FET body diode, and into the SYS cap anyway, except the inductance added by the inductor will create a sizeable voltage transient and possibly cause damage.

**Handling Inrush on LTC4015 and LTC4162:**
There are two approaches to handle inrush in these circuits.

The first way is the 'correct' way: stop inrush at the source. Add current-limiting between the problematic source and the rest of the circuit. A common approach to this problem is to use ferrite beads, but that is not generally recommended here. Although it will mitigate the inrush current, voltage transients will be worse as a result of the added inductance. A better solution is to use a hot-swap controller or a discrete inrush limiting circuit.

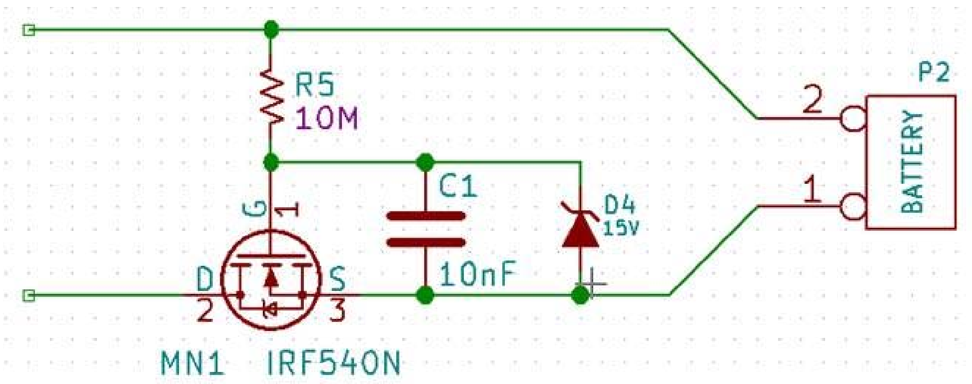


**Figure 2. Inrush Limiting Circuit from Discrete Components.**

The simple circuit in Figure 2 limits inrush current by slowing the turn-on of a pass FET. The values of the resistor and capacitor determine the turn-on speed of the FET. The Zener diode exists only to protect the FET and may not be necessary for battery voltages that are suitably less than the $V_{GS(max)}$ of the FET.

The resistor and capacitor value will likely need to be tweaked depending on the battery's voltage, but the values shown here may be a good starting point.

Note that the capacitor's only discharge path is through the resistor when the battery has been removed. This may be suitable but, if a faster turn-off of the FET is required, a drain resistor can be placed in parallel with the capacitor. Be aware that this will form a voltage divider with the top resistor and that it will add some constant drain to the inrush protection circuit.

Also, note that the pass FET needs to be able to handle the full charge/discharge current of the battery.

Analog Devices also offers a number of hot-swap controllers for purposes such as this:
http://www.analog.com/en/products/monitor-control-protection/hot-swap-controllers.html

There is a second way to handle inrush on the LTC4162 and one of the inputs on the LTC4015.

Since the most likely cause for damage of these ICs as a result of inrush is the differential voltage across the sense inputs, another possible solution is to simply protect these inputs if the inrush to the demo board is not otherwise problematic. That is to say, this solution does not *stop* inrush currents or their associated voltage transients.

An important note about this approach is that it cannot be used on the battery sense inputs of the LTC4015 (CSP/CSN). This would skew current measurements due to the architecture of the coulomb counter. For this input, the previously mentioned approach must be used.

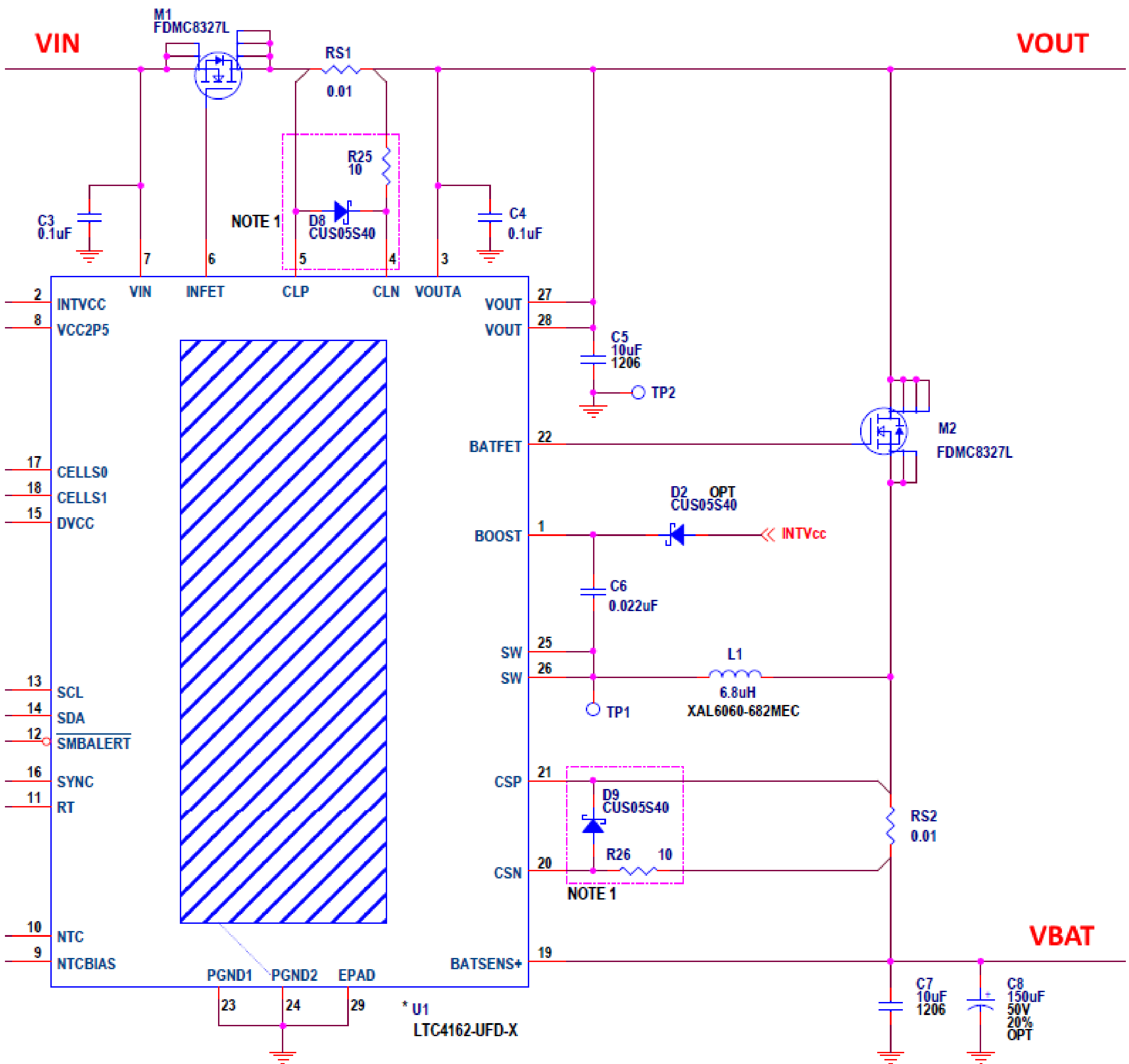


**Figure 3. Protecting Sense Inputs on LTC4162.**

Figure 3 shows a method of limiting the differential voltage across the sense inputs. This is done by dropping the voltage across a 10Ω resistor when it exceeds the forward voltage of a Schottky diode. During normal operation, the differential voltage across the sense inputs is less than the Vf of the diode, so it does not interfere with measurements.

Note that on both the CLP/CLN and CSP/CSN inputs, the diodes always point to the output node (SYS on LTC4015, VOUT on LTC4162). This is due to the direction of the inrush current from each source (VIN or BAT). Also note that the 10Ω resistors are on the negative (CLN/CSN) inputs of the sense input pairs. These are the high-impedance inputs that draw negligible current so that the series resistors do not skew current measurements.

**Testing Hot-Swapping:**

Hot-swapping inrush current and voltage transients always need to be evaluated in systems where hot-swapping is allowed. In order to suitably test this, the following steps should be used:

1. Discharge the caps on the board completely. Worst inrush occurs when the caps are empty.
2. Ensure no other voltage sources are connected when testing inrush. At least, voltage sources that might be holding caps at a non-zero voltage value. Only one hot-swappable input should be tested at a time.
3. Configure an oscilloscope to catch these peak currents or voltages. You might set it to trigger on voltage presence and then watch the current. Or, you may set it to trigger on a SYS/VOUT voltage slightly higher than your battery voltage, for example, to see substantial voltage transients are visible upon connection.
4. Apply voltage by quickly connecting the power supply or battery. That is, manually make the connection rather than enabling/disabling a power supply (power supply output enable is generally too nice to circuits to get a feel for what hot-swapping will be like).
5. Repeat the test many times. You may see 100A inrush currents in one test and 20A upon the next connection. There is a tremendous amount of variability here which can only be accounted for through the use of many tests. Test with a lot of time between connections and also test with many connections in rapid succession.