

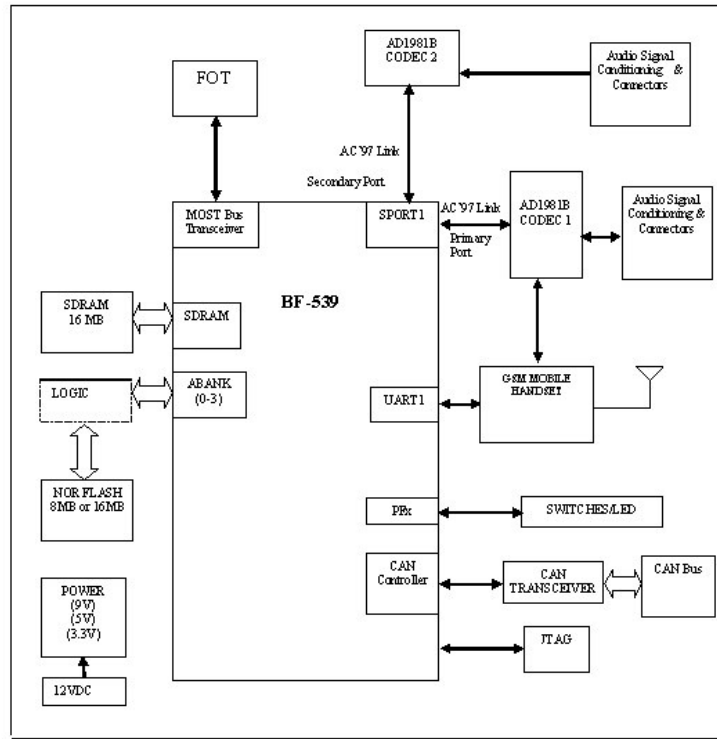
HFCK REV2.0 BOARD FOR BLACKFIN 539 SCHEMATICS

REVISION HISTORY

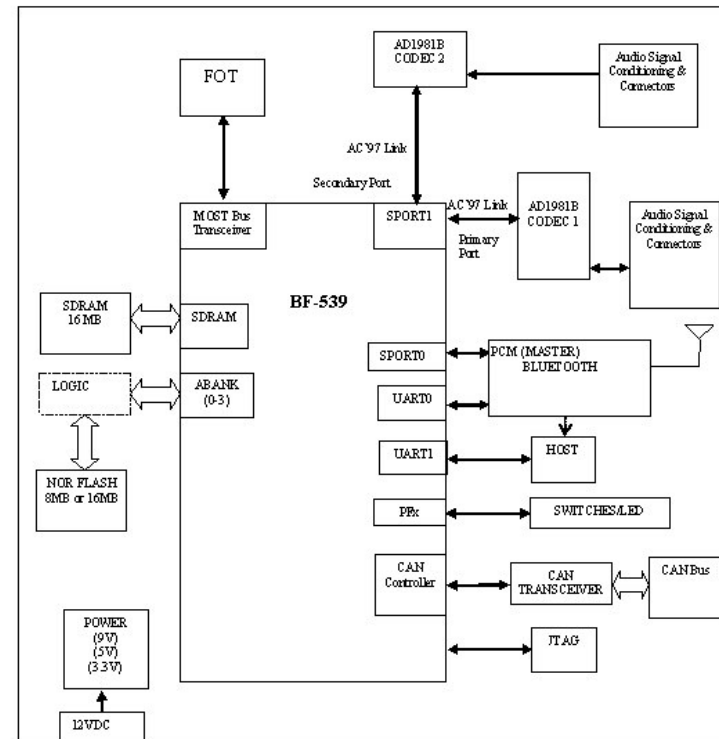
| REV # | DATE | DESCRIPTION OF CHANGES | AUTHOR | REVIEWED BY | APPROVED BY |
|-------|-------------|--|-----------------------|-------------|-------------|
| 001 | 18 AUG 2004 | SCHEMATICS CREATED | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 002 | 20 AUG 2004 | REVIEW UPDATES | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 003 | 21 AUG 2004 | REVIEW UPDATES. CHANGED THE OS8104 SECTION TO 5V FROM 3.3V | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 010 | 24 AUG 2004 | RELEASE | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 011 | 8 SEP 2004 | REVIEW UPDATES | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 012 | 9 SEP 2004 | 1. UPDATED BT-BF INTERFACE - BT- PCM TO BF- SPORT 2. UPDATED BF538 PIN OUT SIGNAL NAMING BASED ON BF538 DATASHEET - PRE REV A | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 013 | 28 SEP 2004 | 1. UPDATED LED SECTION - REMOVED THE TRANSISTORS USED FOR DRIVING THE LEDs. | NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 014 | 14 OCT 2004 | 1. CHANGED THE PROCESSOR TO BF539 2. ADDED INFINEON BLUETOOTH | SHAMEE NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 015 | 18 OCT 2004 | 1.REVIEW UPDATES | SHAMEE NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 016 | 19 OCT 2004 | 1.ADDED OPTION FOR CONNECTING BT-PCM TO BF-SPI | SHAMEE NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 017 | 21 OCT 2004 | 1.ADDED SERIES DAMPING RESISTORS ON ADDRESS BUS[A1:A5] AFTER SI ANALYSIS 2.CHANGED THE 8.192MHz OSCILLATOR | SHAMEE NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 018 | 21 OCT 2004 | 1.REVIEW UPDATES | SHAMEE NAGALAKSHMI | SRIDHAR T S | SRIDHAR T S |
| 019 | 21 OCT 2004 | 1.REVIEW UPDATES | CAD TEAM | SRIDHAR T S | SRIDHAR T S |
| 020 | 26 OCT 2004 | 1.BACK ANNOTATED | CAD TEAM | SRIDHAR T S | SRIDHAR T S |

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|---------|------------------|-------------|------|---|----------------------------------|-------|---------------------------|-----|
| | | | | Drawn by: NAGALAKSHMI, SHAMEE | Approved by: SridharTS | Size | Document Number | Rev |
| | | | | Date: Wednesday, March 31, 2004 | Date: Thursday, October 28, 2004 | B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 |
| | | | | Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | Date: Thursday, October 28, 2004 | | Sheet 1 of 20 | |

HFCK BLOCK DIAGRAM-BF539



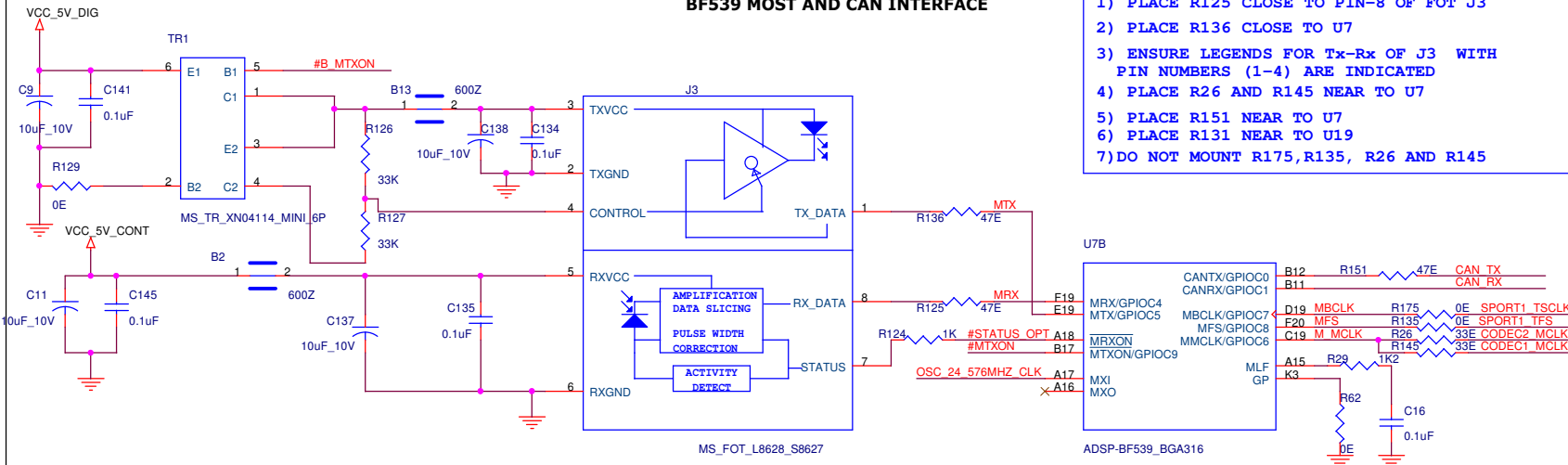
HFCK ARCHITECTURE WITH BF539 AND EXTERNAL GSM HANDSET CONNECTIVITY



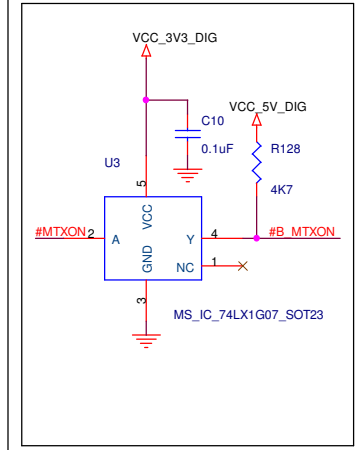
HFCK ARCHITECTURE WITH BF539 AND BLUETOOTH CONNECTIVITY

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|---------|------------------|-------------|------|--|--|------|---------------------------|---------------|
| | | | | | HFCK BLOCK DIAGRAM-BF532 | B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 |
| | | | | Drawn by: NAGALAKSHMI, SHAMEE Date: Wednesday, March 31, 2004 | Approved by: SridharTS Date: Thursday, October 28, 2004 | | | |
| | | | | Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | Date: Thursday, October 28, 2004 | | | |
| | | | | | | | | Sheet 3 of 20 |

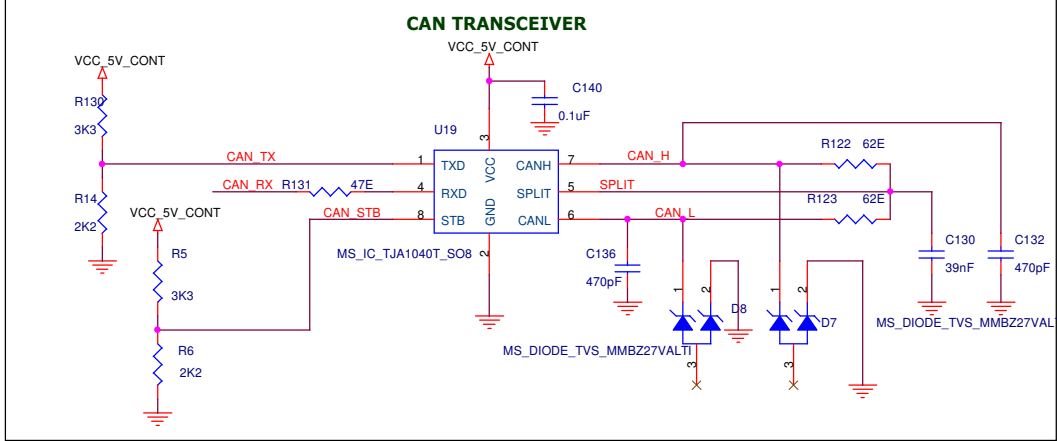
BF539 MOST AND CAN INTERFACE



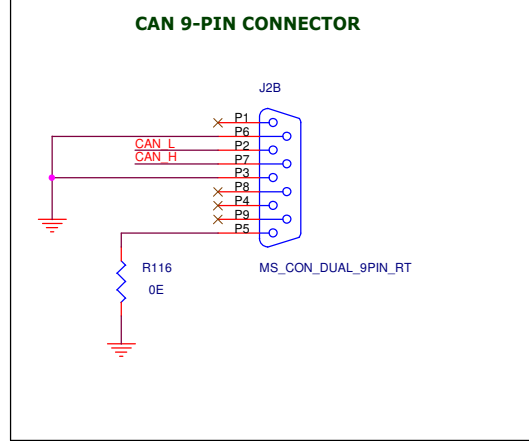
- 1) PLACE R125 CLOSE TO PIN-8 OF FOT J3
- 2) PLACE R136 CLOSE TO U7
- 3) ENSURE LEGENDS FOR Tx-Rx OF J3 WITH PIN NUMBERS (1-4) ARE INDICATED
- 4) PLACE R26 AND R145 NEAR TO U7
- 5) PLACE R151 NEAR TO U7
- 6) PLACE R131 NEAR TO U19
- 7) DO NOT MOUNT R175, R135, R26 AND R145



CAN TRANSCEIVER



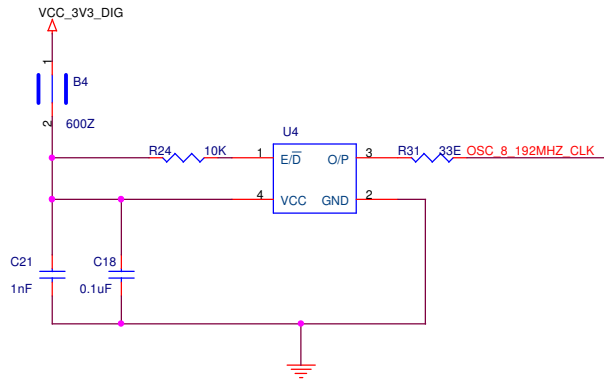
CAN 9-PIN CONNECTOR



- CLOCK**
- OSC 24 576MHZ_CLK <<> OSC_24_576MHZ_CLK 5
 - CODEC1_MCLK <<> CODEC1_MCLK 5,11
 - CODEC2_MCLK <<> CODEC2_MCLK 5,12
- SPORT SIGNALS**
- SPORT1_TFS <<> SPORT1_TFS 8
 - SPORT1_TSCLK <<> SPORT1_TSCLK 8
- CAN CONTROL SIGNALS**
- CAN_STB <<> CAN_STB 8

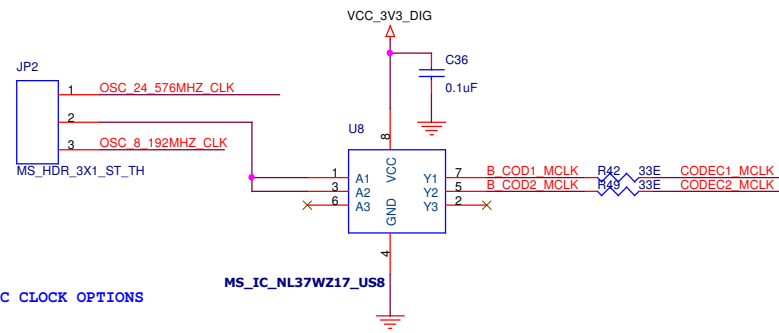
| REV NO. | NATURE OF CHANGE | APPROVED BY | DATE | Mistral Software [P] Ltd. | | Title | |
|---------|------------------|-------------|------|--|--|---|---------------|
| | | | | Mistral Software [P] Ltd. #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-535 6400, Fax : +91-80-5356444 | | BF539 MOST & CAN INTERFACE | |
| | | | | Drawn by: NAGALAKSHMI, SHAMEE Date: Wednesday, March 31, 2004 | Approved by: SridharTS Date: Thursday, October 28, 2004 | Size: B Document Number: MSADI_HFCK_REV2.0_SCH-020 | Rev: 2.0 |
| | | | | Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | | Date: Thursday, October 28, 2004 | Sheet 4 of 20 |

8.192MHz CODEC CLOCK



- 1) PLACE R31 CLOSER TO U4
- 2) PROVIDE SHIELDING TO U4

BUFFERED CLOCK INPUT TO CODECS & BF532



CODEC CLOCK OPTIONS

- 1) 8.192MHz OSC CLOCK AS CODEC CLOCK
CLOSE 2 AND 3 OF JP2.
- 2) 24.576MHz OSC CLOCK AS CODEC CLOCK
CLOSE PIN NO.1 AND 2 OF JP2.

- 1) PLACE R42 AND R49 CLOSE TO U8

CLOCK DISTRIBUTION

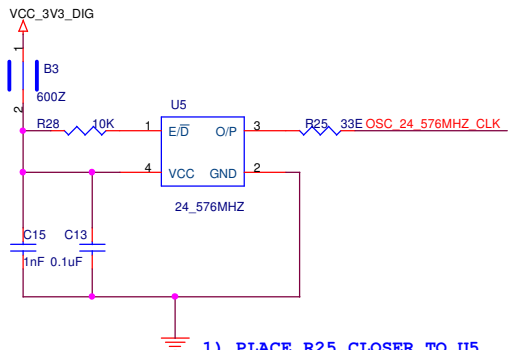
CODEC1_MCLK >>>CODEC1_MCLK 4,11
CODEC2_MCLK >>>CODEC2_MCLK 4,12

OSC_24_576MHZ_CLK >>>OSC_24_576MHZ_CLK 4
OSC_32_768KHZ_CLK >>>OSC_32_768KHZ_CLK 16

RESET

#SYS_RESET >>>#SYS_RESET 6,9,16

24.576 MHz CLOCK FOR BF539 AND CODEC

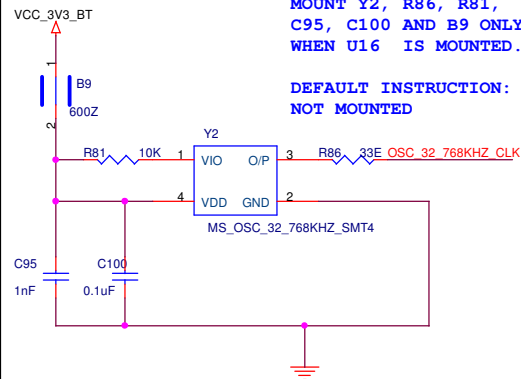


- 1) PLACE R25 CLOSER TO U5
- 2) PROVIDE SHIELDING TO U5

BLUETOOTH CLOCK

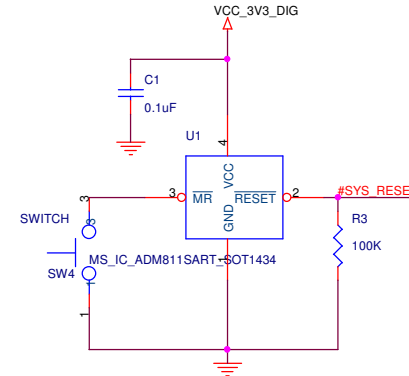
MOUNT Y2, R86, R81,
C95, C100 AND B9 ONLY
WHEN U16 IS MOUNTED.

DEFAULT INSTRUCTION:
NOT MOUNTED



- 1) PLACE R86 CLOSER TO Y2
- 2) PROVIDE SHIELDING TO Y2

RESET CIRCUITRY



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| | | | |
| | | | |
| | | | |
| | | | |

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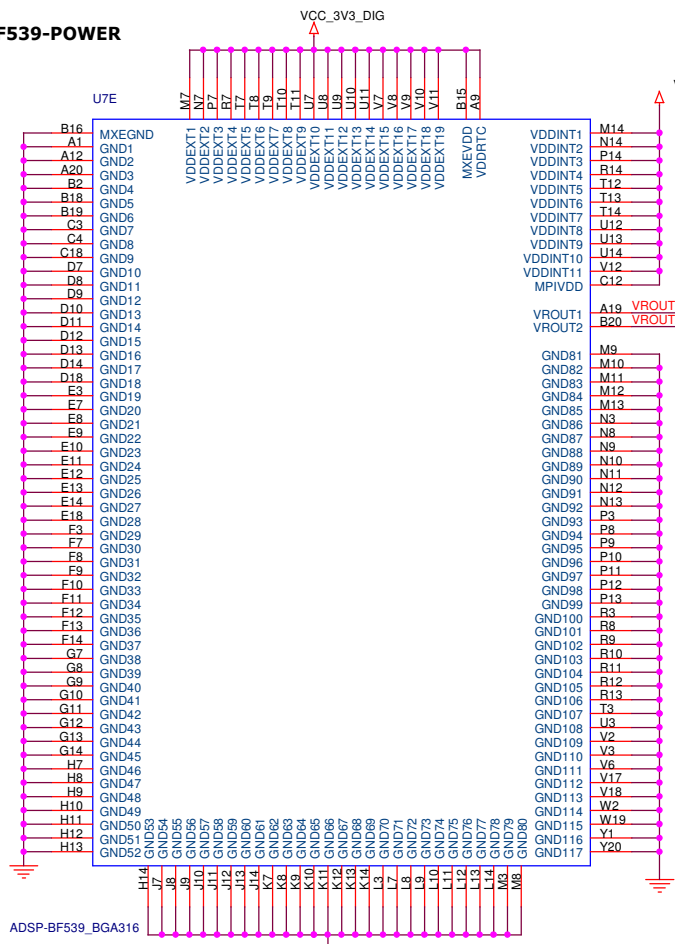
Drawn by: NAGALAKSHMI, SHAMEE
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Approved by: SridharTS
 Date: Thursday, October 28, 2004

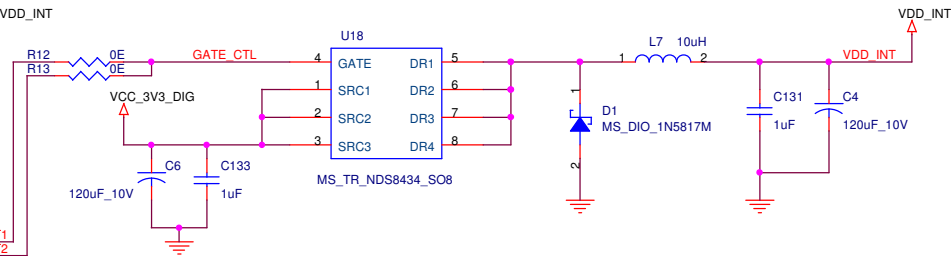
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| Title | | |
|-----------------|----------------------------|---------------|
| CLOCK AND RESET | | |
| Size | Document Number | Rev |
| B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 |
| Date: | Thursday, October 28, 2004 | Sheet 5 of 20 |

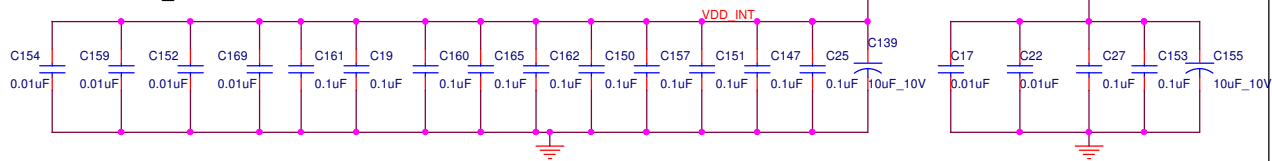
BF539-POWER



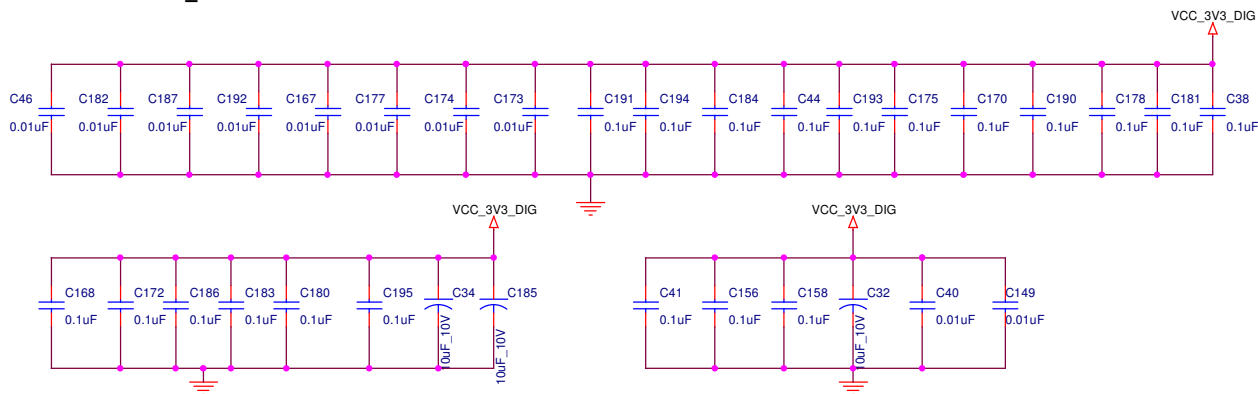
VDD_INT REGULATOR EXTERNAL CIRCUITRY



VDD_INT DECAPS FOR BF-539



VCC_3V3 DECAPS FOR BF-539



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| Title | | Rev | |
|-----------------------------------|----------------------------|-------|---------|
| BF539 POWER AND DECOUPLING | | 2.0 | |
| Size | Document Number | | |
| B | MSADI_HFCK_REV2.0_SCH-020 | | |
| Date: | Thursday, October 28, 2004 | Sheet | 7 of 20 |

- 1) PLACE ALL THE PULL-UP RESISTORS SHOWN BELOW CLOSE TO BLACKFIN (U7) .
- 2) PLACE R162, R155, R168, R170, R169, R56 CLOSE TO U7
- 3)DO NOT MOUNT R172, R64, R164, R57 AND R56
- 4)DO NOT MOUNT R173, R63 AND R171 IF U16 IS MOUNTED.

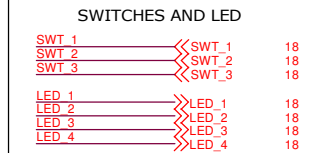
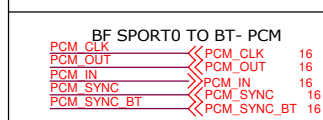
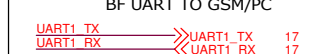
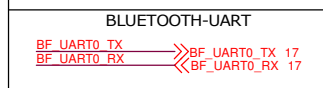
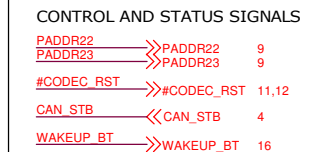
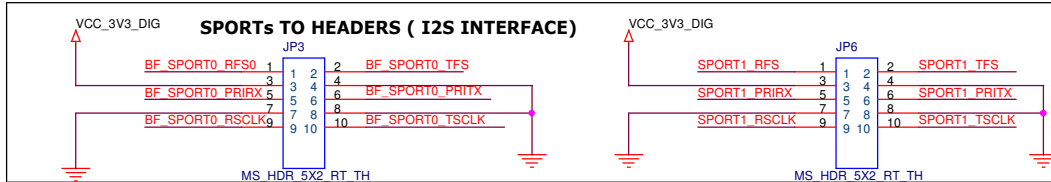
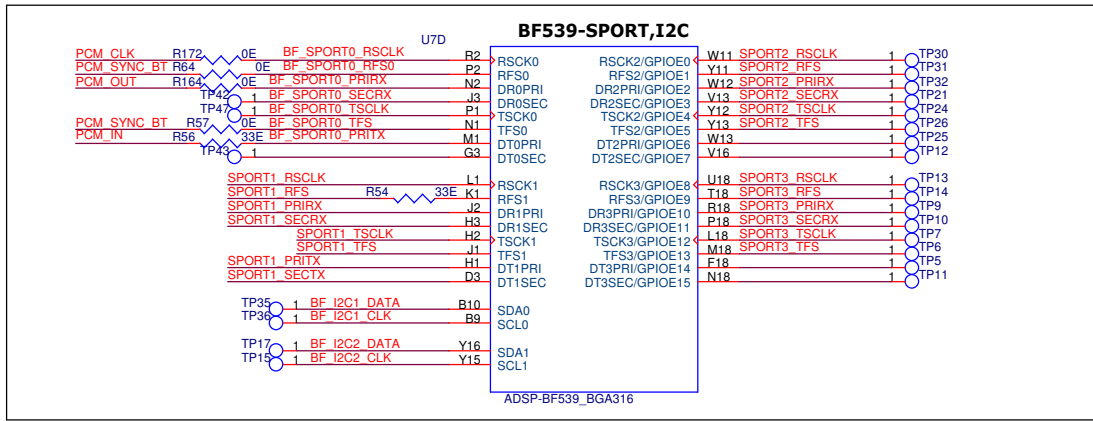
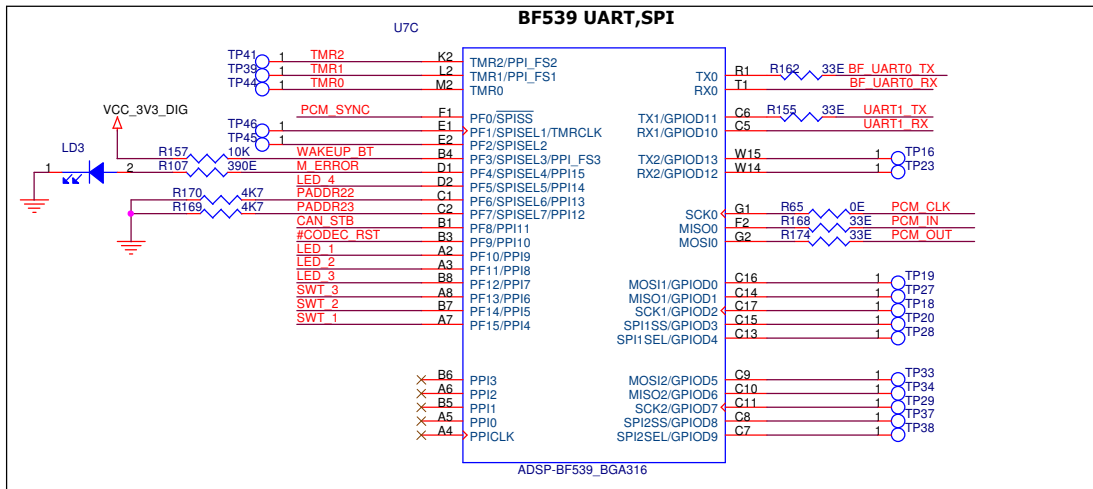
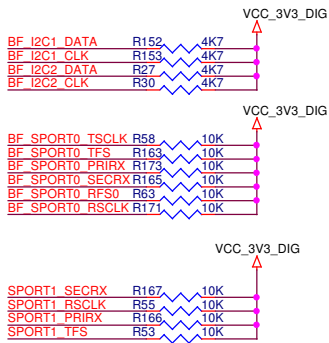
OPTION FOR CONNECTING BT-PCM TO BF-SPI0 OR BF-SPI1

OPTION1: TO CONNECT BT-PCM TO BF-SPI0
MOUNT R65, R168, R174, R182 AND R184.
DO NOT MOUNT R172, R64, R164, R57 AND R56

OPTION2: TO CONNECT BT-PCM TO BF-SPORT0
DO NOT MOUNT R65, R168, R174, R182 AND R184.

MOUNT R172, R64, R164, R57 AND R56

DEFAULT OPTION : BT-PCM TO BF-SPI0



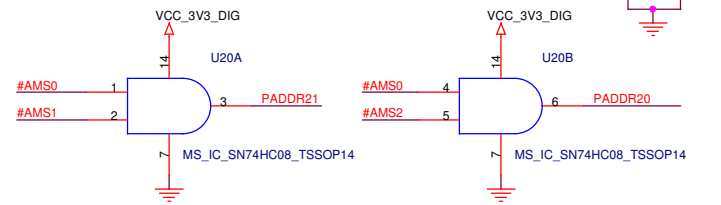
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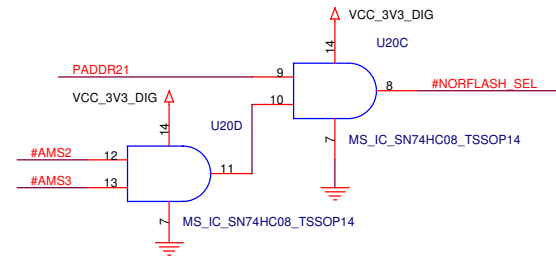
Drawn by: NAGALAKSHMI, SHAMEE Approved by: SridharTS
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Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN

| Title BF539 -SPORT,SPI,UART,FLAGS | | |
|--|----------------------------|---------------|
| Size | Document Number | Rev |
| B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 |
| Date: | Thursday, October 28, 2004 | Sheet 8 of 20 |

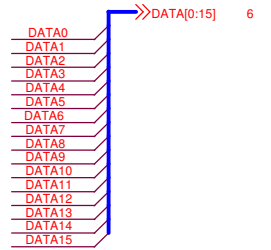
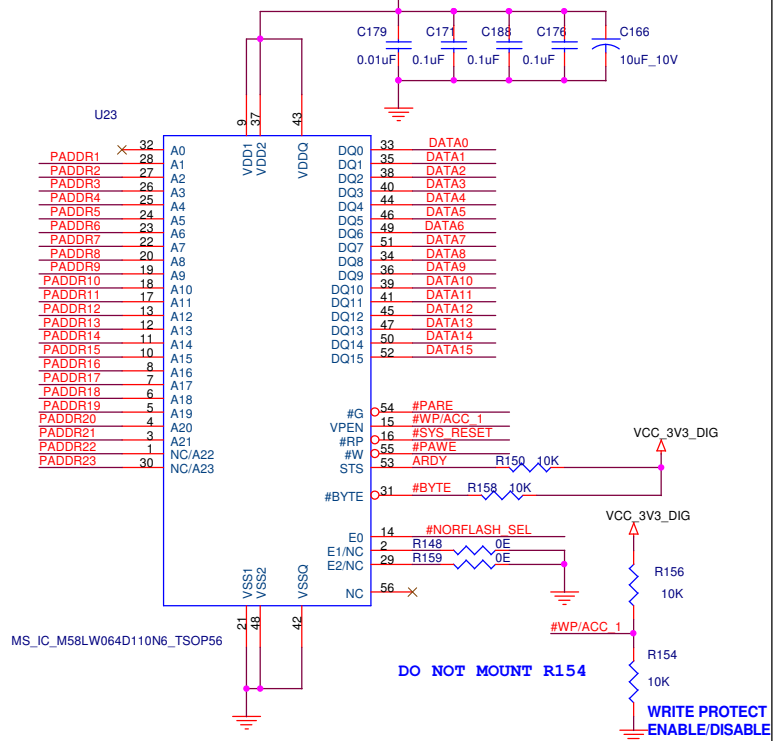
ADDRESS(A20 & A21) GENERATION



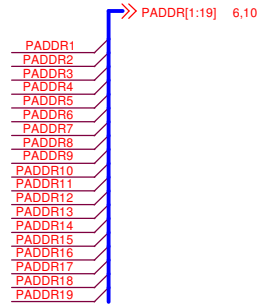
NOR FLASH CHIP SELECT LOGIC



NORFLASH (BOOT FLASH)



PROCESSOR ADDRESS BUS



CONTROL SIGNALS



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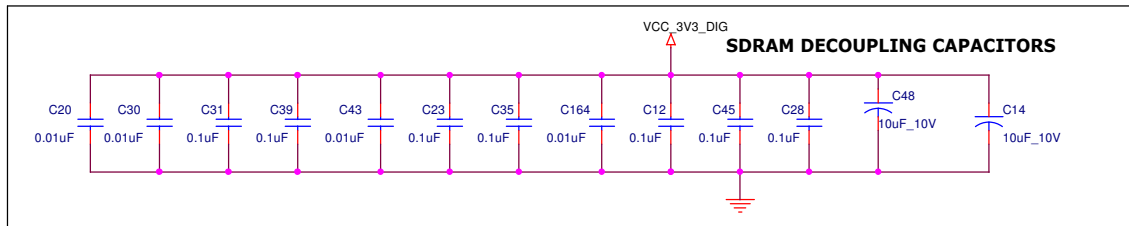
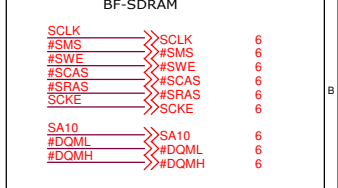
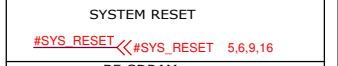
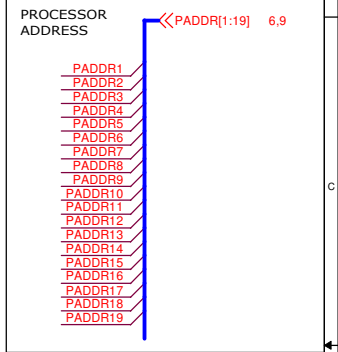
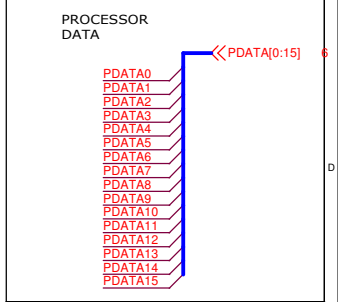
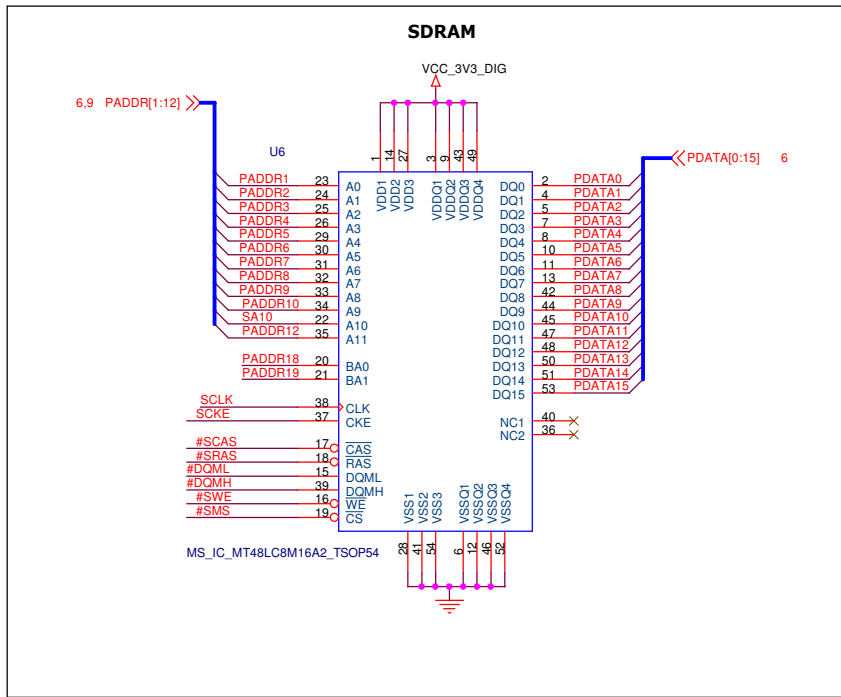
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Approved by: SridharTS
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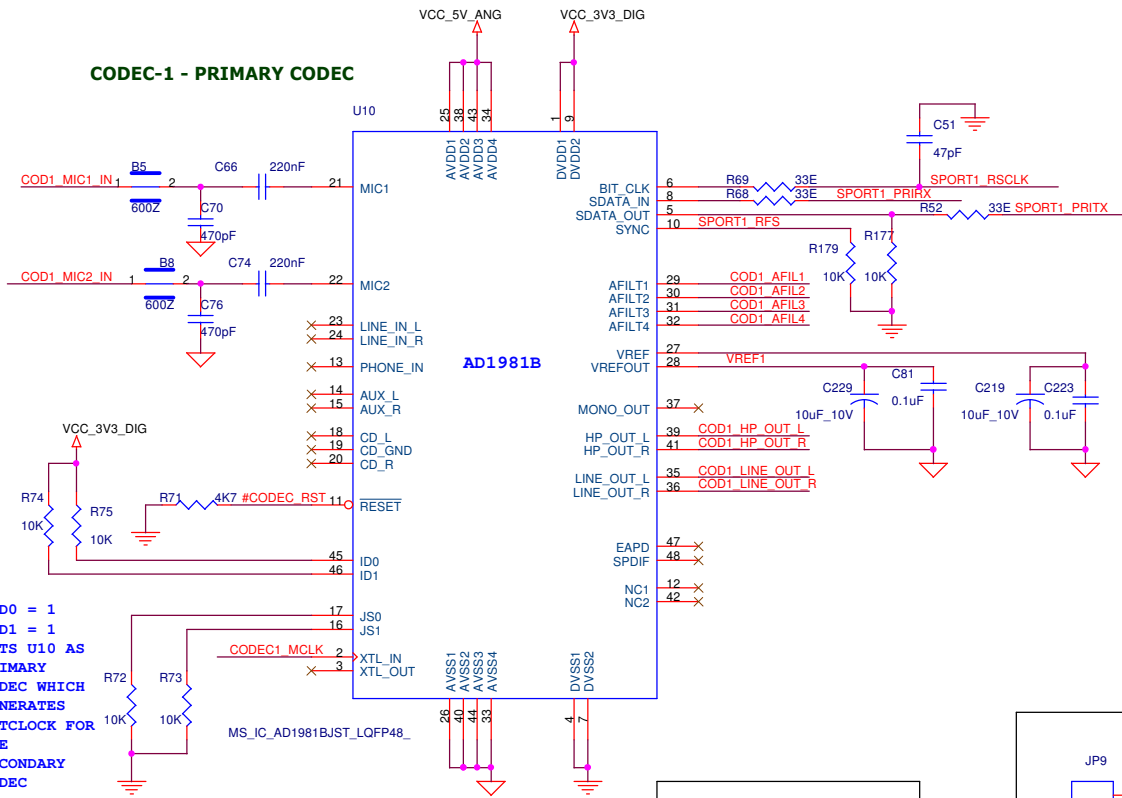
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| Title | | MEMORY LOGIC AND NOR FLASH | |
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| Size | Document Number | | Rev |
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| Date: | Thursday, October 28, 2004 | Sheet | 9 of 20 |

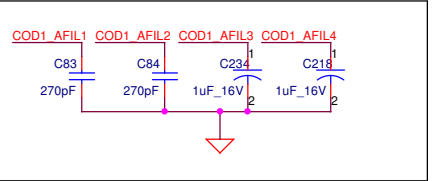


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| | | | | <p>#60 Adarsh regent, 100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-535 6400, Fax : +91-80-5356444</p> | | <p>SDRAM INTERFACE</p> | | B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 |
| | | | | <p>Drawn by: NAGALAKSHMI, SHAMEE Date: Wednesday, March 31, 2004</p> | <p>Approved by: SridharTS Date: Thursday, October 28, 2004</p> | | | | | |
| | | | | <p>Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH\020.DS</p> | | <p>Date: Thursday, October 28, 2004</p> | | | | Sheet 10 of 20 |

CODEC-1 - PRIMARY CODEC



#ID0 = 1
#ID1 = 1
SETS U10 AS
PRIMARY
CODEC WHICH
GENERATES
BITCLOCK FOR
THE
SECONDARY
CODEC

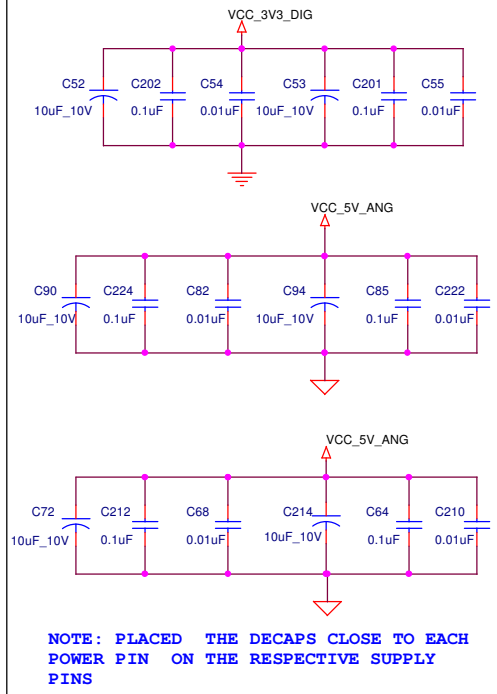


PLACE THE FILTER CAPACITORS NEAR TO THE RESPECTIVE PINS
PLACE B3 AND B6 NEAR TO CODEC -U8

PLACE R69,R68,C51
NEAR TO CODEC-U10

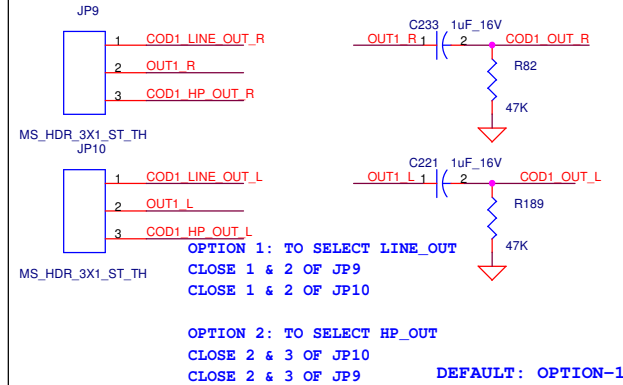
PLACE R52 NEAR TO BF
(U7)

DECAPS FOR AD1981



NOTE: PLACED THE DECAPS CLOSE TO EACH POWER PIN ON THE RESPECTIVE SUPPLY PINS

SELECTION OF CODEC OUTPUT CHANNEL



| SPORT SIGNALS | |
|---------------------------------|----------------------|
| SPORT1_PRIRX | >>>SPORT1_PRIRX 8 |
| SPORT1_PRITX | <<<SPORT1_PRITX 8 |
| SPORT1_RFS | <<<SPORT1_RFS 8.12 |
| SPORT1_RSCLK | >>>SPORT1_RSCLK 8.12 |
| CODEC CLOCK AND CONTROL SIGNALS | |
| #CODEC_RST | <<<#CODEC_RST 8.12 |
| CODEC1_MCLK | <<<CODEC1_MCLK 4.5 |
| VREF1 | >>>VREF1 13 |
| CODEC-1 AUDIO I/Os | |
| COD1_MIC2_IN | <<<COD1_MIC2_IN 13 |
| COD1_MIC1_IN | <<<COD1_MIC1_IN 13 |
| COD1_OUT_R | >>>COD1_OUT_R 15 |
| COD1_OUT_L | >>>COD1_OUT_L 15 |

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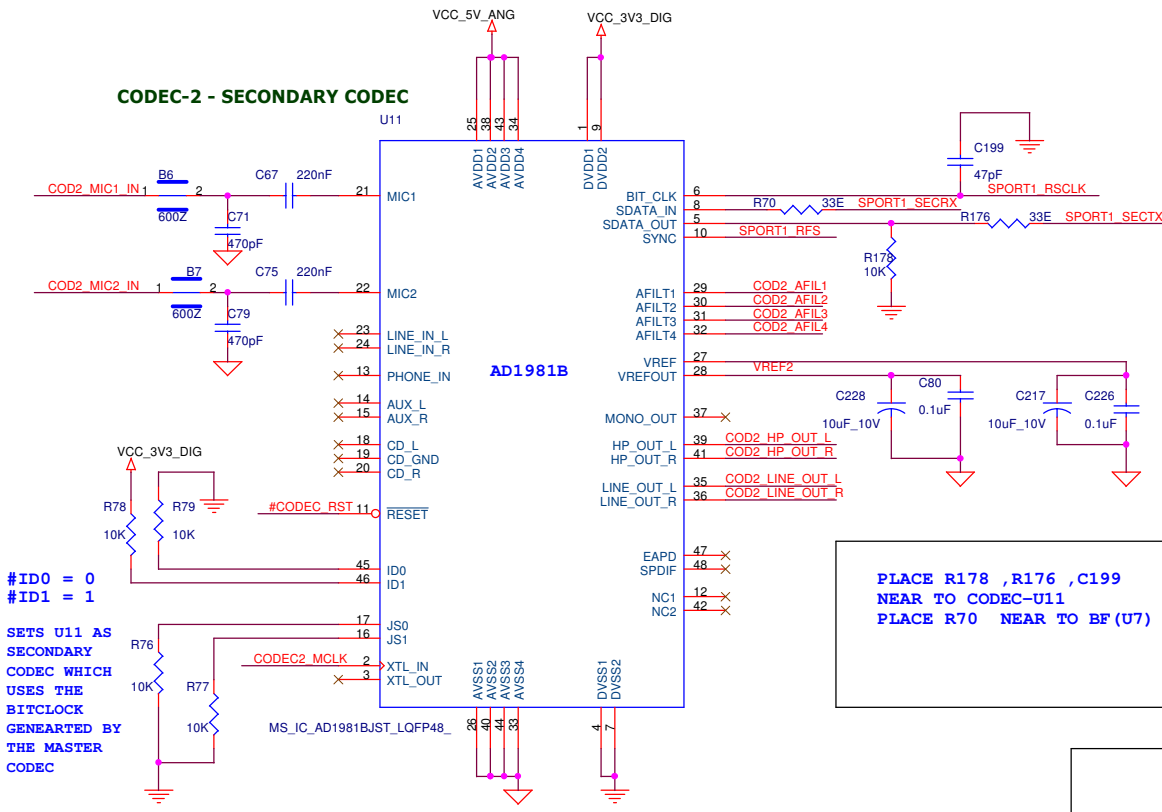
Drawn by: NAGALAKSHMI, SHAMEE
 Date: Wednesday, March 31, 2004

Approved by: SridharTS
 Date: Thursday, October 28, 2004

Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN

| Title | | MSADI_HFCK_REV2.0_SCH-020 | |
|---------------------------------|----------------------------|---------------------------|----------|
| AUDIO CODEC (AD1981B) -1 | | Size | Rev |
| | | B | 2.0 |
| Date: | Thursday, October 28, 2004 | Sheet | 11 of 20 |

CODEC-2 - SECONDARY CODEC

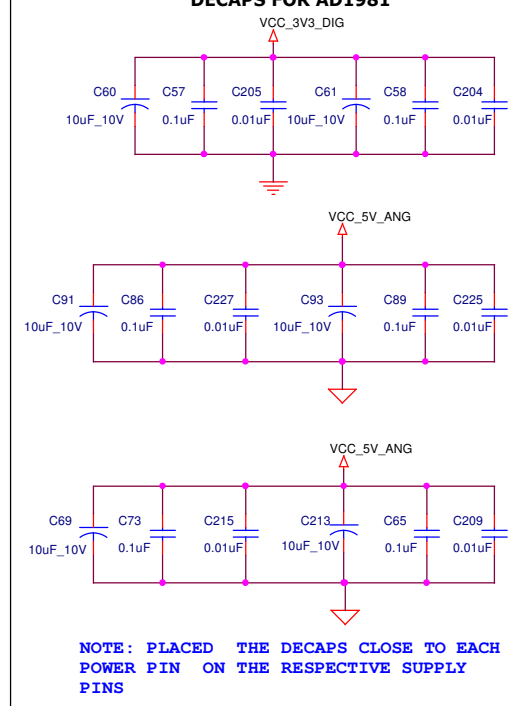


#ID0 = 0
#ID1 = 1

SETS U11 AS SECONDARY CODEC WHICH USES THE BITCLOCK GENERATED BY THE MASTER CODEC

PLACE R178 ,R176 ,C199 NEAR TO CODEC-U11
PLACE R70 NEAR TO BF (U7)

DECAPS FOR AD1981

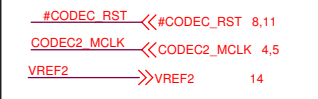


NOTE: PLACED THE DECAPS CLOSE TO EACH POWER PIN ON THE RESPECTIVE SUPPLY PINS

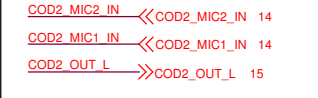
SPORT SIGNALS



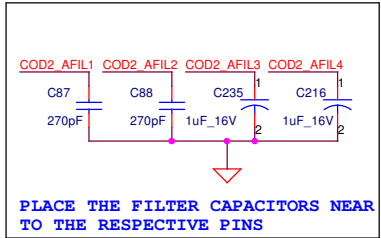
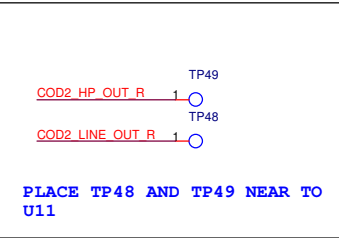
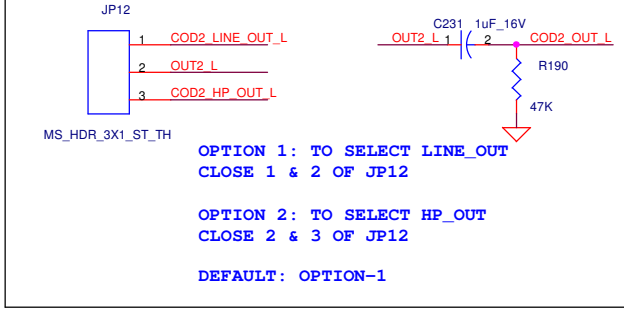
CODEC CLOCK AND CONTROL SIGNALS



CODEC-2 AUDIO I/Os

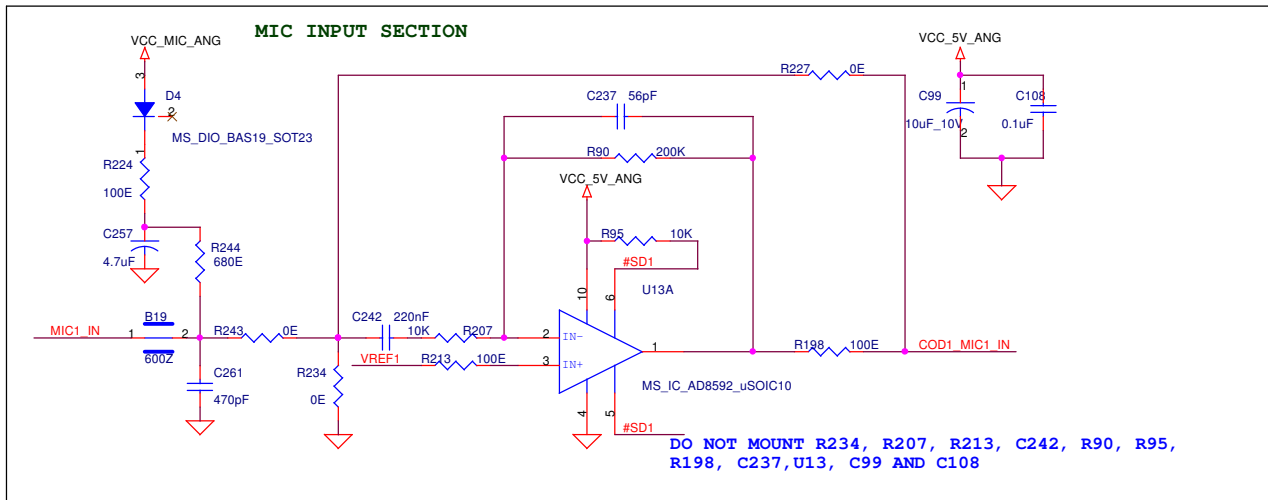


SELECTION OF CODEC OUTPUT CHANNEL TO SPEAKER

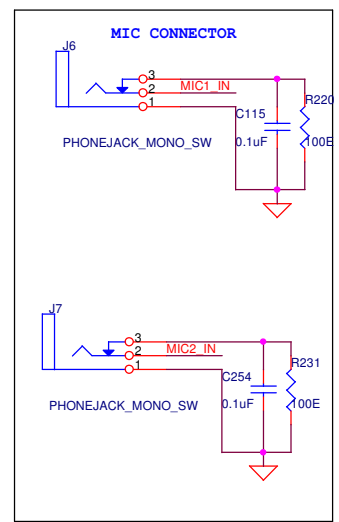
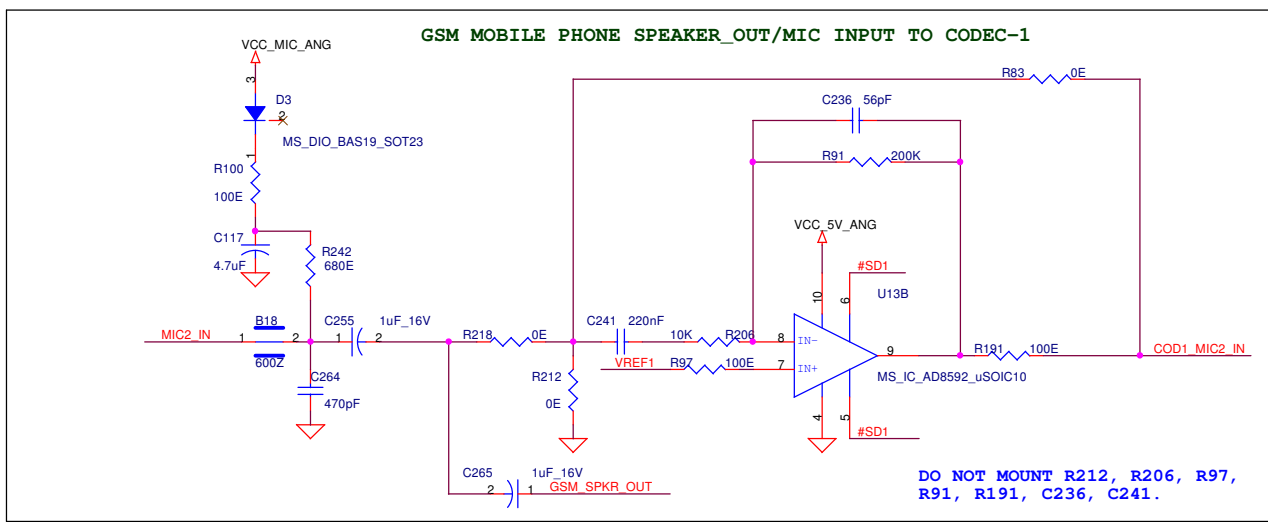


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|---------|------------------|-------------|------|---|----------------------------------|----------------------------------|--|----------------|
| | | | | Drawn by: NAGALAKSHMI, SHAMEE | Approved by: SridharTS | Size: B | Document Number: MSADI_HFCK_REV2.0_SCH-020 | Rev: 2.0 |
| | | | | Date: Wednesday, March 31, 2004 | Date: Thursday, October 28, 2004 | | | |
| | | | | Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | | Date: Thursday, October 28, 2004 | | Sheet 12 of 20 |

AUDIO INPUT SECTION FOR CODEC-1



| |
|---|
| GSM MOBILE PHONE AUDIO |
| <u>GSM_SPKR_OUT</u> << GSM_SPKR_OUT 17 |
| CODEC-1 MIC INPUT |
| <u>COD1_MIC1_IN</u> >>> COD1_MIC1_IN 11 |
| <u>COD1_MIC2_IN</u> >>> COD1_MIC2_IN 11 |
| CONTROL SIGNALS |
| <u>VREF1</u> <<< VREF1 11 |



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Drawn by: NAGALAKSHMI, SHAMEE
 Date: Wednesday, March 31, 2004

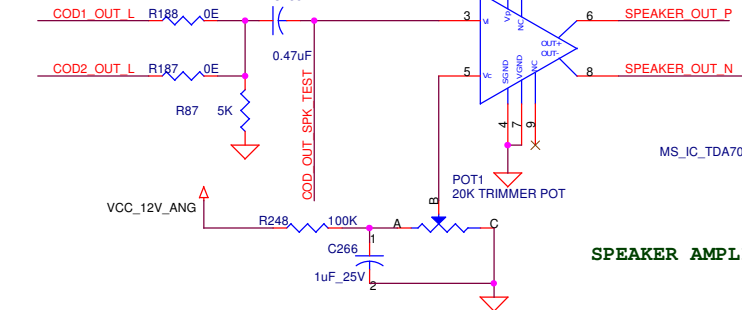
Approved by: SridharTS
 Date: Thursday, October 28, 2004

Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN

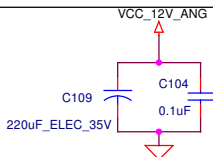
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|------------------------------------|----------------|--------|---|---------|
| Title AUDIO INPUT SECTION-1 | | Size B | Document Number MSADI_HFCK_REV2.0_SCH-020 | Rev 2.0 |
| Date: Thursday, October 28, 2004 | Sheet 13 of 20 | | | |

CODEC-1 AUDIO OUTPUT SECTION

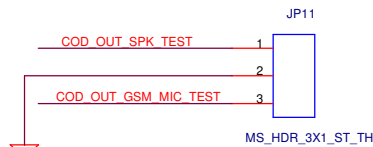
DO NOT MOUNT R187



SPEAKER AMPLIFIER SECTION

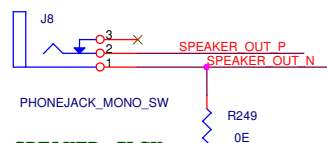


AUDIO TEST HEADER



SPEAKER JACK

DO NOT MOUNT R249



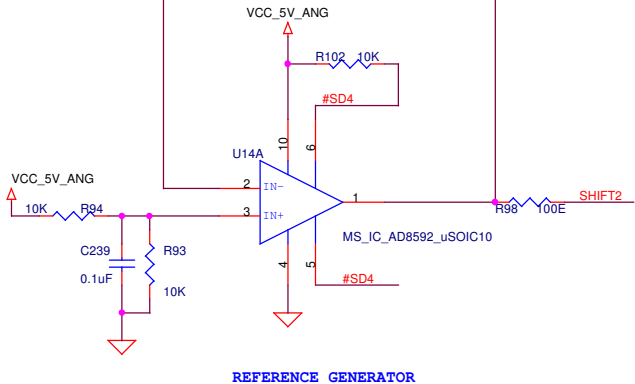
CODEC DAC OUTPUTS

COD1_OUT_R << COD1_OUT_R 11
 COD1_OUT_L << COD1_OUT_L 11
 COD2_OUT_L << COD2_OUT_L 12

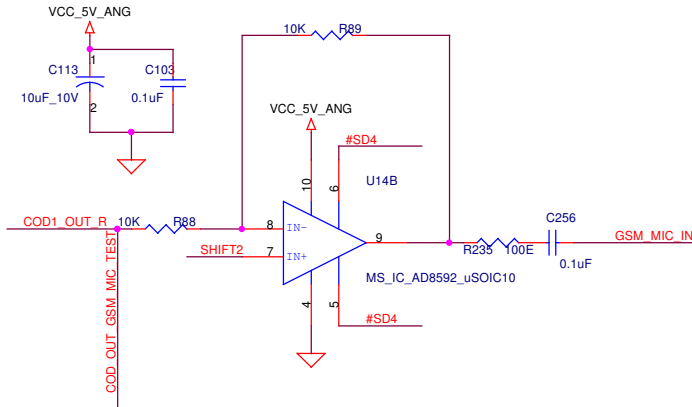
AMPLIFIER OUTPUTS

GSM_MIC_IN >> GSM_MIC_IN 17

GSM MOBILE PHONE MIC INPUT



REFERENCE GENERATOR



NOTE: THE VALUE OF C256 MAY BE CHANGED DURING TESTING DEPENDING ON THE LOAD (GSM HANDSET) RESISTANCE.

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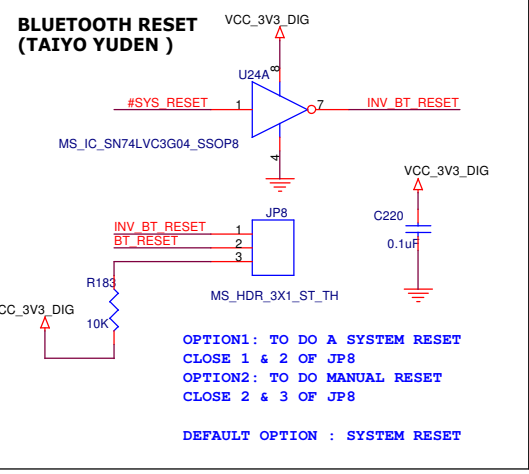
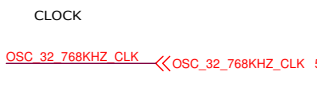
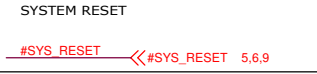
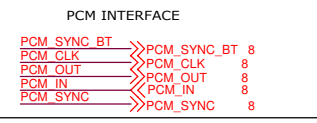
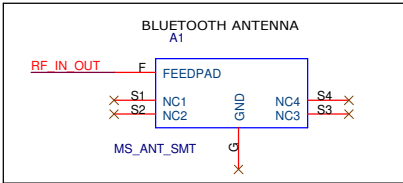
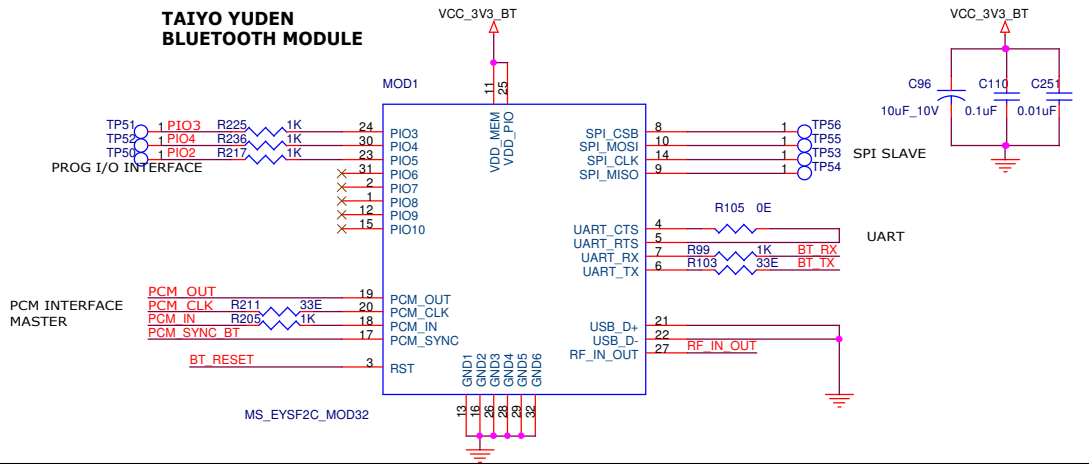
Drawn by: NAGALAKSHMI, SHAMEE
 Date: Wednesday, March 31, 2004

Approved by: SridharTS
 Date: Thursday, October 28, 2004

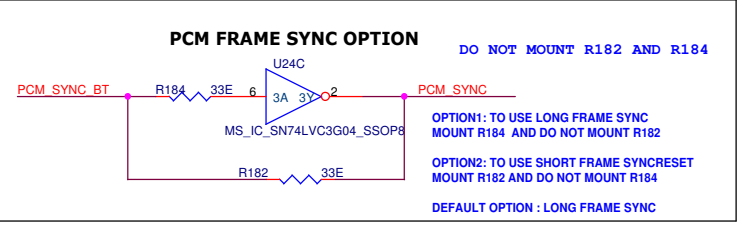
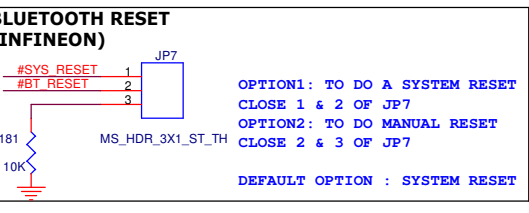
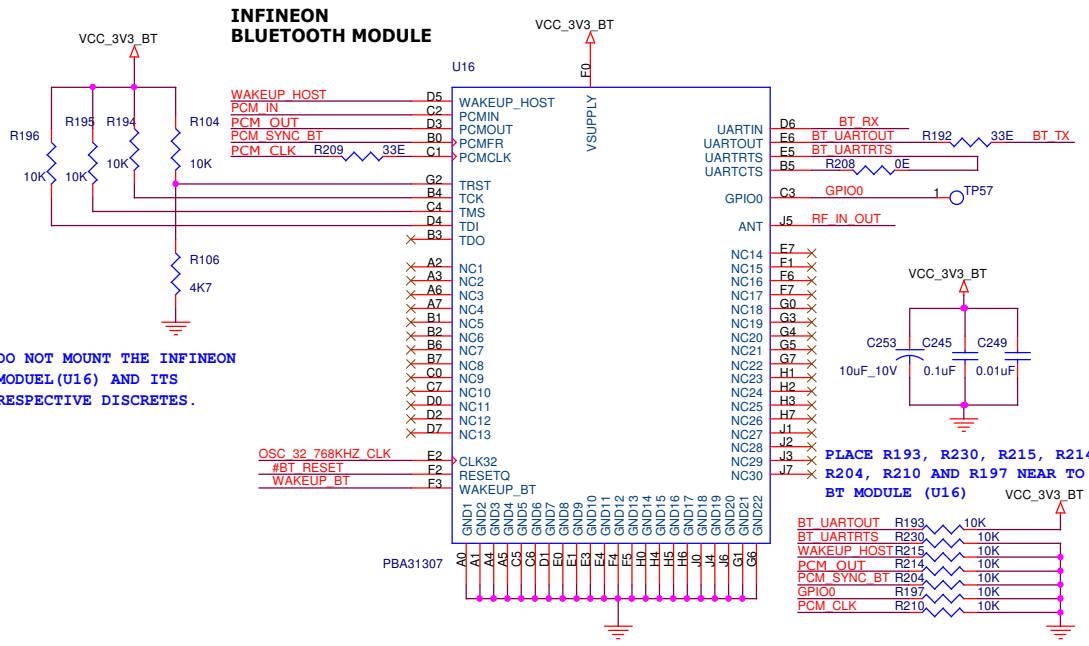
Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN

| Title | | AUDIO OUTPUT SECTION | |
|-------|----------------------------|----------------------|----------|
| Size | Document Number | Rev | |
| B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 | |
| Date: | Thursday, October 28, 2004 | Sheet | 15 of 20 |

**TAIYO YUDEN
BLUETOOTH MODULE**

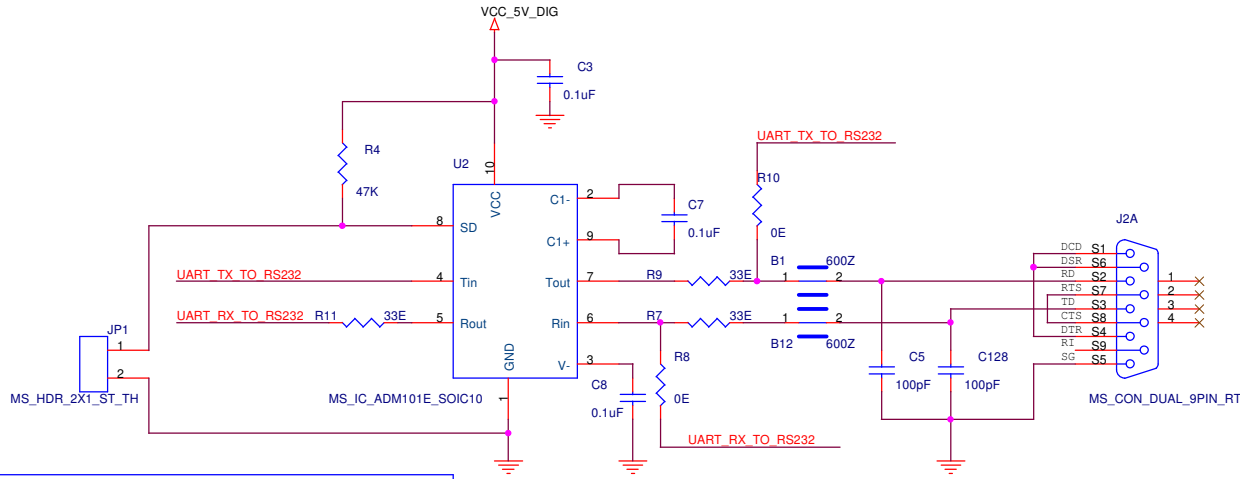


**INFINEON
BLUETOOTH MODULE**

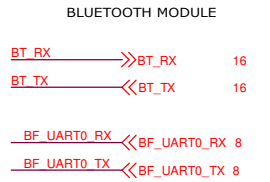
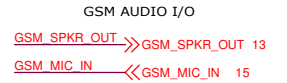
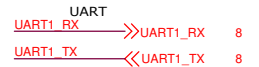


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| | | | | #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-535 6400, Fax : +91-80-5356444 | | BLUETOOTH INTERFACE |
| | | | | Drawn by: NAGALAKSHMI, SHAMEE Date: Wednesday, March 31, 2004 | Approved by: SridharTS Date: Thursday, October 28, 2004 | Size: B Document Number: MSADI_HFCK_REV2.0_SCH-020 |
| | | | | Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | | Date: Thursday, October 28, 2004 Sheet 16 of 20 |

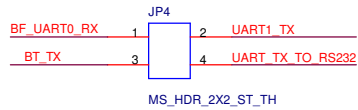
GSM MOBILE PHONE DATA PORT/RS232 INTERFACE



- 1) SHORT LINK JP1 TO TURN ON RS-232 TRANSCEIVER
- 2) PLACE R11, R9 CLOSE TO U2
- 3) PLACE R7 AND B12 NEAR TO J2.
- 4) DONOT MOUNT R10, R8



SELECTION OF UART INTERFACE - BLACKFIN TO PC/GSM OR BLUETOOTH TO PC OR BT TO BF

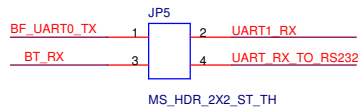
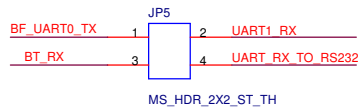


OPTION 1: TO CONNECT BLACKFIN UART1 TO PC
CLOSE 2 & 4 OF JP4
CLOSE 2 & 4 OF JP5

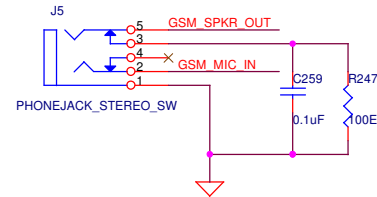
OPTION 2: TO CONNECT BLUETOOTH UART TO BF UART0
CLOSE 1 & 3 OF JP4
CLOSE 1 & 3 OF JP5

OPTION 3: TO CONNECT BLUETOOTH UART TO PC
CLOSE 3 & 4 OF JP4
CLOSE 3 & 4 OF JP5

DEFAULT OPTION: BF UART1 TO PC AND BF UART0 TO BT



GSM MOBILE PHONE AUDIO PORT INTERFACE CONNECTOR



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Bangalore 560 071, Ph : +91-80-535 6400, Fax : +91-80-5356444

Title **GSM MOBILE PHONE INTERFACE**

Drawn by: NAGALAKSHMI, SHAMEE
Date: Wednesday, March 31, 2004

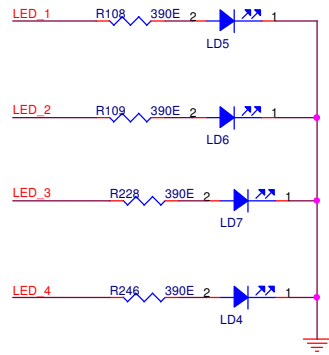
Approved by: SridharTS
Date: Thursday, October 28, 2004

Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DS

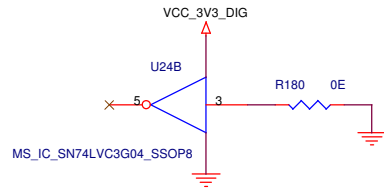
Size B Document Number MSADI_HFCK_REV2.0_SCH-020 Rev 2.0

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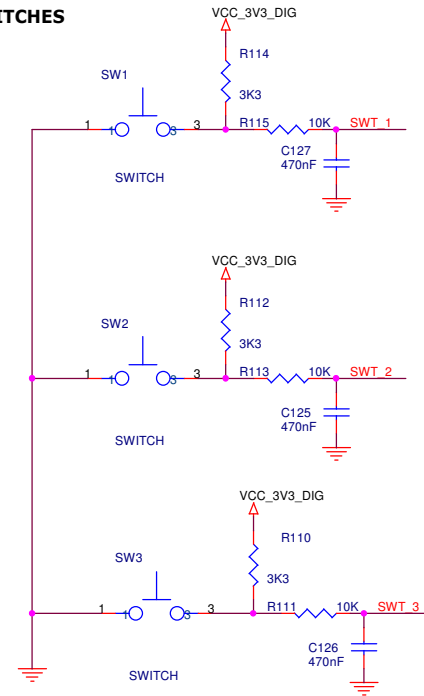
LED INTERFACE TO BLACKFIN



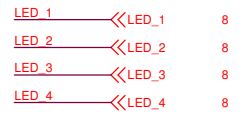
UNUSED GATE



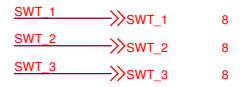
SWITCHES



LEDs



SWITCHES



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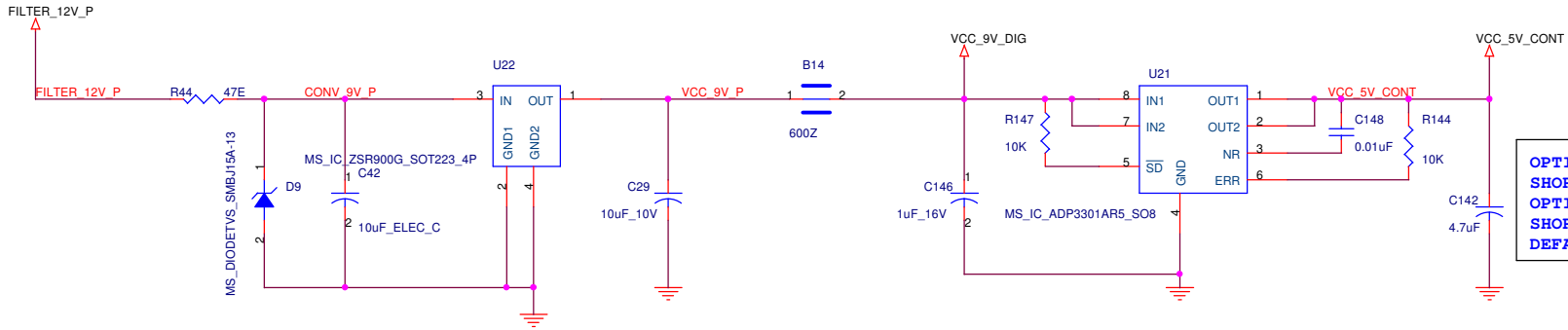
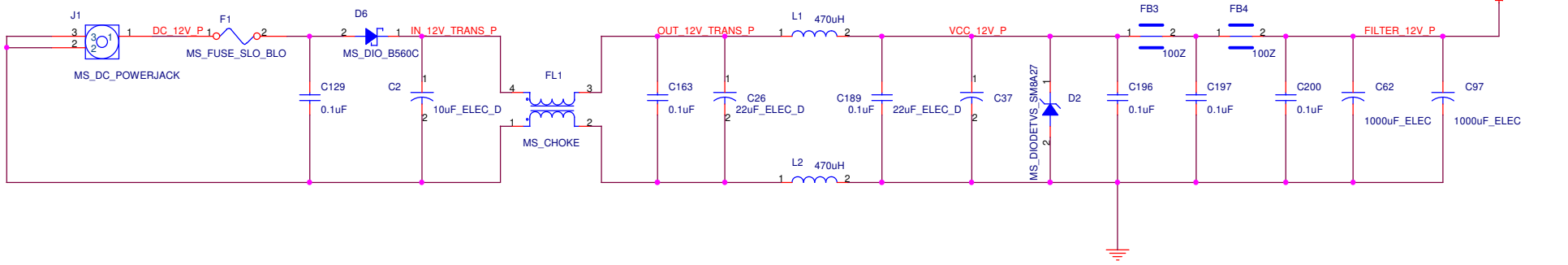
Drawn by: NAGALAKSHMI, SHAMEE Approved by: SridharTS
 Date: Wednesday, March 31, 2004 Date: Thursday, October 28, 2004

Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DS

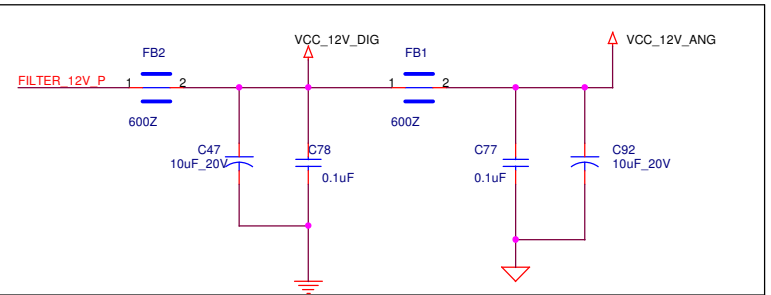
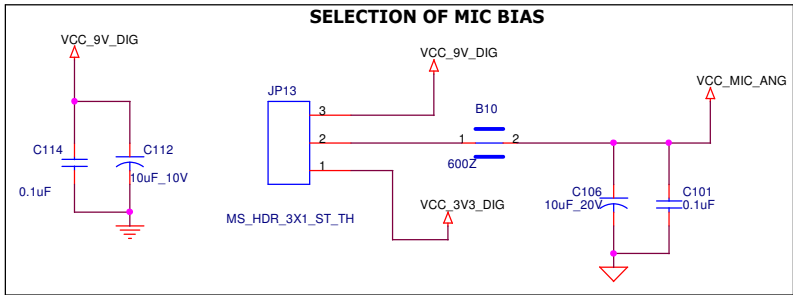
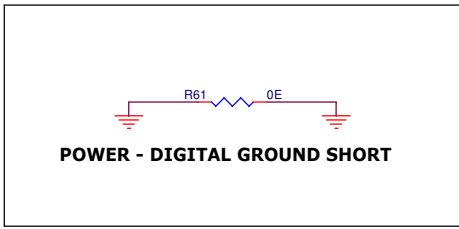
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|----------------------------------|----------------|--------|---|---------|
| Title LEDs AND SWITCHES | | Size B | Document Number MSADI_HFCK_REV2.0_SCH-020 | Rev 2.0 |
| Date: Thursday, October 28, 2004 | Sheet 18 of 20 | | | |

AUTOMOTIVE EMI/ EMC FILTER, LOAD DUMP TRANSIENT & REVERSE VOLTAGE PROTECTION

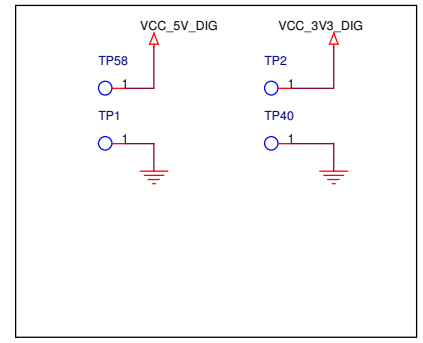
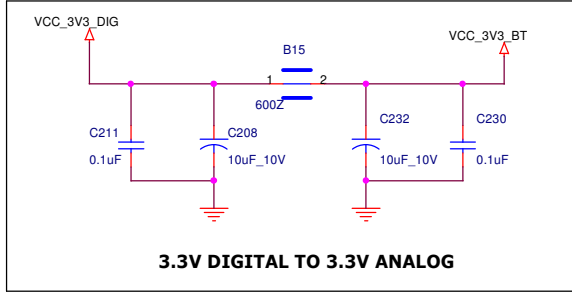
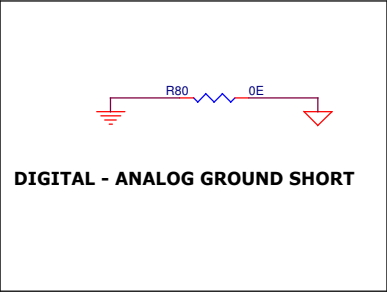
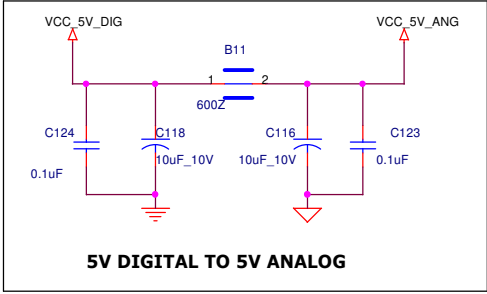
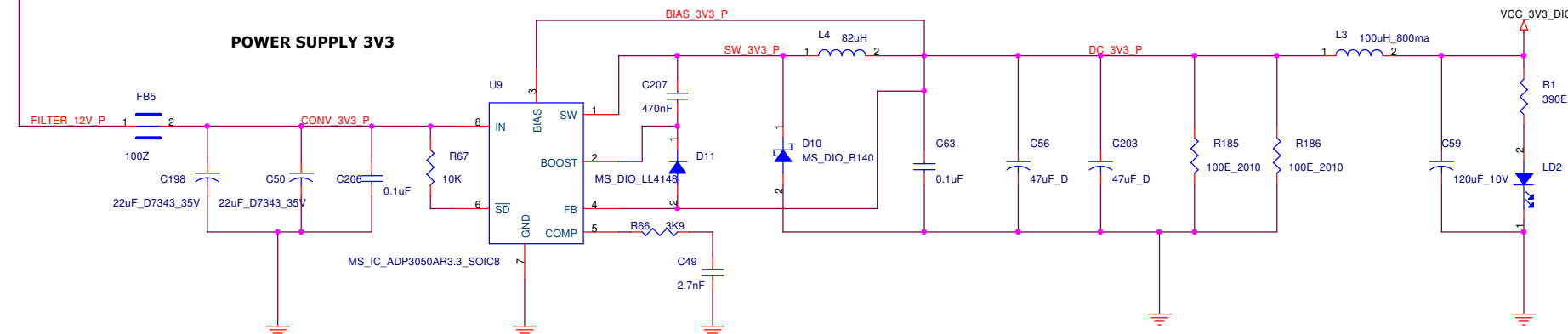
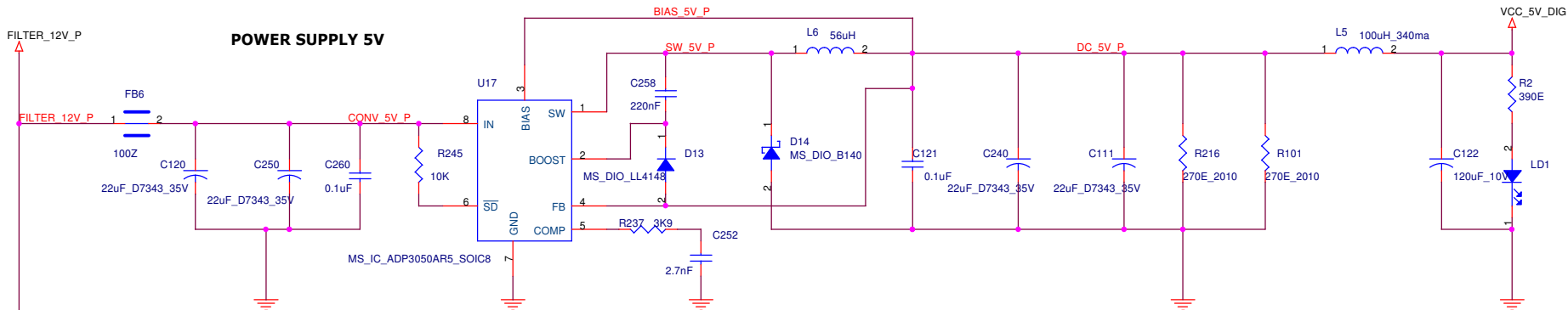
**12 VOLTS
FILTERED
O/P**



**OPTION 1: SELECT 8V BIAS TO MIC
SHORT PIN 2 & 3 OF JP13.
OPTION 2: SELECT 2.5V BIAS TO MIC
SHORT PIN 1 & 2 OF JP13.
DEFAULT: OPTION 2.**



| | | | | | | | |
|--|------------------|-------------|------|---|--|--|---|
| REV NO. | NATURE OF CHANGE | APPROVED BY | DATE | <p>Mistral Software [P] Ltd. #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-535 6400, Fax : +91-80-5356444</p> | Title POWER SUPPLY FILTER & FOT_5V_CONT | | |
| | | | | | Drawn by: NAGALAKSHMI, SHAMEE Date: Wednesday, March 31, 2004 | Approved by: SridharTS Date: Thursday, October 28, 2004 | Size: B Document Number: MSADI_HFCK_REV2.0_SCH-020 |
| Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | | | | Date: Thursday, October 28, 2004 | Sheet: 19 of 20 | | |



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|---------|------------------|-------------|------|---|----------------------------------|-------|----------------------------|----------------|
| | | | | Drawn by: NAGALAKSHMI, SHAMEE | Approved by: SridharTS | Size | Document Number | Rev |
| | | | | Date: Wednesday, March 31, 2004 | Date: Thursday, October 28, 2004 | B | MSADI_HFCK_REV2.0_SCH-020 | 2.0 |
| | | | | Design file path: D:\PROJECTS\HFCK\REV2.0\SCHEMATICS\020\MS_ADI_HFCK_REV2.0_SCH020.DSN | | Date: | Thursday, October 28, 2004 | Sheet 20 of 20 |