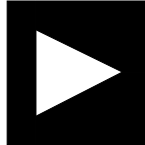
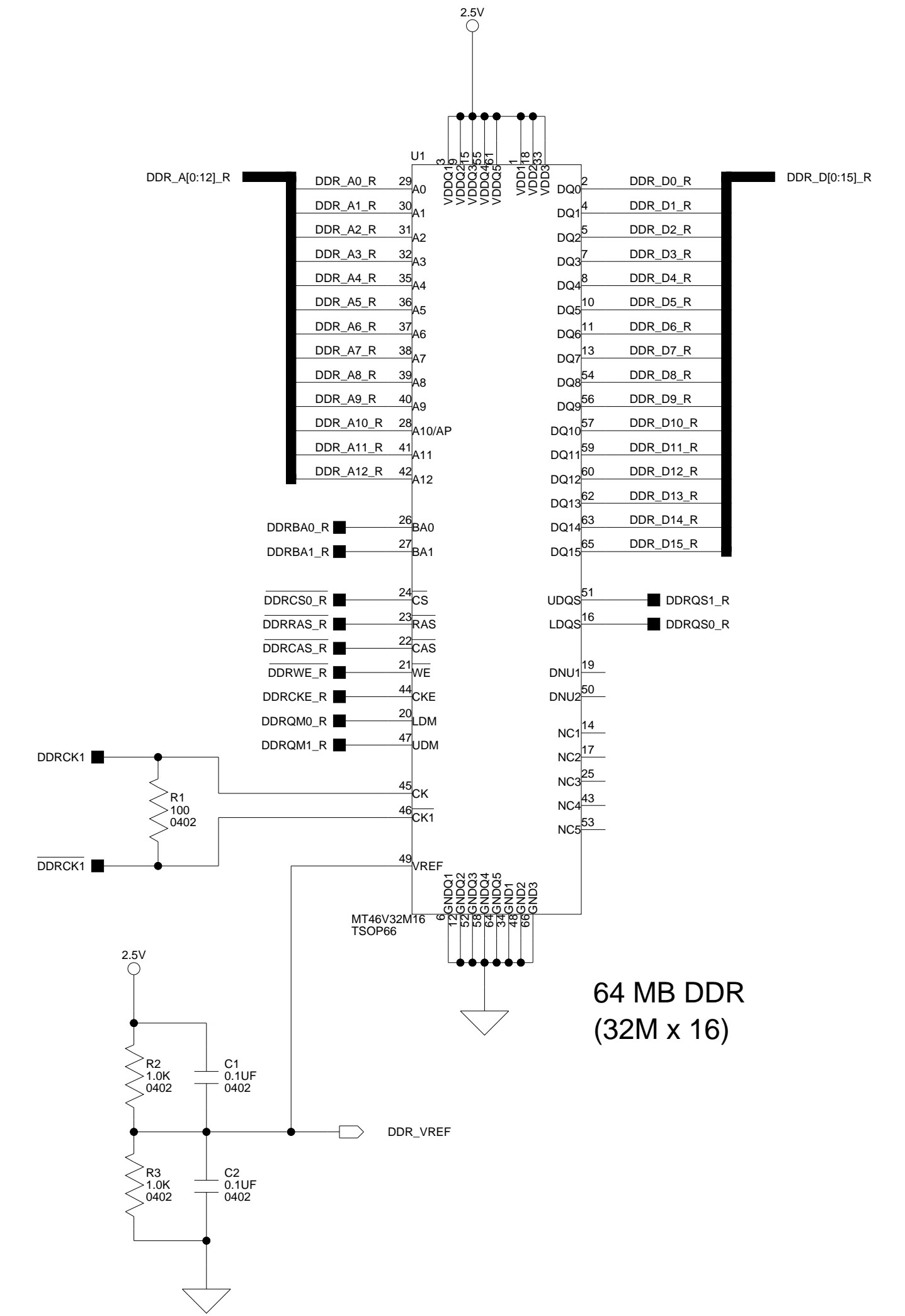
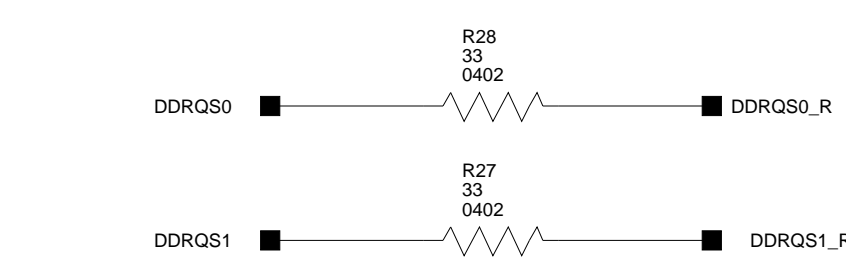
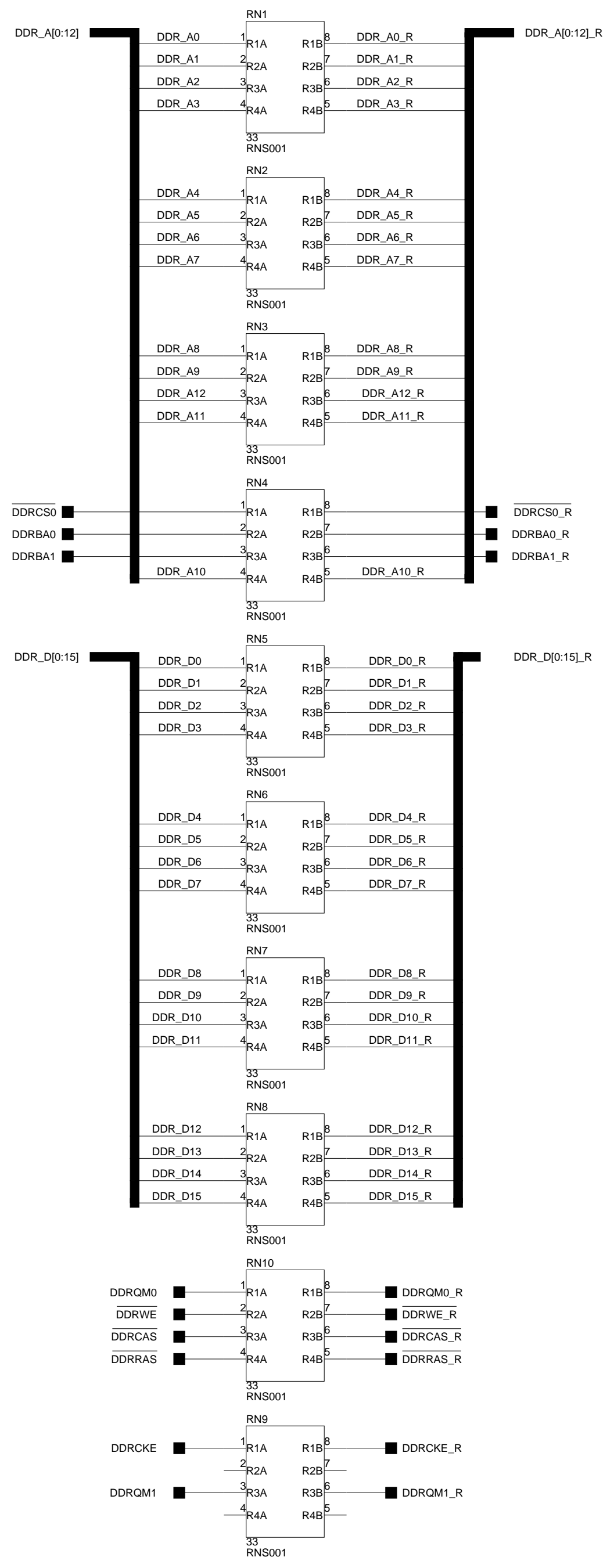
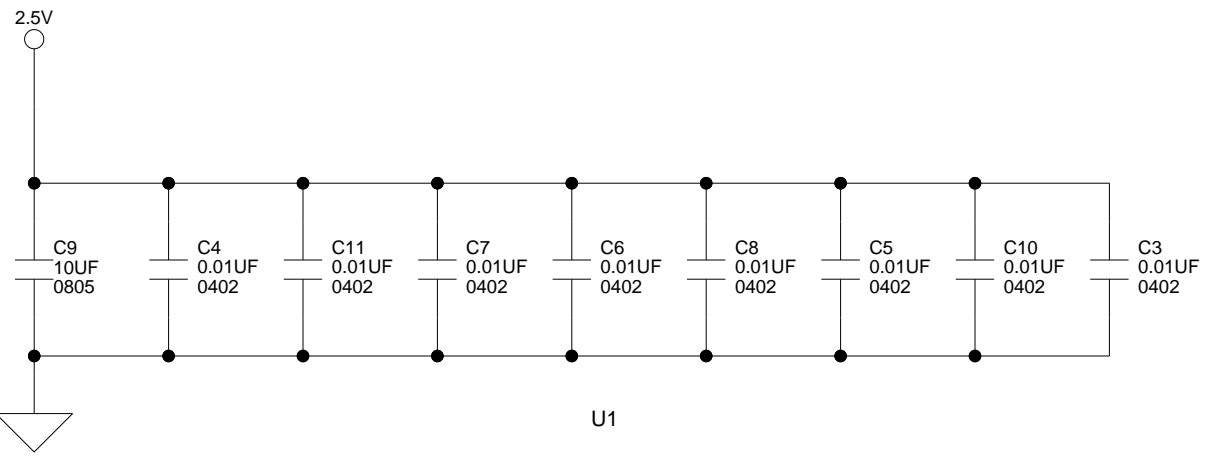
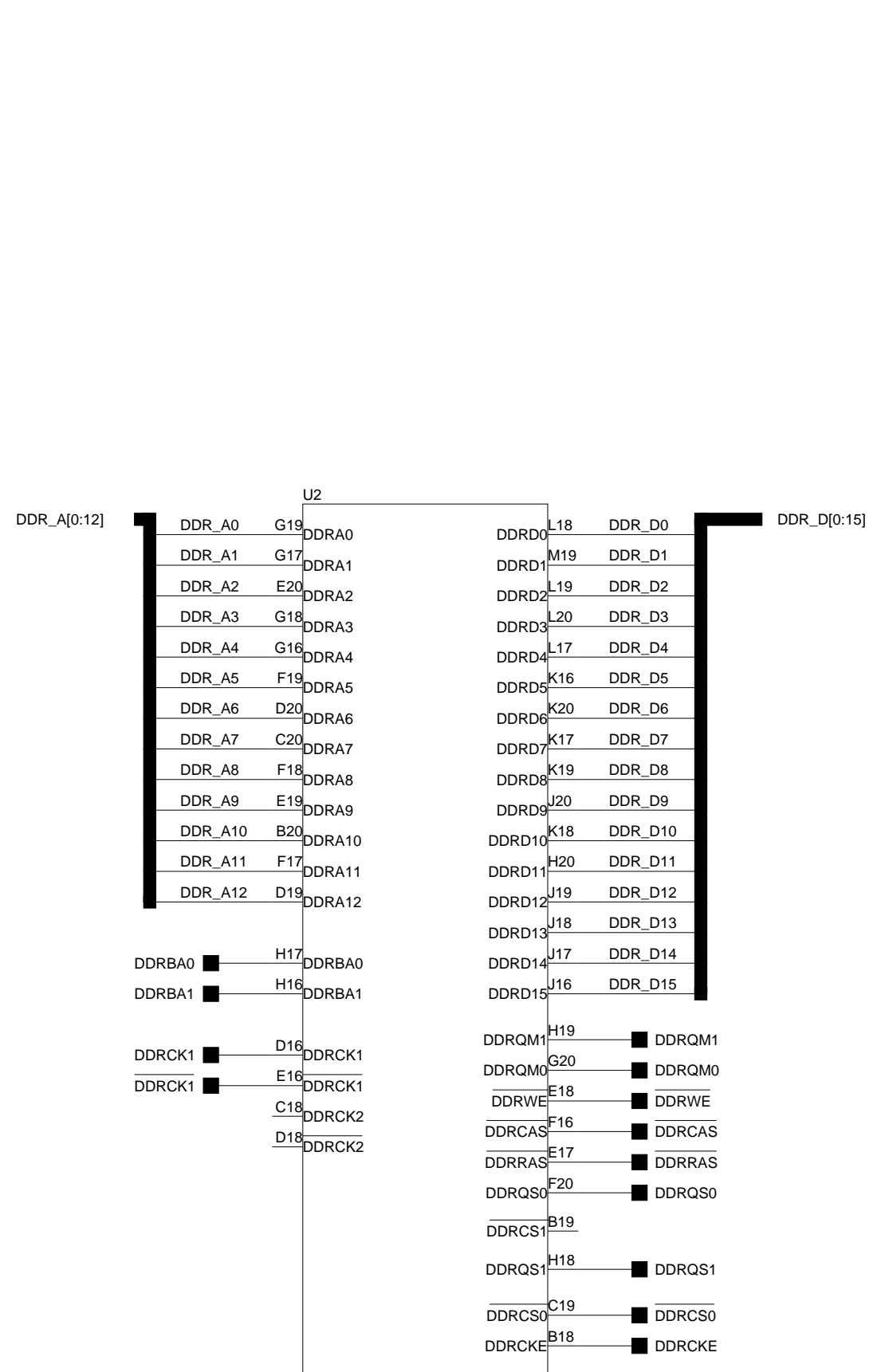
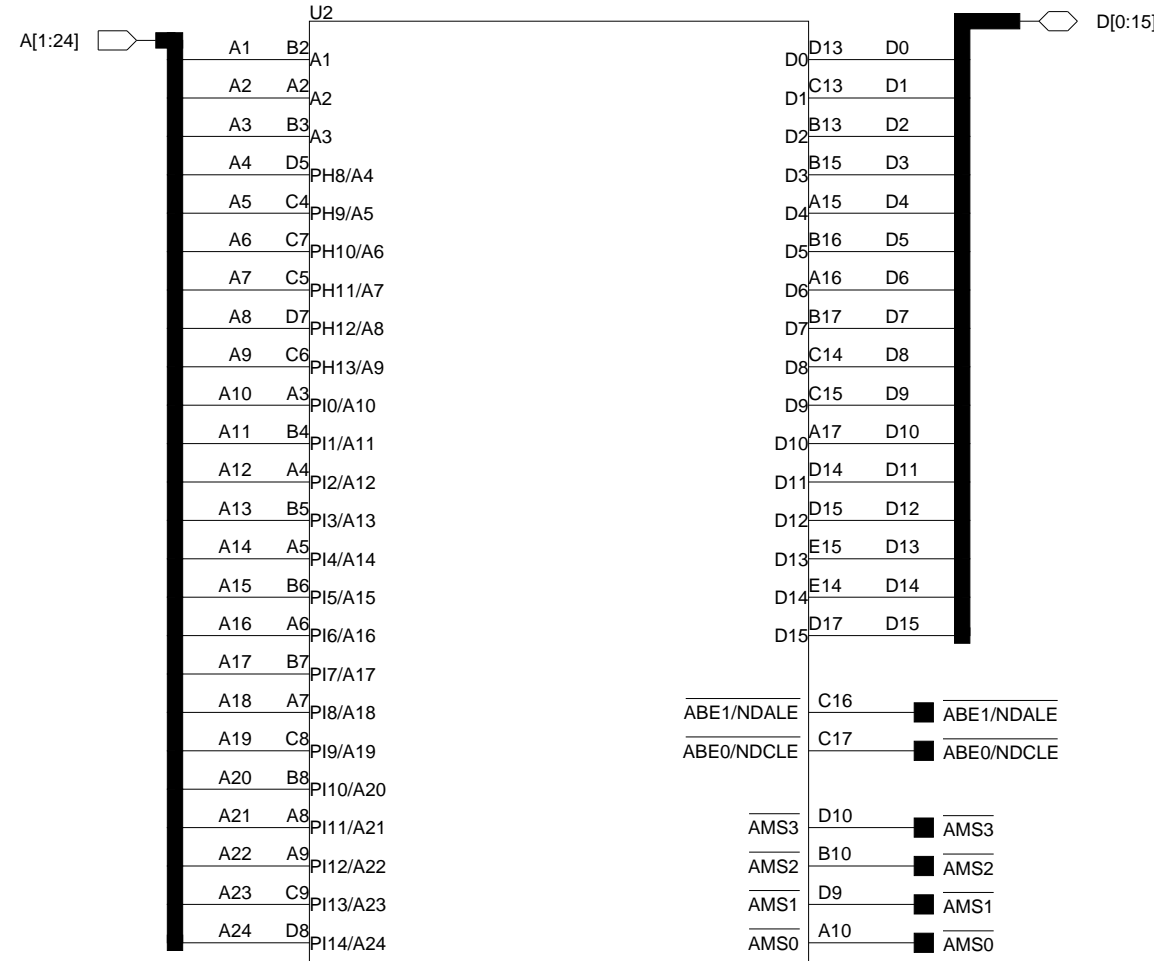


ADSP-BF548 EZ-KIT LITE SCHEMATIC

		ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD
Title		ADSP-BF548 EZ-KIT LITE TITLE	
Size C	Board No.	A0206-2006	Rev 1.4B
Date	12-4-2007_10:10	Sheet	1 of 17



		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF548 EZ-KIT LITE DDR INTERFACE	
Size C	Board No. A0206-2006	Rev 1.4B	
Date 12-4-2007_10:10	Sheet 2 of 17		

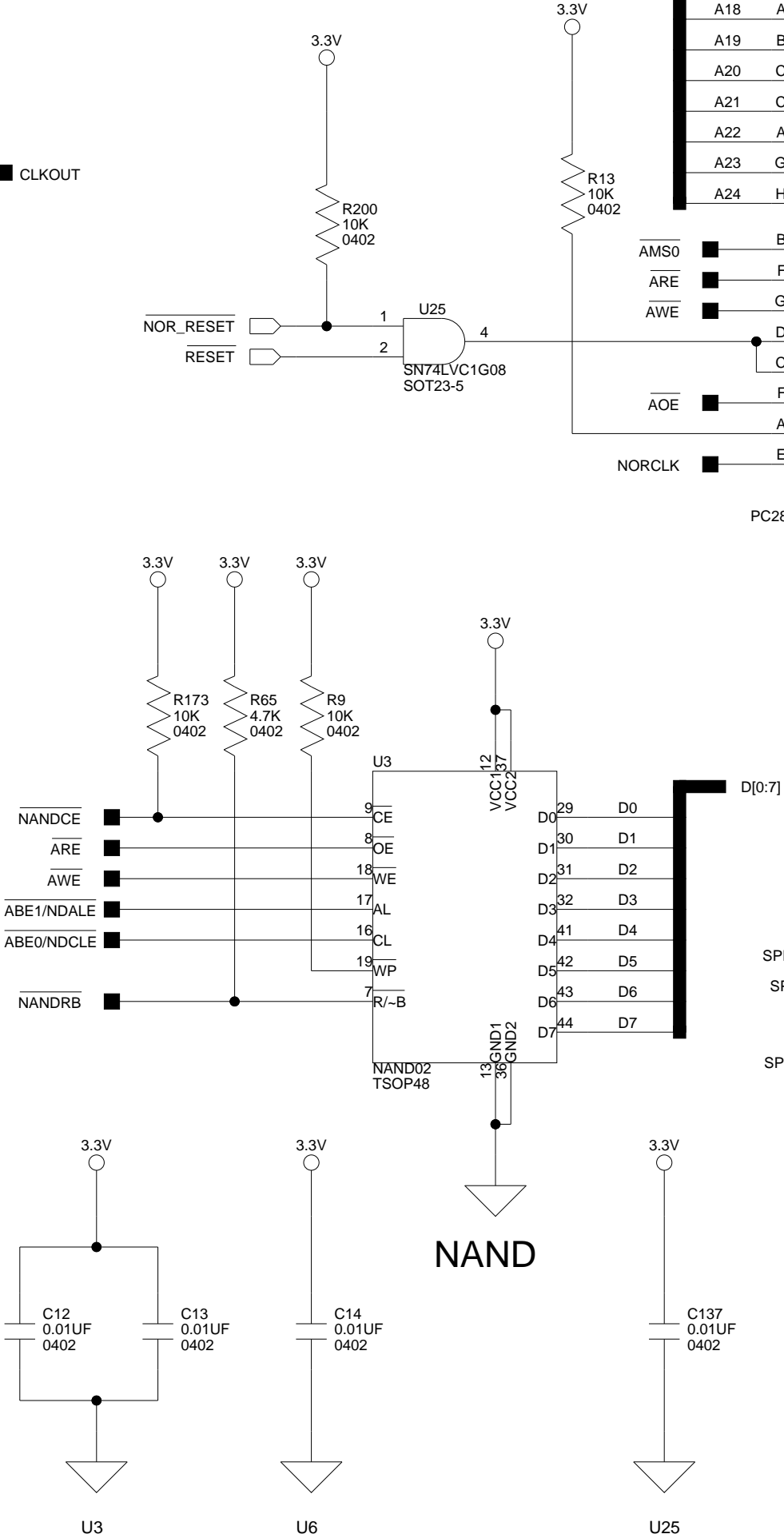
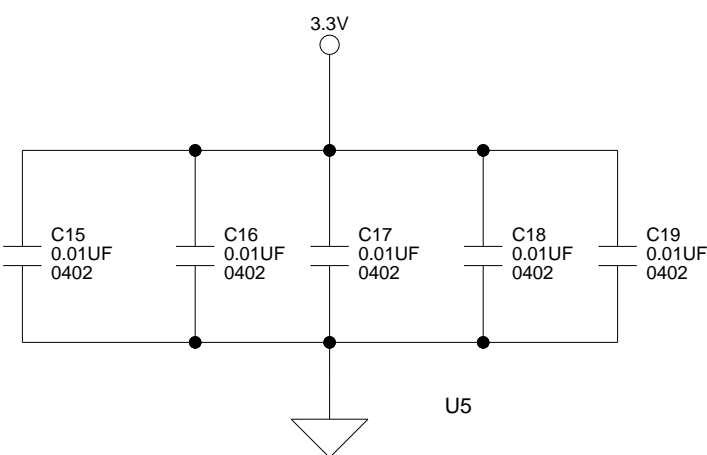


- ABE1/NDALE C16 ■ ABE1/NDALE
- ABE0/NDCLE C17 ■ ABE0/NDCLE
- AMS3 D10 ■ AMS3
- AMS2 B10 ■ AMS2
- AMS1 D9 ■ AMS1
- AMS0 A10 ■ AMS0
- AOE C10 ■ AOE
- ARE B12 ■ ARE
- AWE D12 ■ AWE
- CLKOUT L16 ■ CLKOUT
- PI15/A25/NORCLK B9 ■ NORCLK
- PJ0/AMCARDY/NORWAIT R20 ■ NORWAIT
- PJ1/NANDCE# N18 ■ NANDCE
- PJ2/NANDRB# M16 ■ NANDRB
- PJ3/ATAPIDIOR# T20 ■ ATAPIDIOR
- PJ4/ATAPIDIOW# N17 ■ ATAPIDIOW
- PJ5/ATAPICS0# U20 ■ ATAPICS0
- PJ6/ATAPICS1# P18 ■ ATAPICS1
- PJ7/ATAPIDMACK# N16 ■ ATAPIDMACK
- PJ8/ATAPIDMARQ# R19 ■ ATAPIDMARQ
- PJ9/ATAPIINTRQ P17 ■ ATAPIINTRQ
- PJ10/ATAPIORDY T19 ■ ATAPIORDY
- ATAPIPIA P19 ■ ATAPIPIA
- PJ11/BR# M17 ○ BR/PJ11
- PJ12/BG# P20 ○ BG/PJ12
- PJ13/BGH# N19 ○ BGH/PJ13

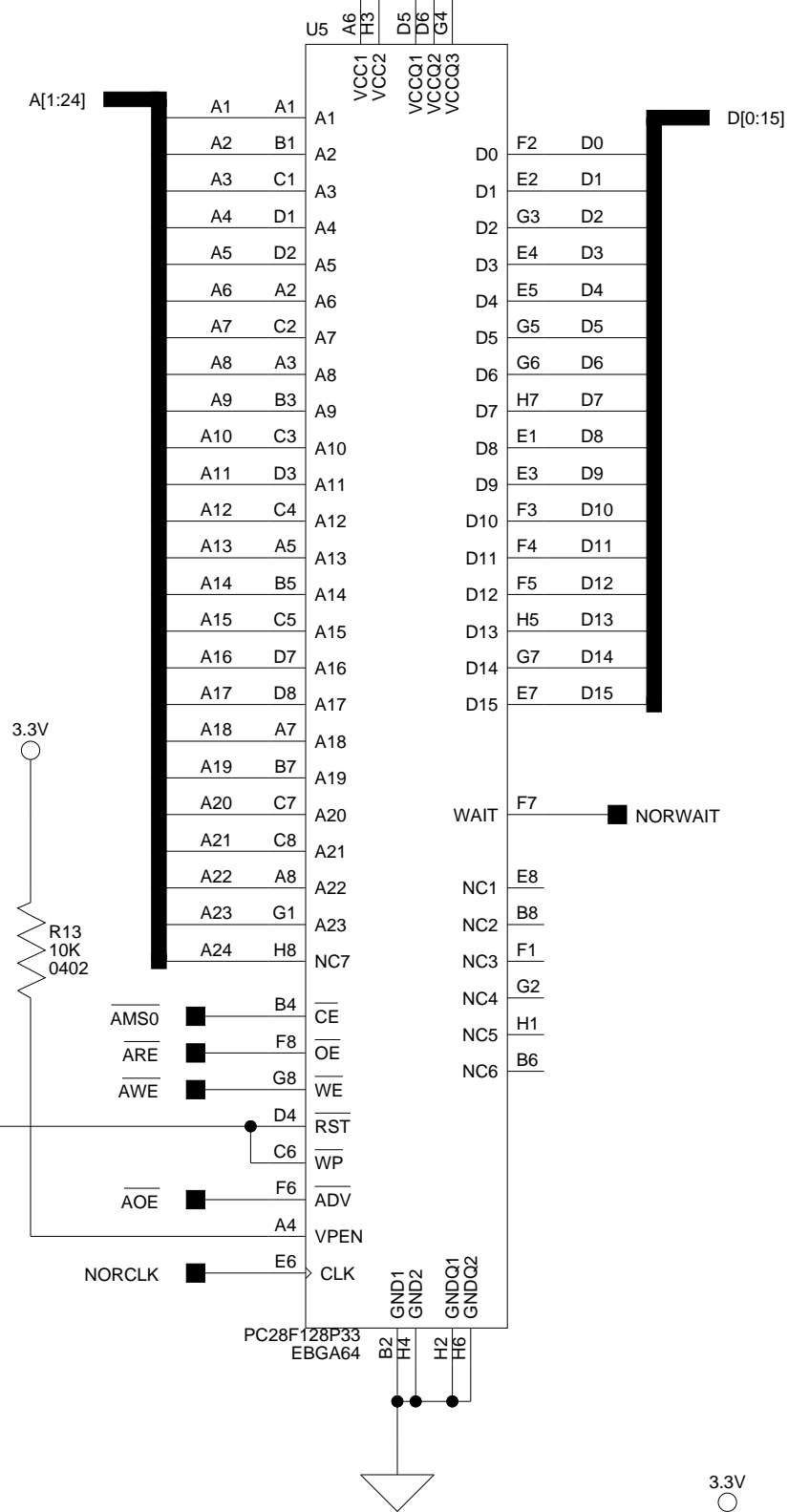
ADSP-BF548
MBGA400

Memory Map

START	END	BANK	DEVICE
0x0000 0000	0x01FF FFFF	DDR Bank 0	64MB DDR
0x2000 0000	0x21FF FFFF	ASYNC Memory Bank 0	32MB BURST FLASH
0x2400 0000	0x2400 007F	ASYNC Memory Bank 1	ETHERNET
0x2800 0000	0x27FF FFFF	ASYNC Memory Bank 2	NOT USED
0x2C00 0000	0x2FFF FFFF	ASYNC Memory Bank 3	NOT USED

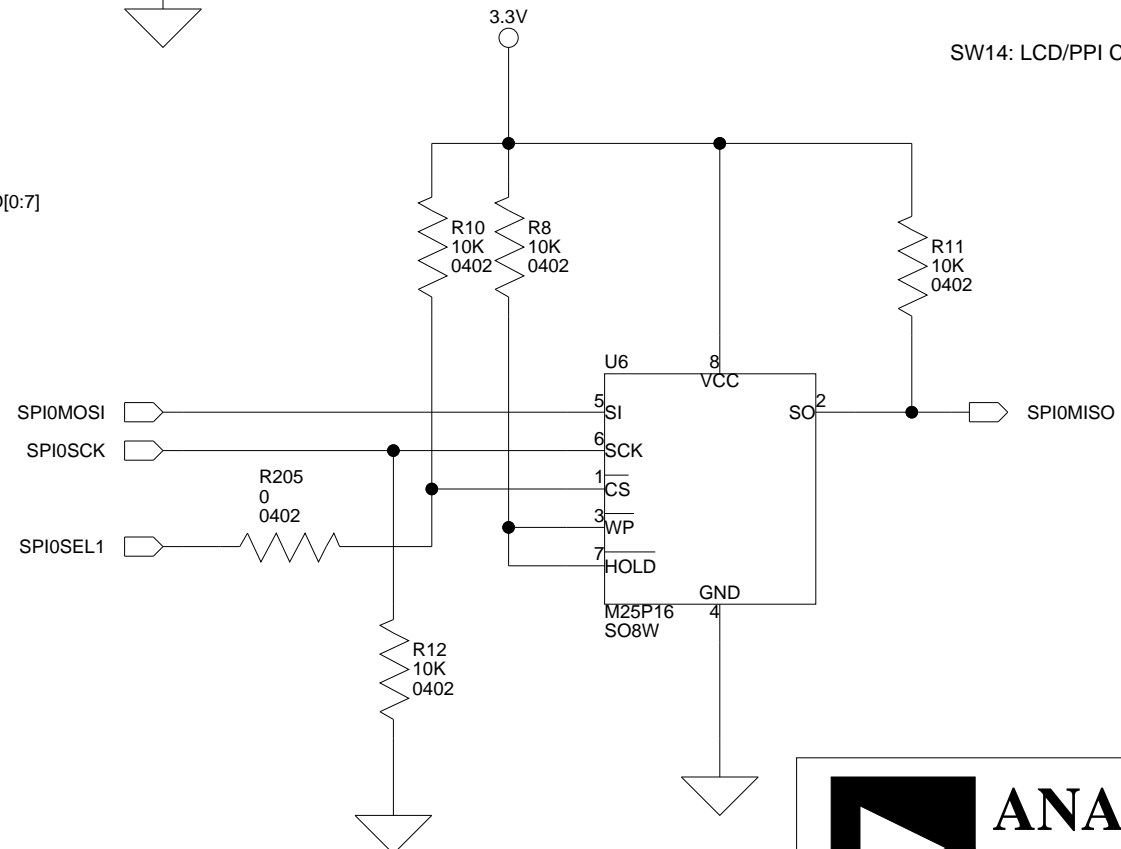
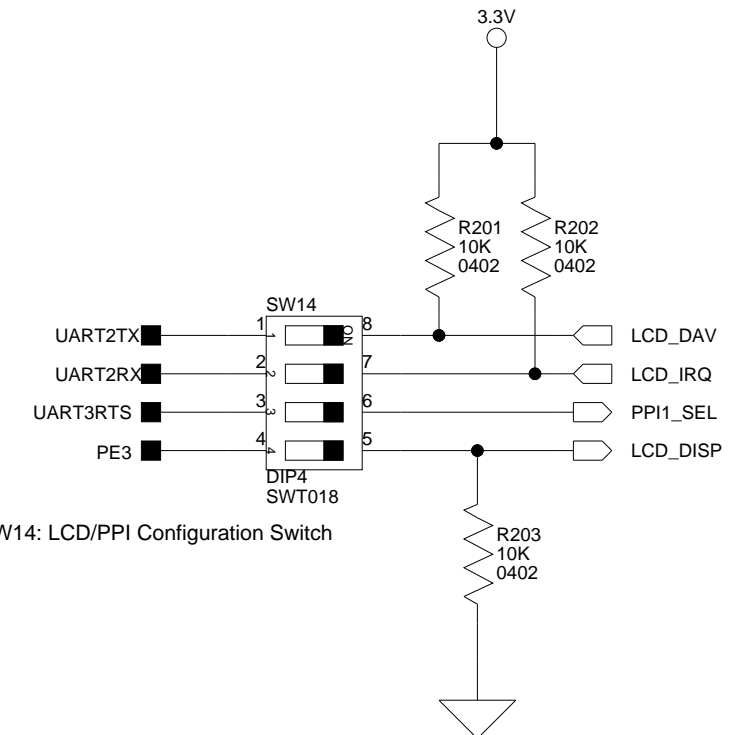


32 MB BURST FLASH
(16M x 16)



SW14: LCD/PPI Configuration Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW14.1	UART2TX (U2)	LCD_DAV (U9)	ON	J3.6 (Expansion Interface)
SW14.2	UART2RX (U2)	LCD_IRQ (U9)	ON	J3.5 (Expansion Interface)
SW14.3	UART3RTS (U2)	PPI1_SEL (U20)	ON	J3.32 (Expansion Interface)
SW14.4	PE3 (U2)	LCD_DISP (P15)	ON	J2.11 (Expansion Interface)

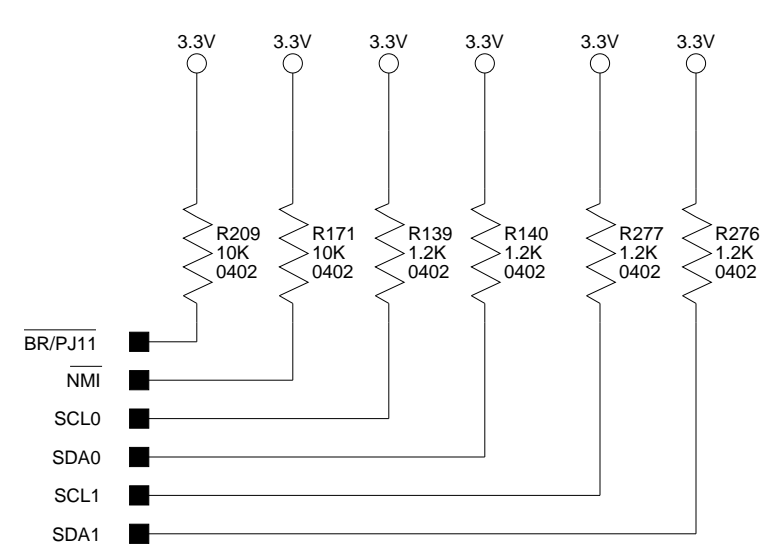
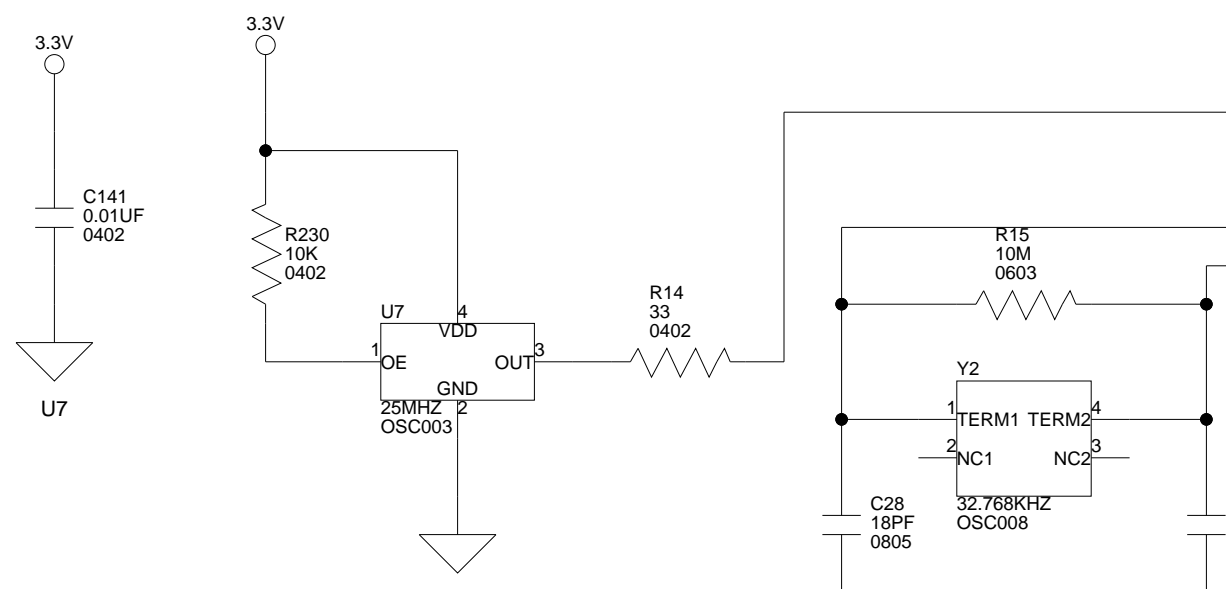


16 Mb SPI FLASH

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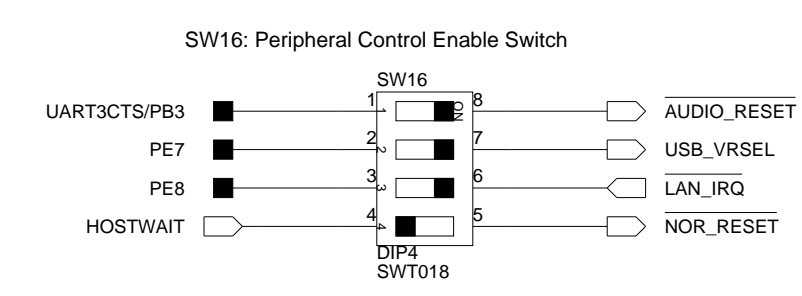
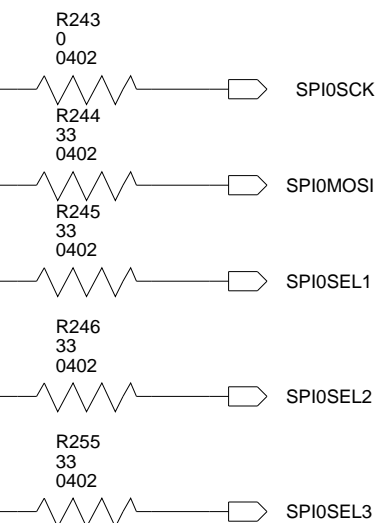
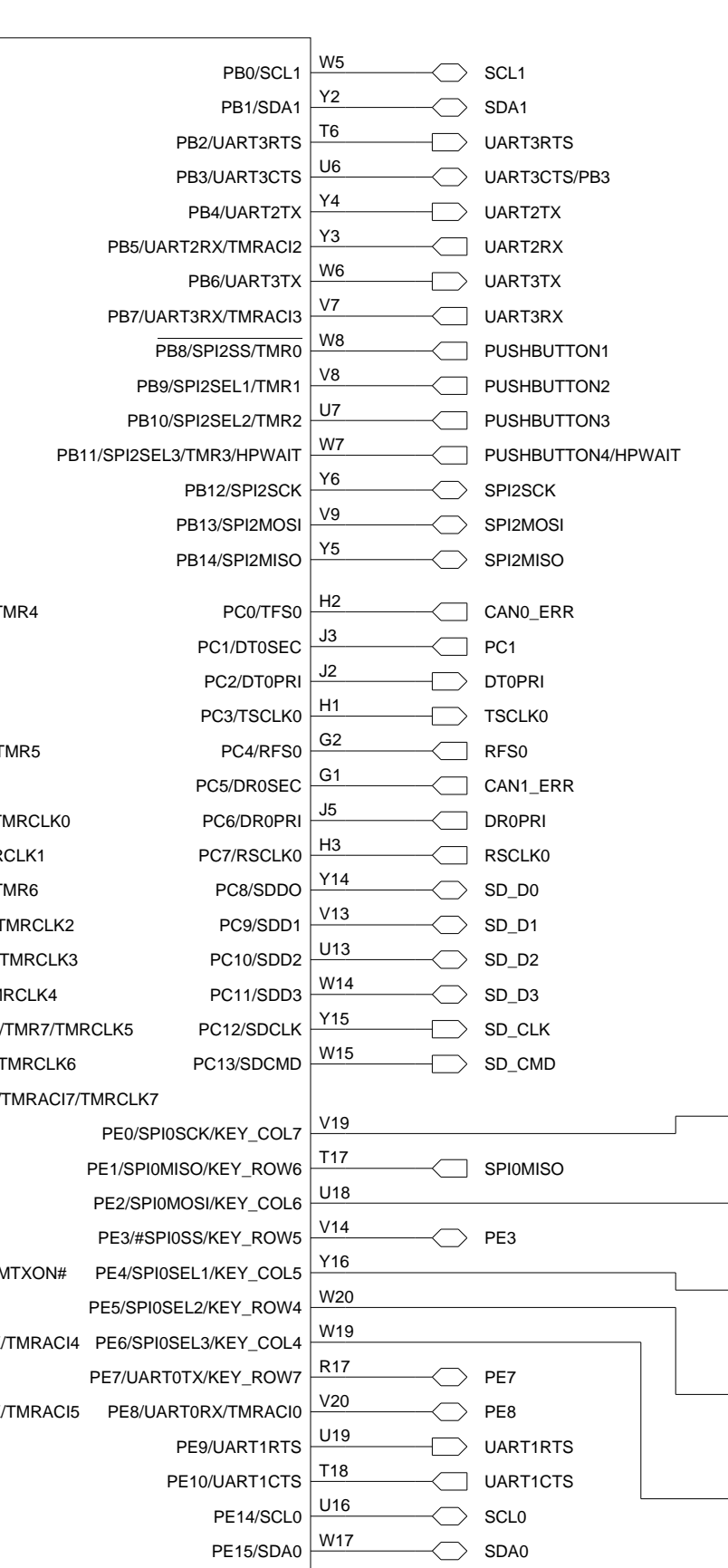
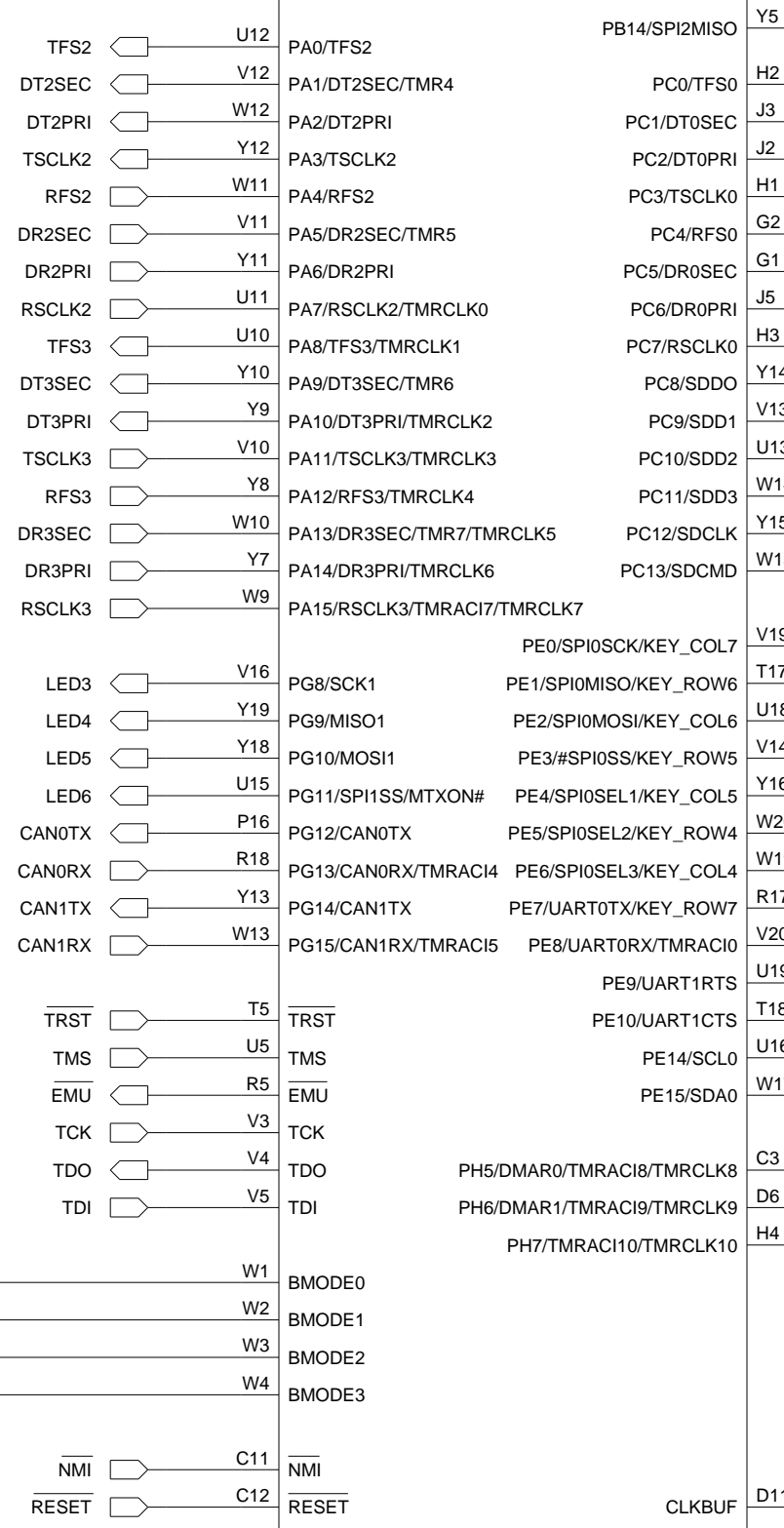
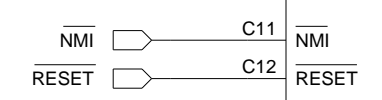
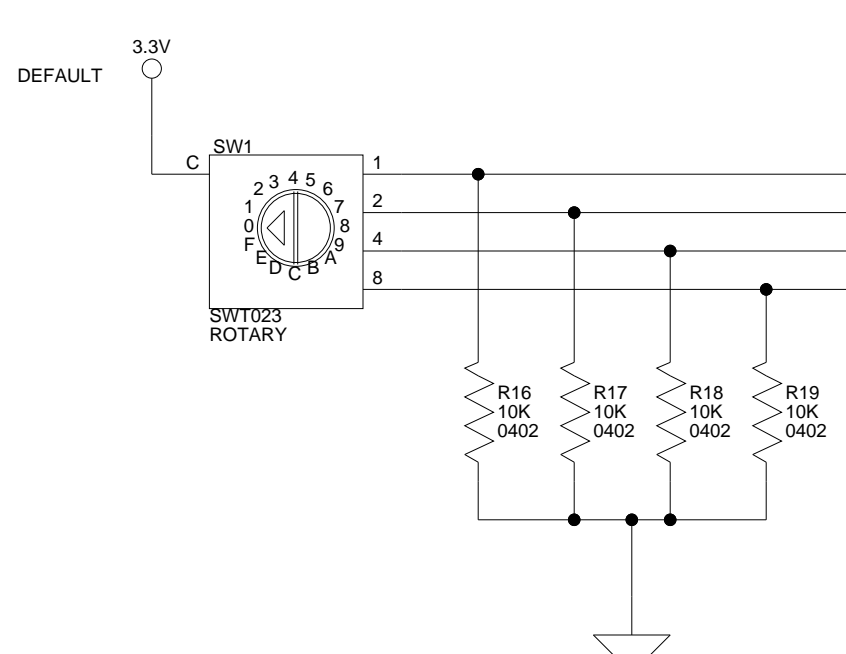
Title ADSP-BF548 EZ-KIT LITE EBIU

Size C	Board No. A0206-2006	Rev 1.4B
Date 12-4-2007_10:10	Sheet 3 of 17	



SW1: Boot Mode Select Switch

POSITION	BOOT MODE
0	Idle-no boot
1	Boot from 16-bit flash memory
2	Boot from 16-bit asynchronous FIFO
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART host
8	Reserved
9	Reserved
A	Boot from DDR SDRAM
B	Reserved
C	Reserved
D	Reserved
E	Boot from 16-bit Host DMA
F	Boot from 8-bit Host DMA



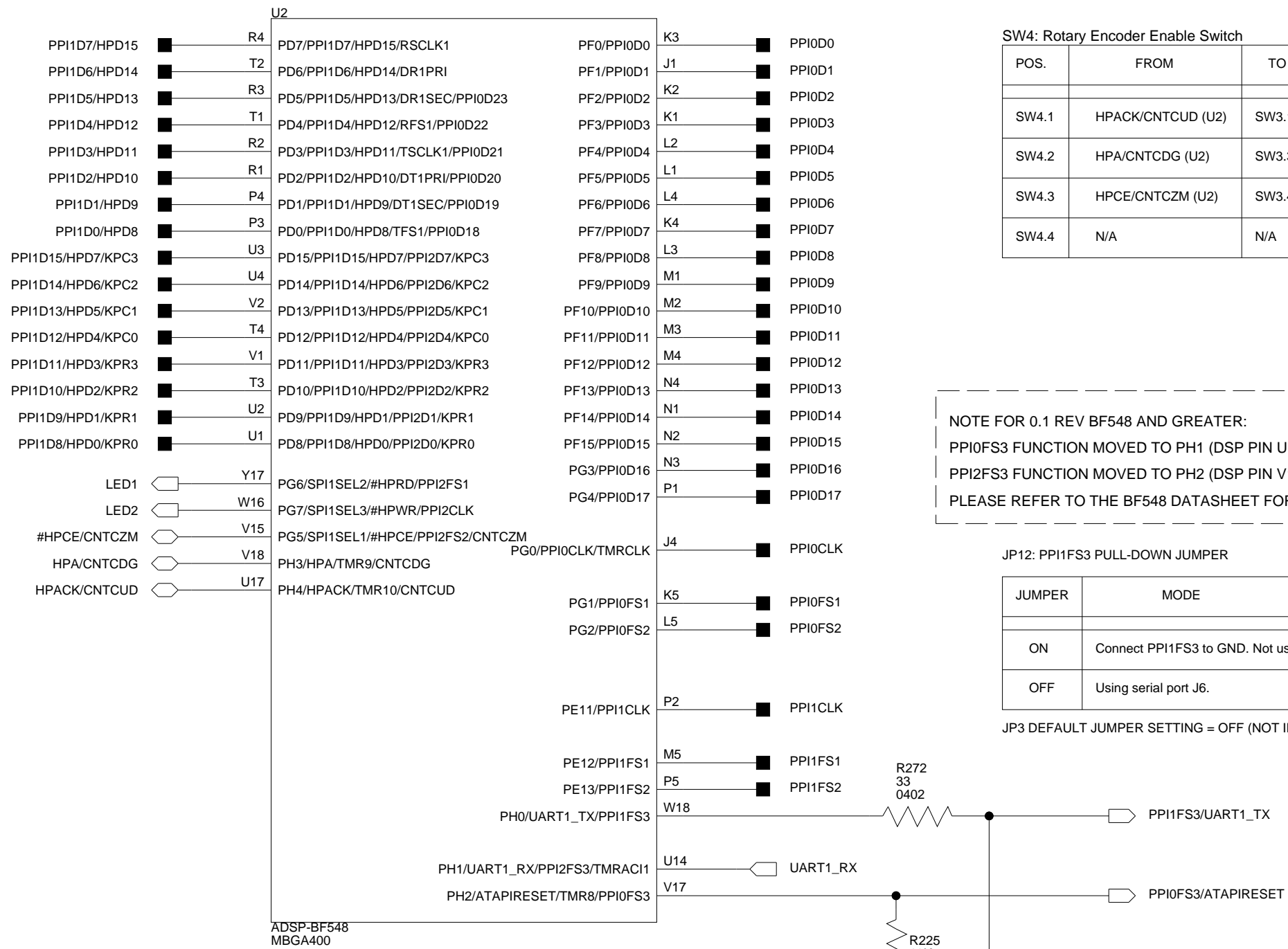
SW16: Peripheral Control Enable Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW16.1	UART3CTS/PB3 (U2)	AUDIO_RESET (U11)	ON	J3.33 (Expansion Interface)
SW16.2	PE7 (U2)	USB_VRSEL (U39, VR1)	ON	J3.37 (Expansion Interface)
SW16.3	PE8 (U2)	LAN_IRQ (U14)	ON	J3.38 (Expansion Interface)
SW16.4	HOSTWAIT (U2)	NOR_RESET (U25)	OFF	P3.12 (HOST Interface)

ANALOG DEVICES

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Title		ADSP-BF548 EZ-KIT LITE CONTROL	
Size C	Board No.	A0206-2006	
Date	2-15-2008_17:12	Sheet	4 of 17



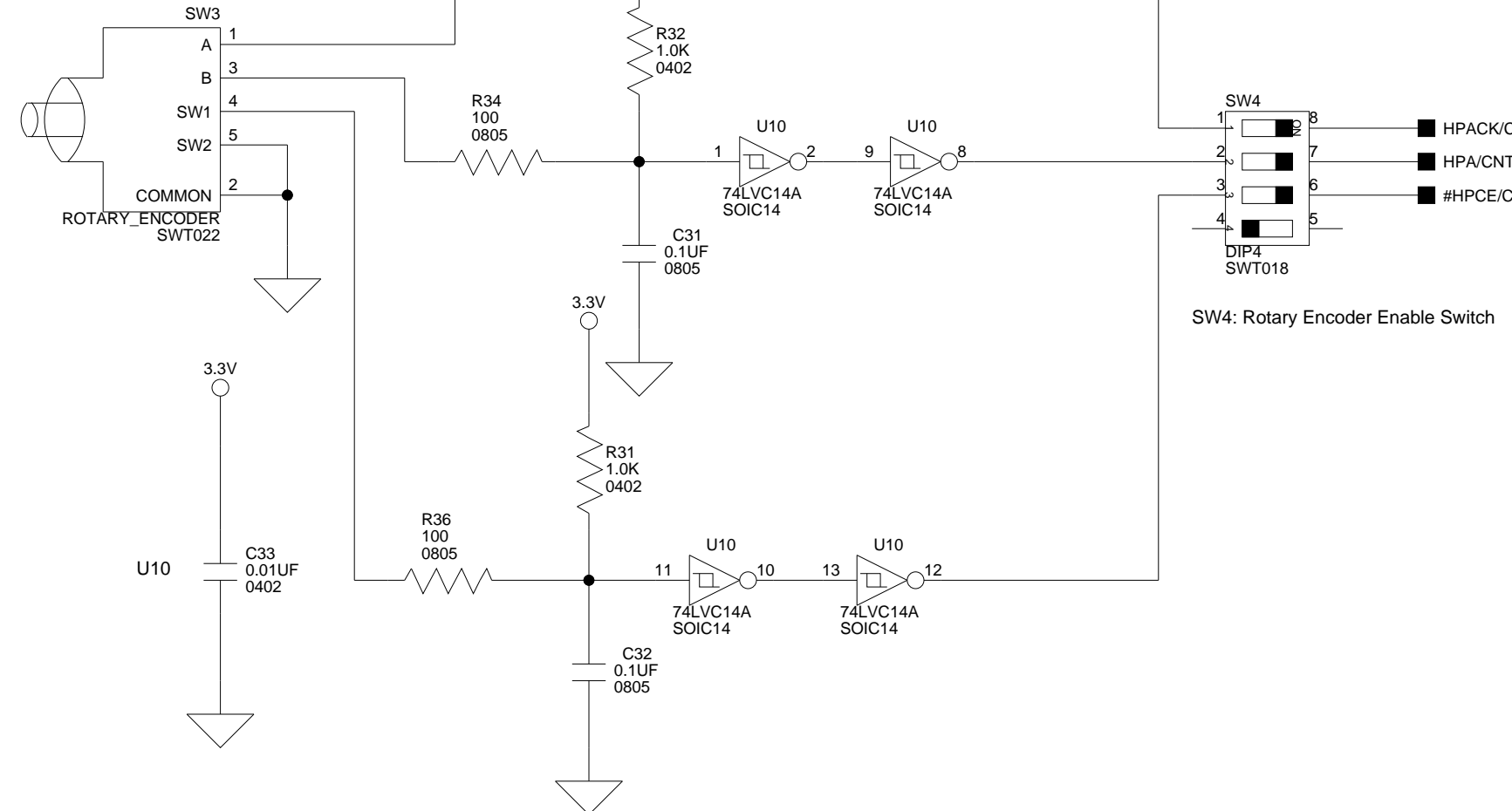
NOTE FOR 0.1 REV BF548 AND GREATER:
 PPI0FS3 FUNCTION MOVED TO PH1 (DSP PIN U14)
 PPI2FS3 FUNCTION MOVED TO PH2 (DSP PIN V17)
 PLEASE REFER TO THE BF548 DATASHEET FOR MORE DETAILS

JUMPER	MODE
ON	Connect PPI1FS3 to GND. Not using serial port J6
OFF	Using serial port J6.

JP3 DEFAULT JUMPER SETTING = OFF (NOT INSTALLED)

NOTE: DEFAULT JUMPER SETTING = DNP

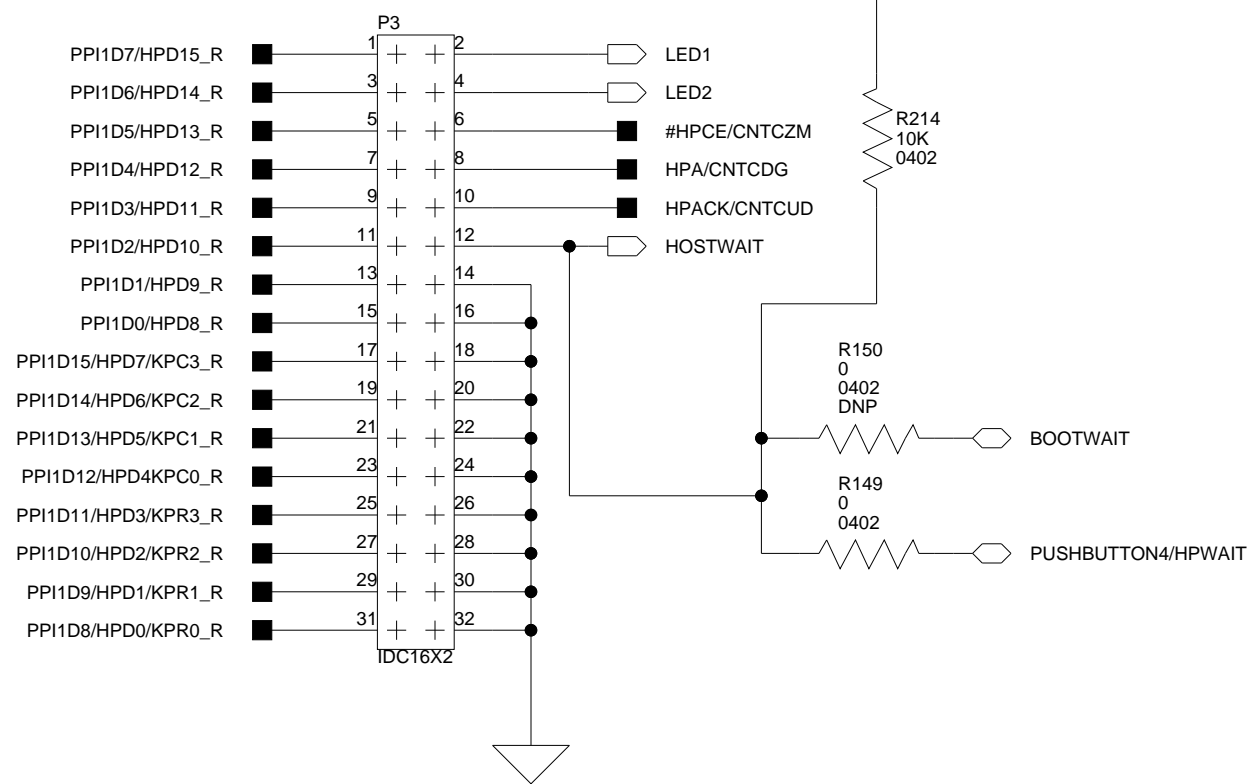
ROTARY ENCODER



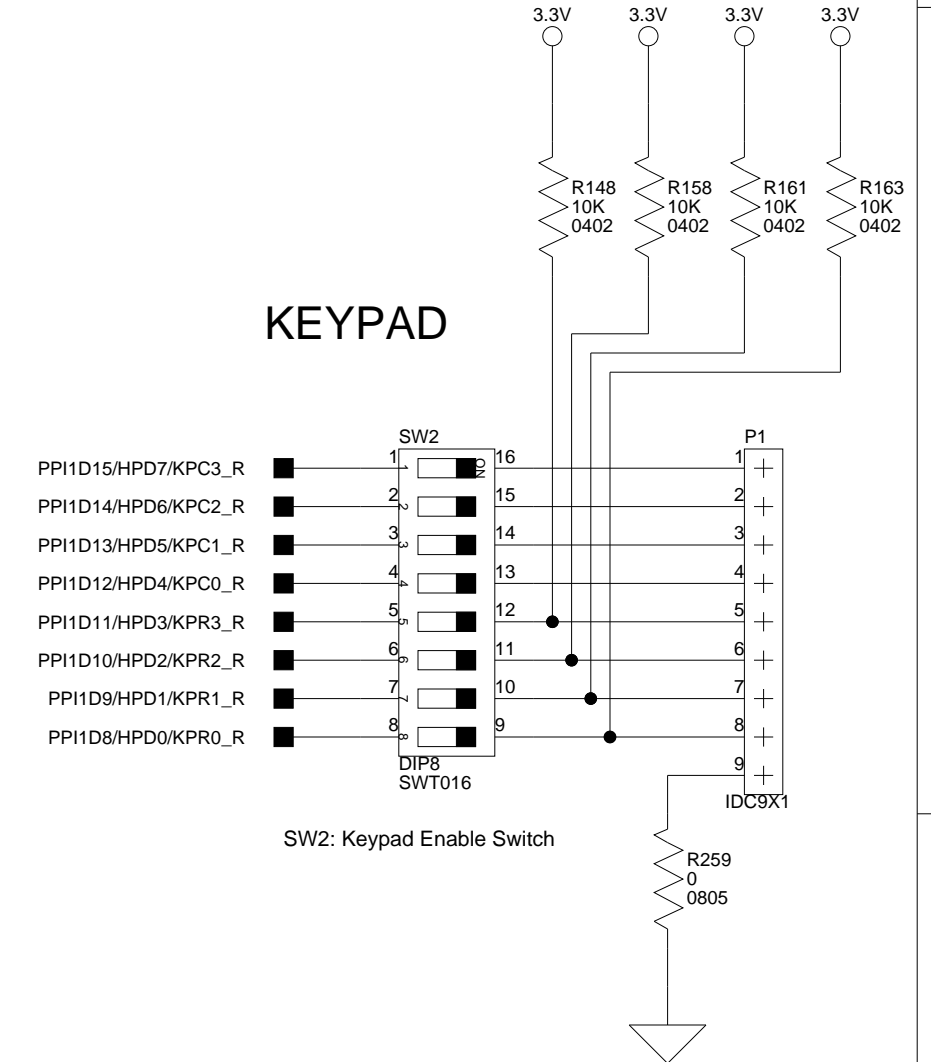
SW2: Keypad Enable Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW2.1	DSP (U2)	P1.1	ON	Expansion Interface, HOST Interface, PPI1
SW2.2	DSP (U2)	P1.2	ON	Expansion Interface, HOST Interface, PPI1
SW2.3	DSP (U2)	P1.3	ON	Expansion Interface, HOST Interface, PPI1
SW2.4	DSP (U2)	P1.4	ON	Expansion Interface, HOST Interface, PPI1
SW2.5	DSP (U2)	P1.5	ON	Expansion Interface, HOST Interface, PPI1
SW2.6	DSP (U2)	P1.6	ON	Expansion Interface, HOST Interface, PPI1
SW2.7	DSP (U2)	P1.7	ON	Expansion Interface, HOST Interface, PPI1
SW2.8	DSP (U2)	P1.8	ON	Expansion Interface, HOST Interface, PPI1

HOST PORT

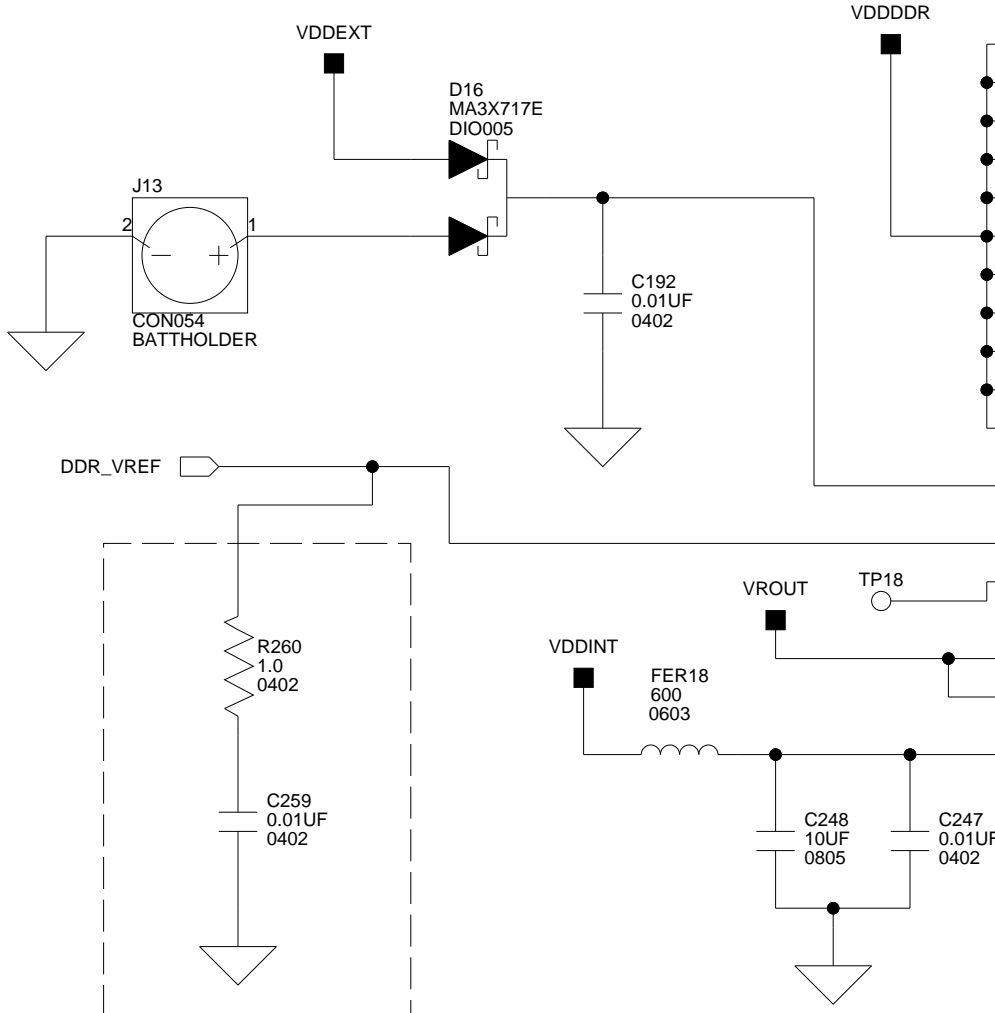
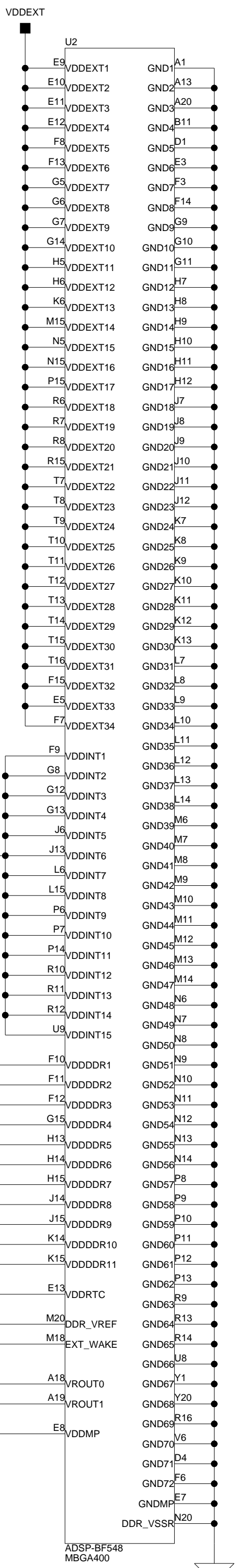


KEYPAD



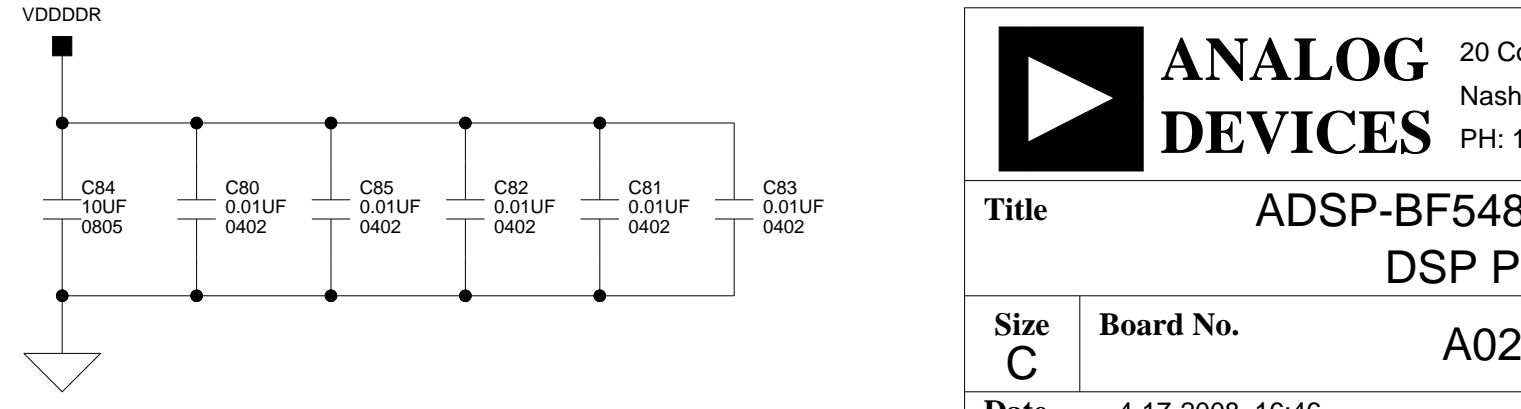
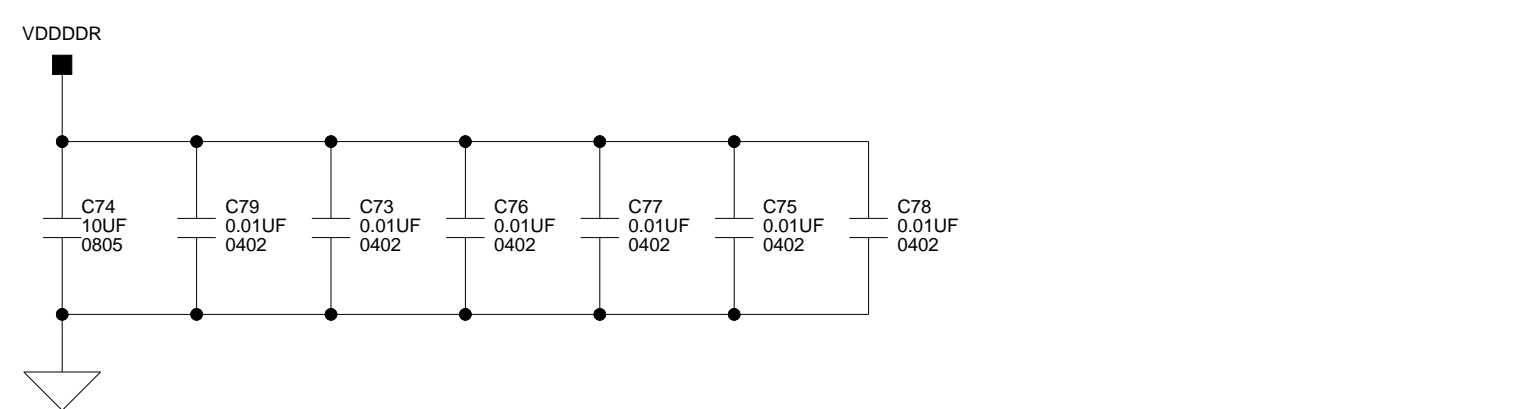
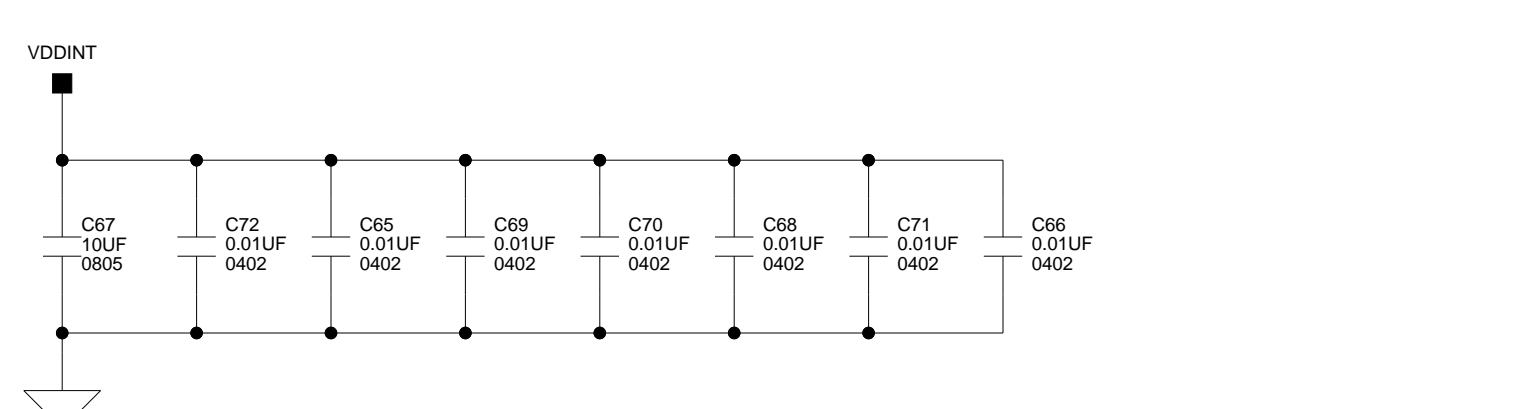
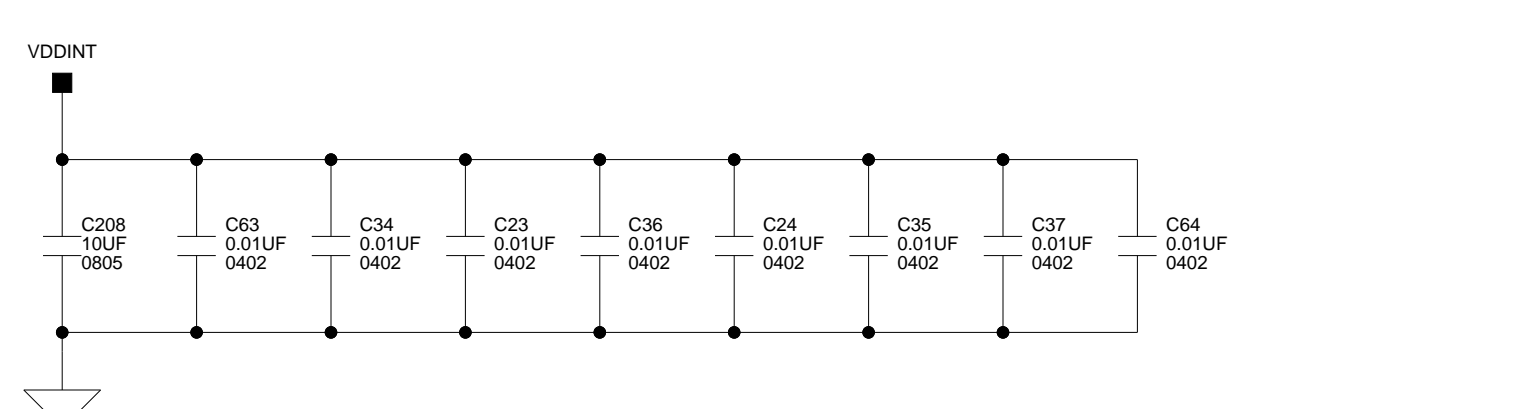
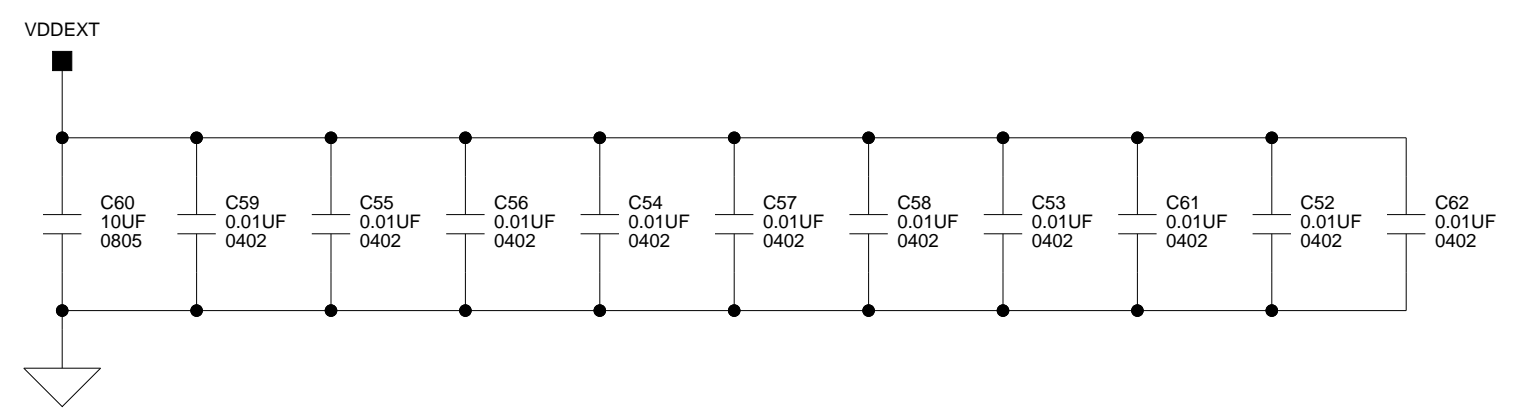
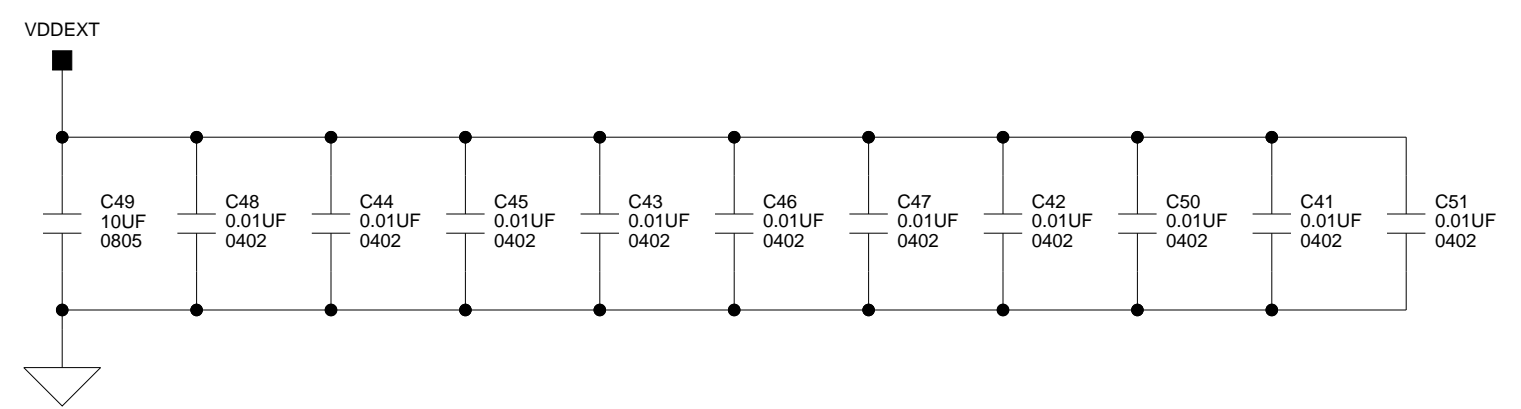
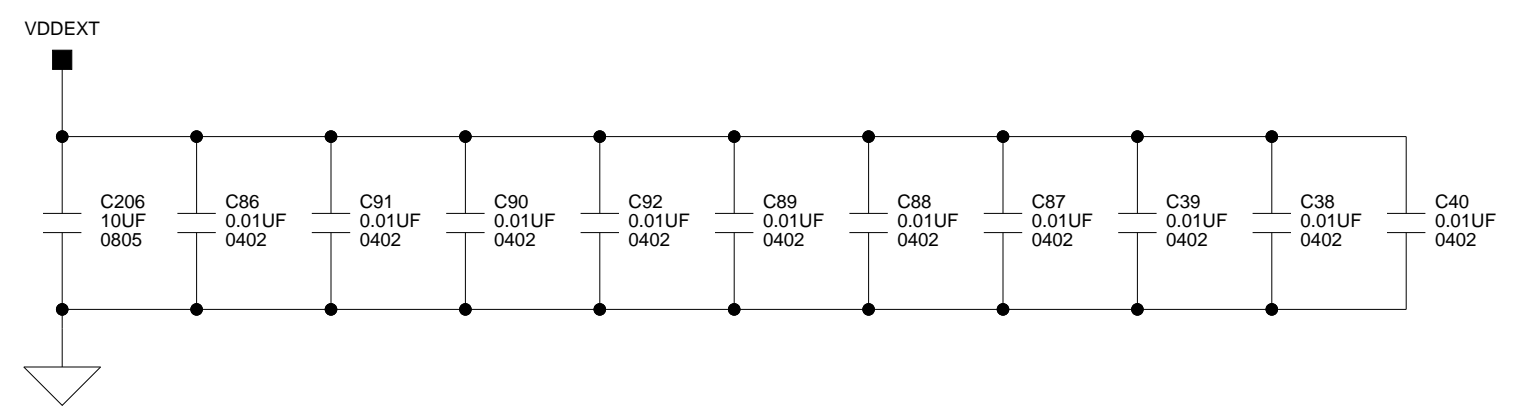
20 Cotton Road
 Nashua, NH 03063
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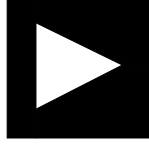
Title		ADSP-BF548 EZ-KIT LITE	
PPI, KEYPAD, THUMBWHEEL INTERFACE			
Size C	Board No.	A0206-2006	Rev
Date	1-8-2008_16:23	Sheet	5 of 17

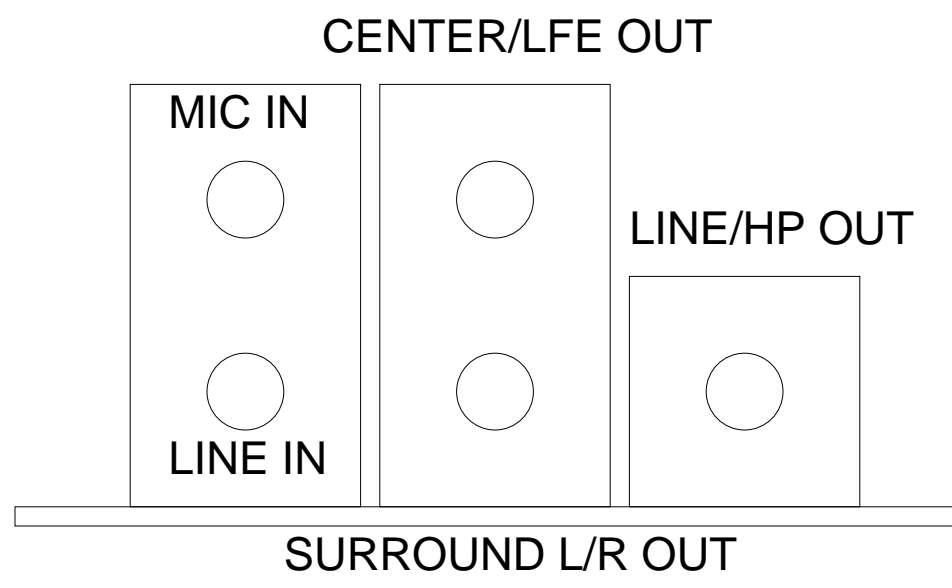


PLACE AS CLOSE TO U2.M20 AS POSSIBLE

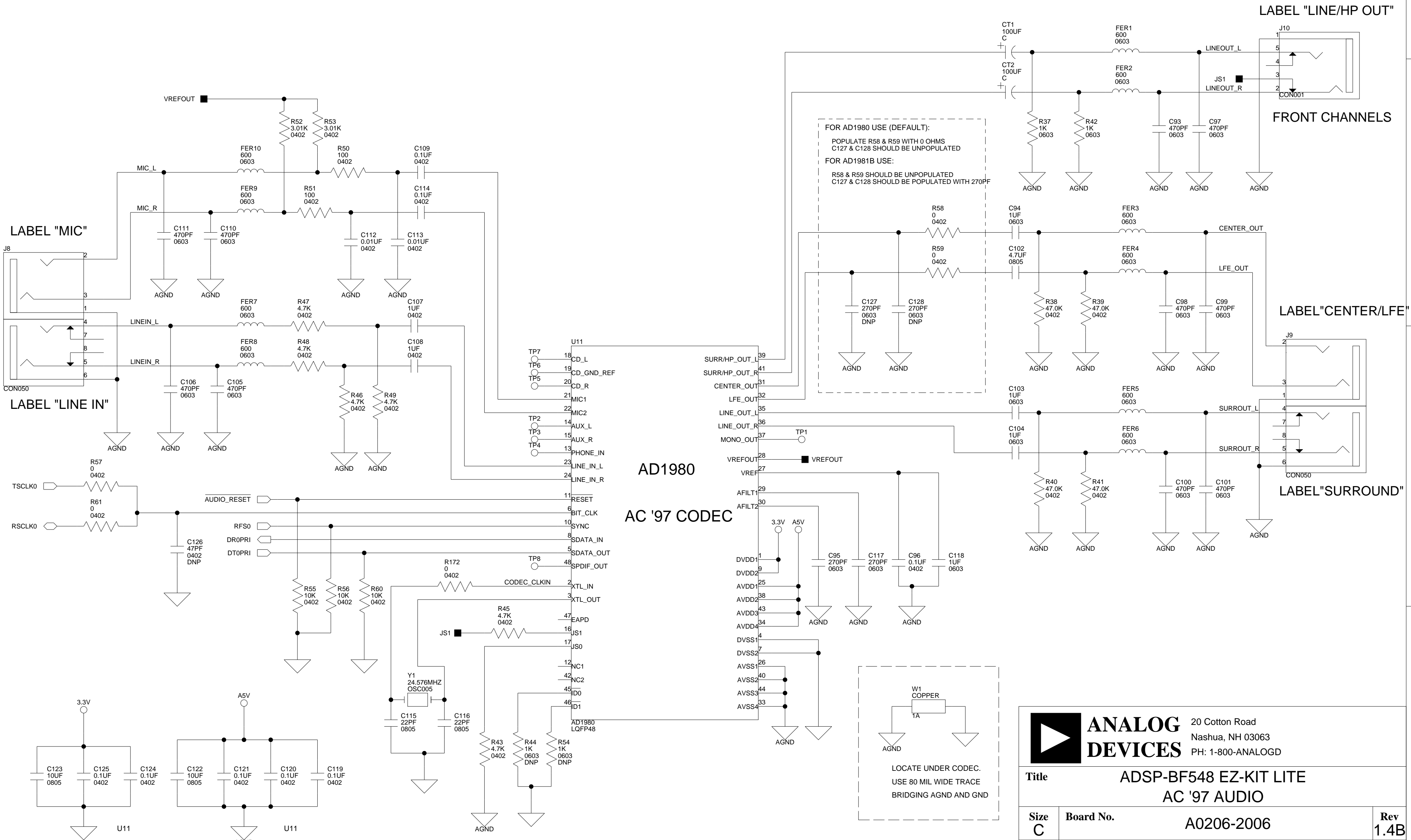
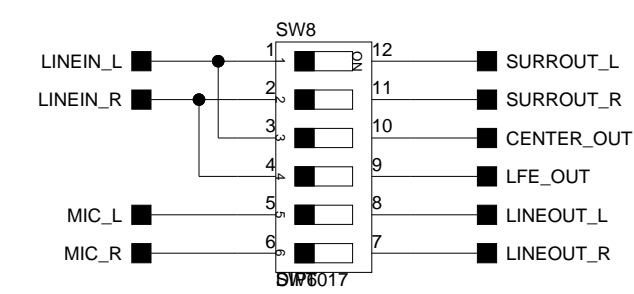
VDDMP ON BF548 DESIGNS CAN BE CONNECTED DIRECTLY TO VDDINT



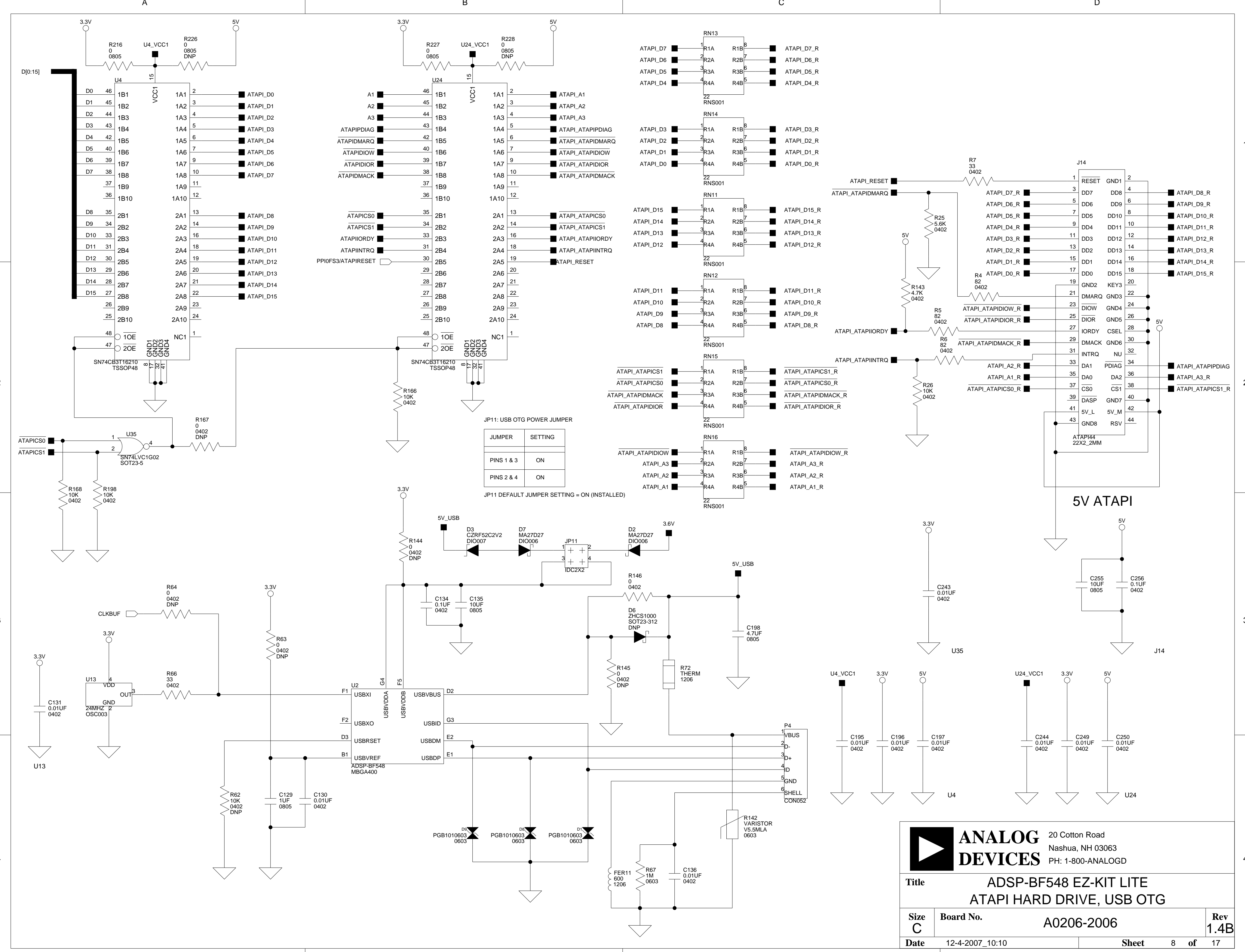
 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF548 EZ-KIT LITE DSP POWER	
Size C	Board No. A0206-2006	Rev 1.4B	
Date 4-17-2008_16:46	Sheet 6 of 17		

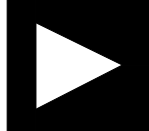


Audio Loopback Test Switch
(Default = ALL OFF)
For Test Purposes Only



		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF548 EZ-KIT LITE AC '97 AUDIO	
Size C	Board No.	A0206-2006	
Date	12-4-2007_10:10	Sheet	7 of 17
		Rev 1.4B	

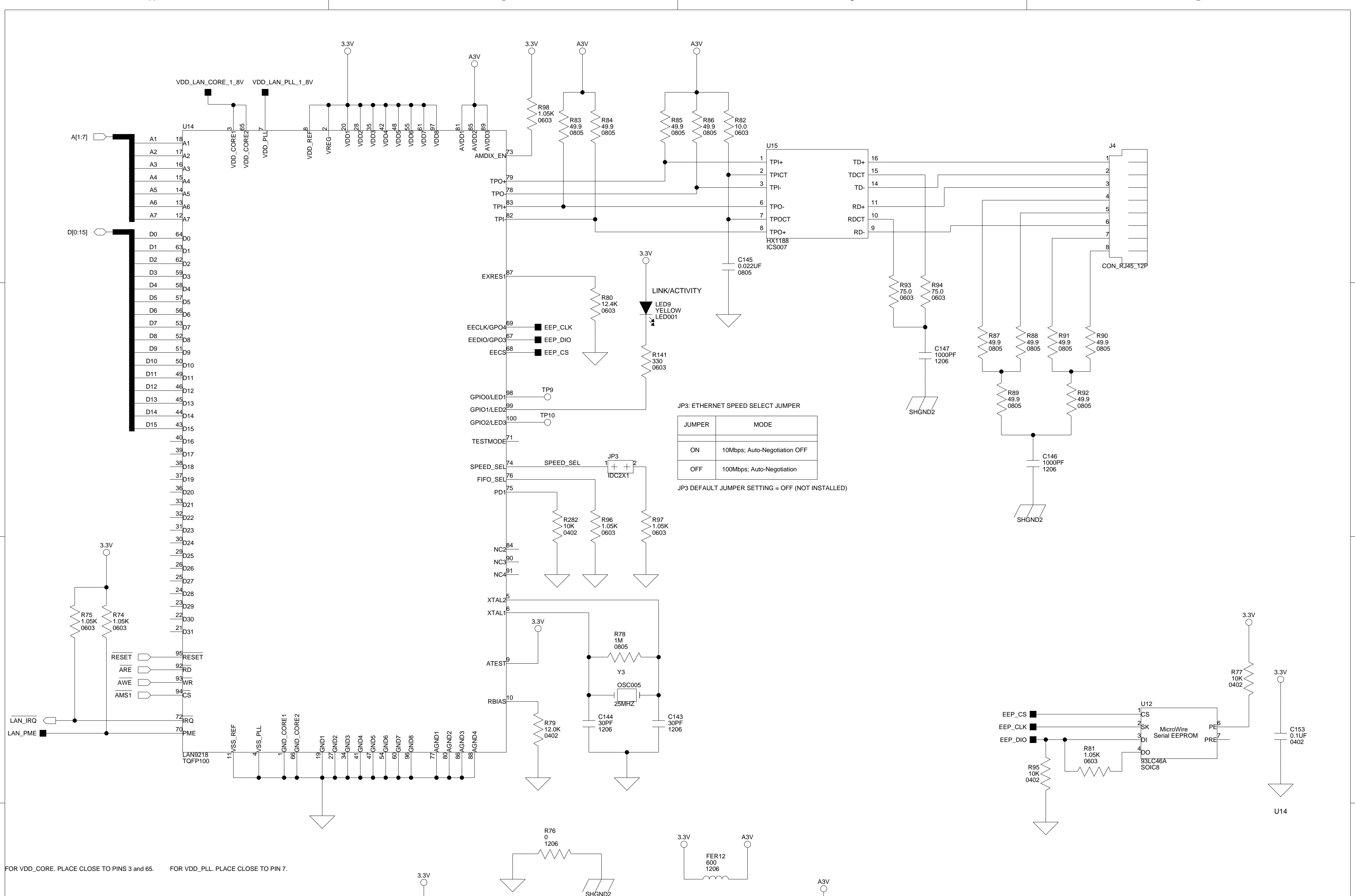




ANALOG DEVICES

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Title		
ADSP-BF548 EZ-KIT LITE ATAPI HARD DRIVE, USB OTG		
Size C	Board No.	Rev
	A0206-2006	1.4B
Date	12-4-2007_10:10	Sheet 8 of 17

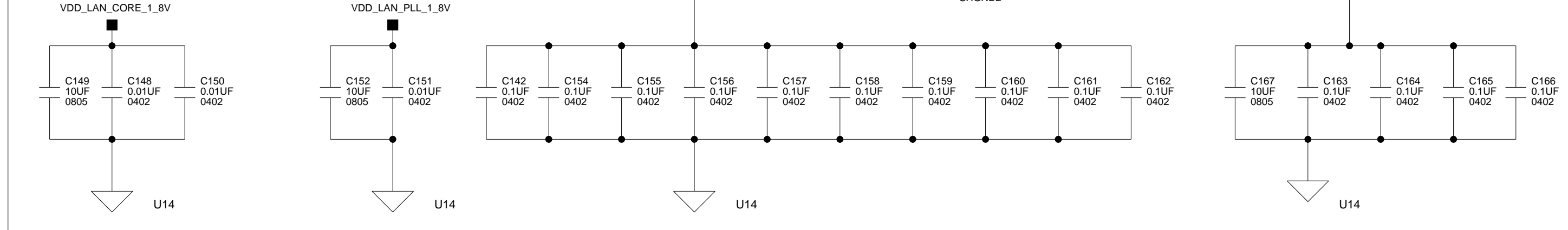


JP3: ETHERNET SPEED SELECT JUMPER

JUMPER	MODE
ON	10Mbps; Auto-Negotiation OFF
OFF	100Mbps; Auto-Negotiation

JP3 DEFAULT JUMPER SETTING = OFF (NOT INSTALLED)

FOR VDD_CORE. PLACE CLOSE TO PINS 3 and 65. FOR VDD_PLL. PLACE CLOSE TO PIN 7.

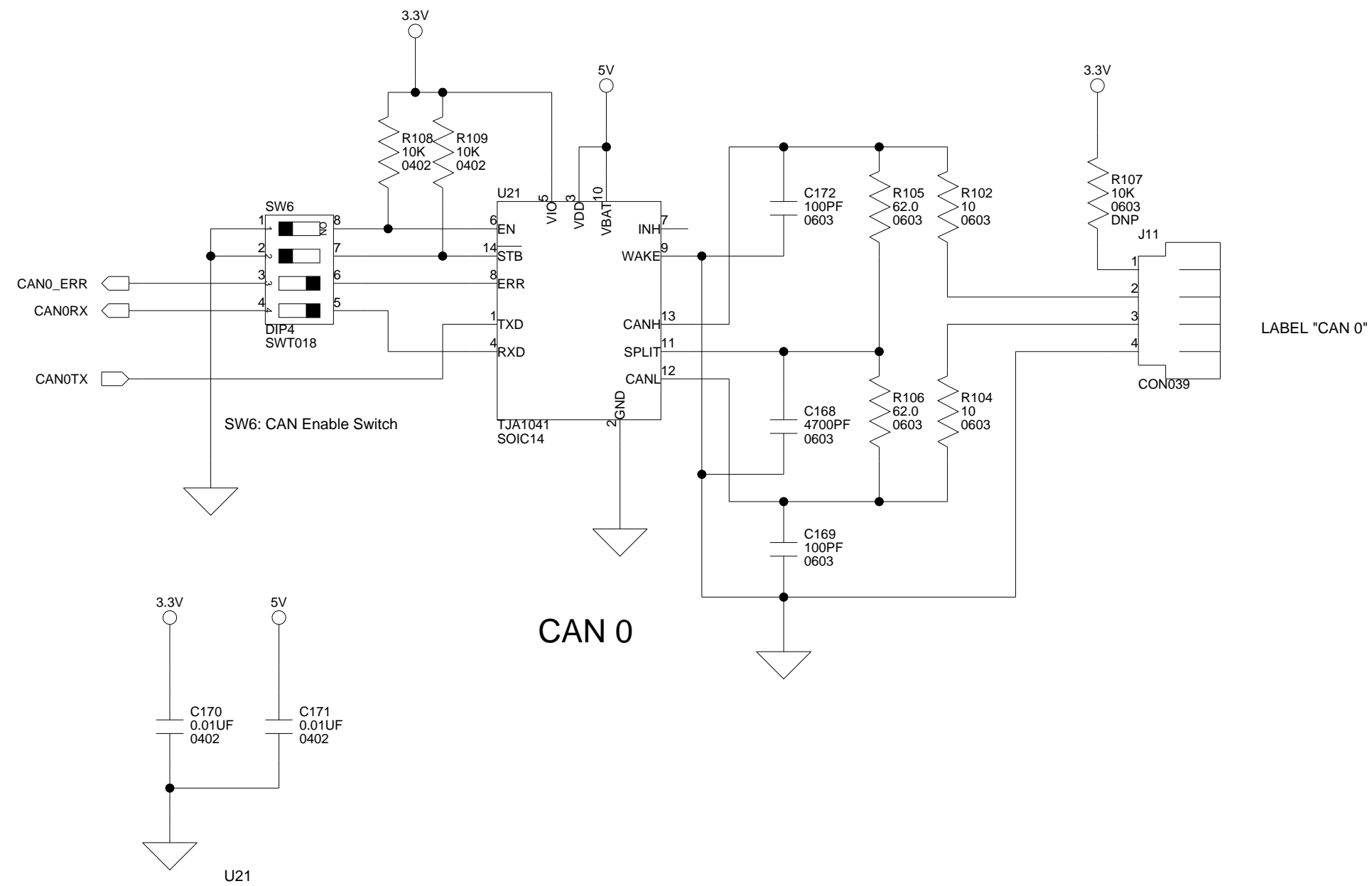


ANALOG DEVICES

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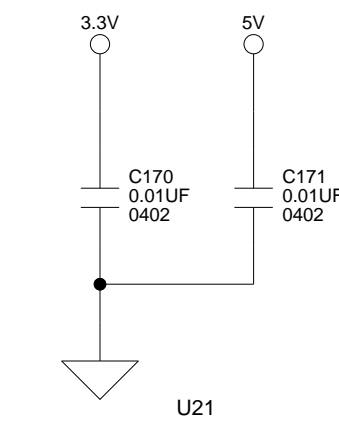
Title ADSP-BF548 EZ-KIT LITE ETHERNET

Size C	Board No. A0206-2006	Rev 1.4B
Date 12-4-2007_10:10	Sheet 9 of 17	

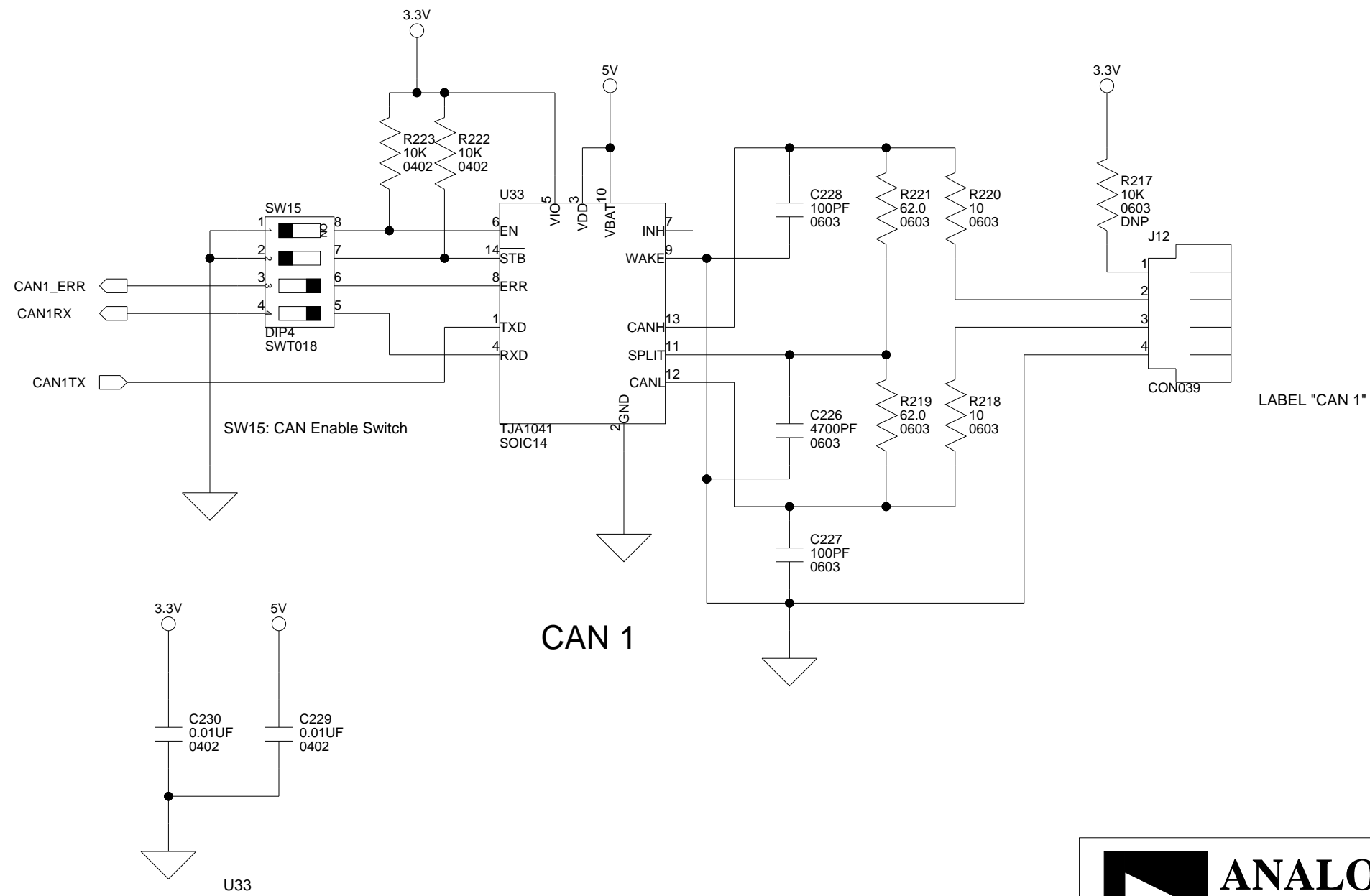


SW6: CAN0 Enable Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION
SW6.1	ENABLE	GND	OFF	
SW6.2	-STB	GND	OFF	
SW6.3	CAN0_ERR	U2 - PC0	ON	STAMP_GPIO1
SW6.4	CAN0RX	U2 - PG13	ON	STAMP_GPIO0

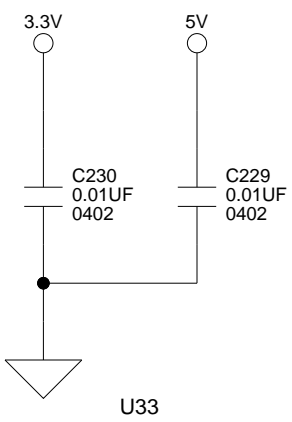


CAN 0

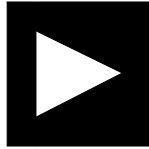


SW15: CAN1 Enable Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION
SW15.1	ENABLE	GND	OFF	
SW15.2	-STB	GND	OFF	
SW15.3	CAN1_ERR	U2 - PC5	ON	STAMP_GPIO3
SW15.4	CAN1RX	U2 - PG15	ON	STAMP_GPIO2

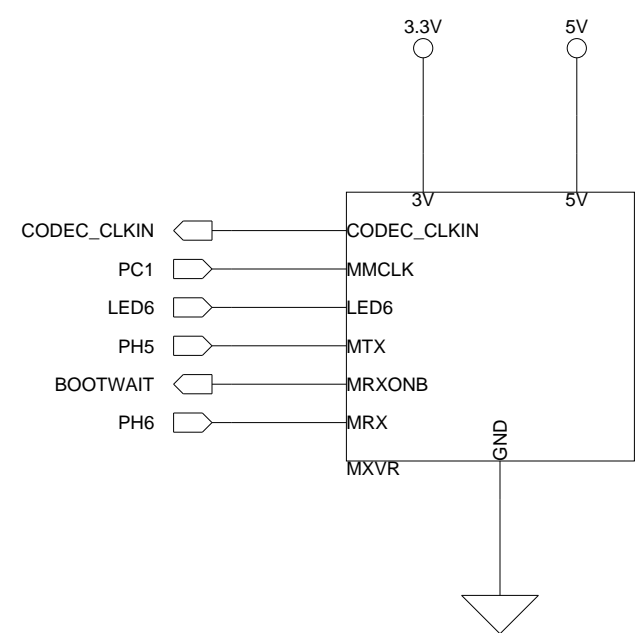
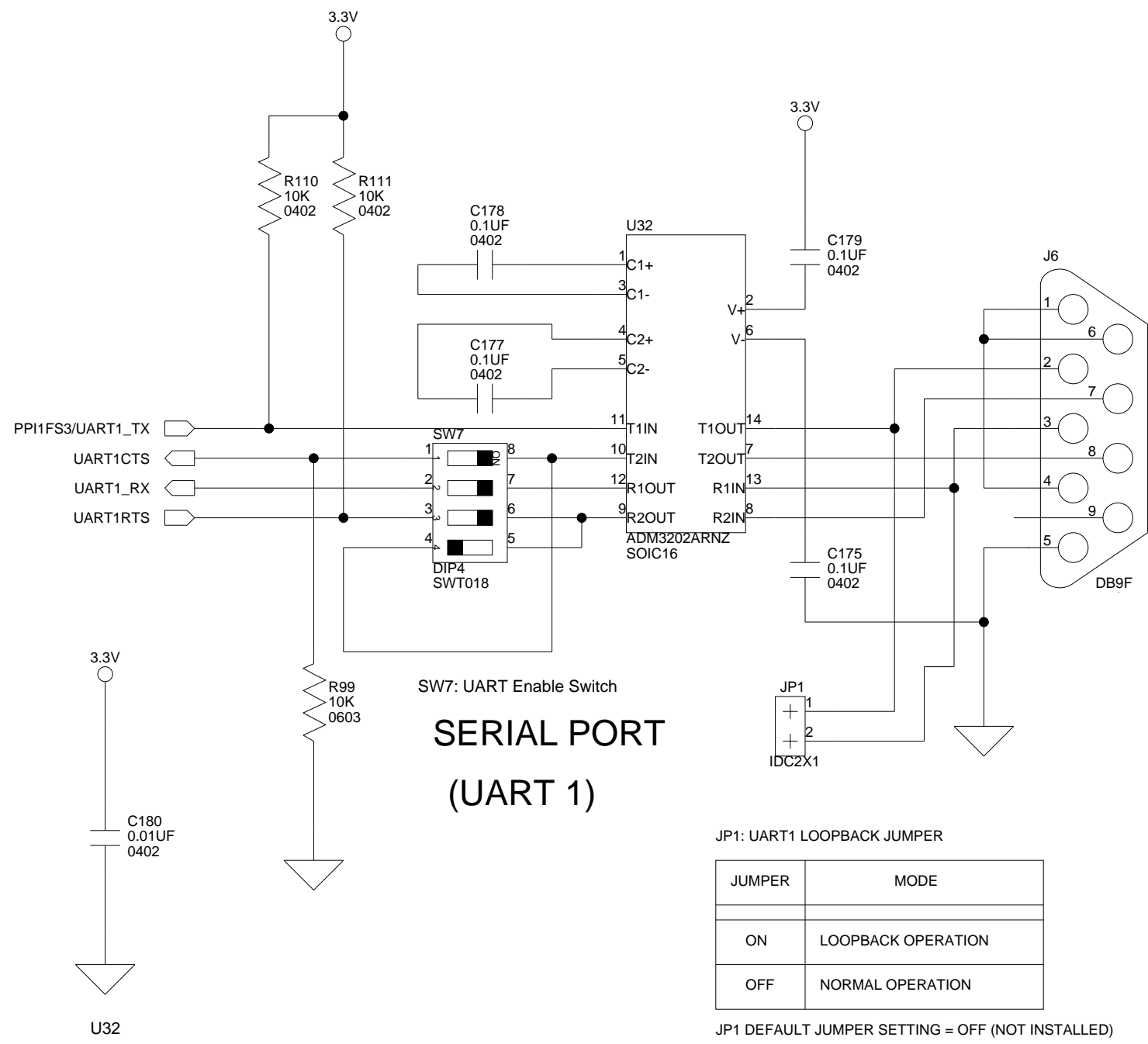


CAN 1

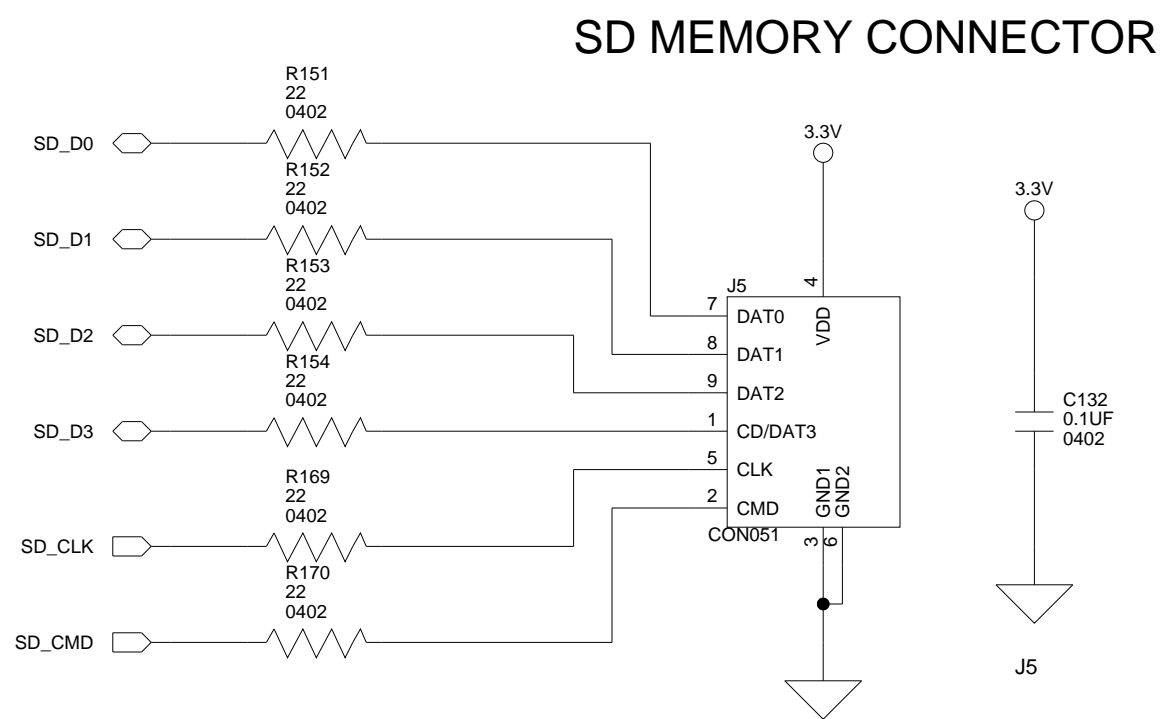
 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF548 EZ-KIT LITE CAN	
Size C	Board No. A0206-2006	Rev 1.4B	
Date 12-4-2007_10:10	Sheet 10 of 17		

SW7: UART Enable Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW7.1	UART1CTS (U2)	U32	ON	N/A
SW7.2	UART1_RX (U2)	U32	ON	J3.47 (Expansion Interface)
SW7.3	UART1RTS (U2)	U32	ON	N/A
SW7.4	UART1RTS	UART1CTS	OFF	LOOPBACK OF CTS TO RTS



THE MXVR PORT IS ONLY AVAILABLE ON THE BF549
SOME OF THESE PINS STILL NEED TO BE CONNECTED ON THE BF548
PLEASE REFER TO BF548 DATASHEETS FOR MOST ACCURATE INFO



ANALOG DEVICES

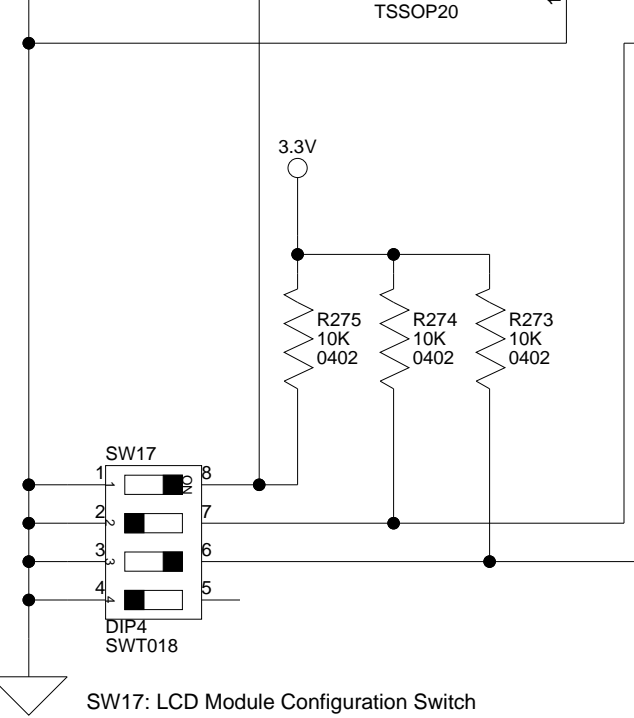
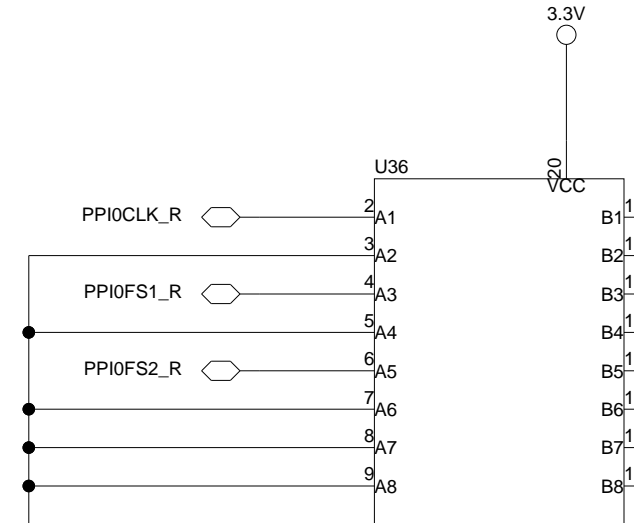
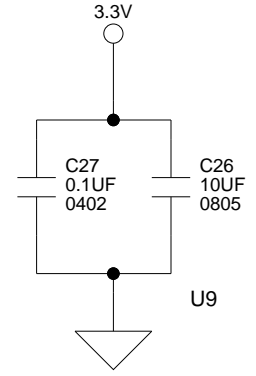
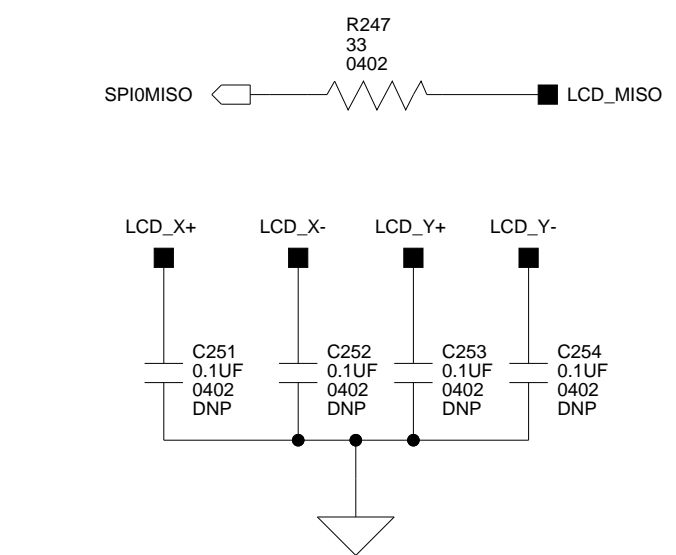
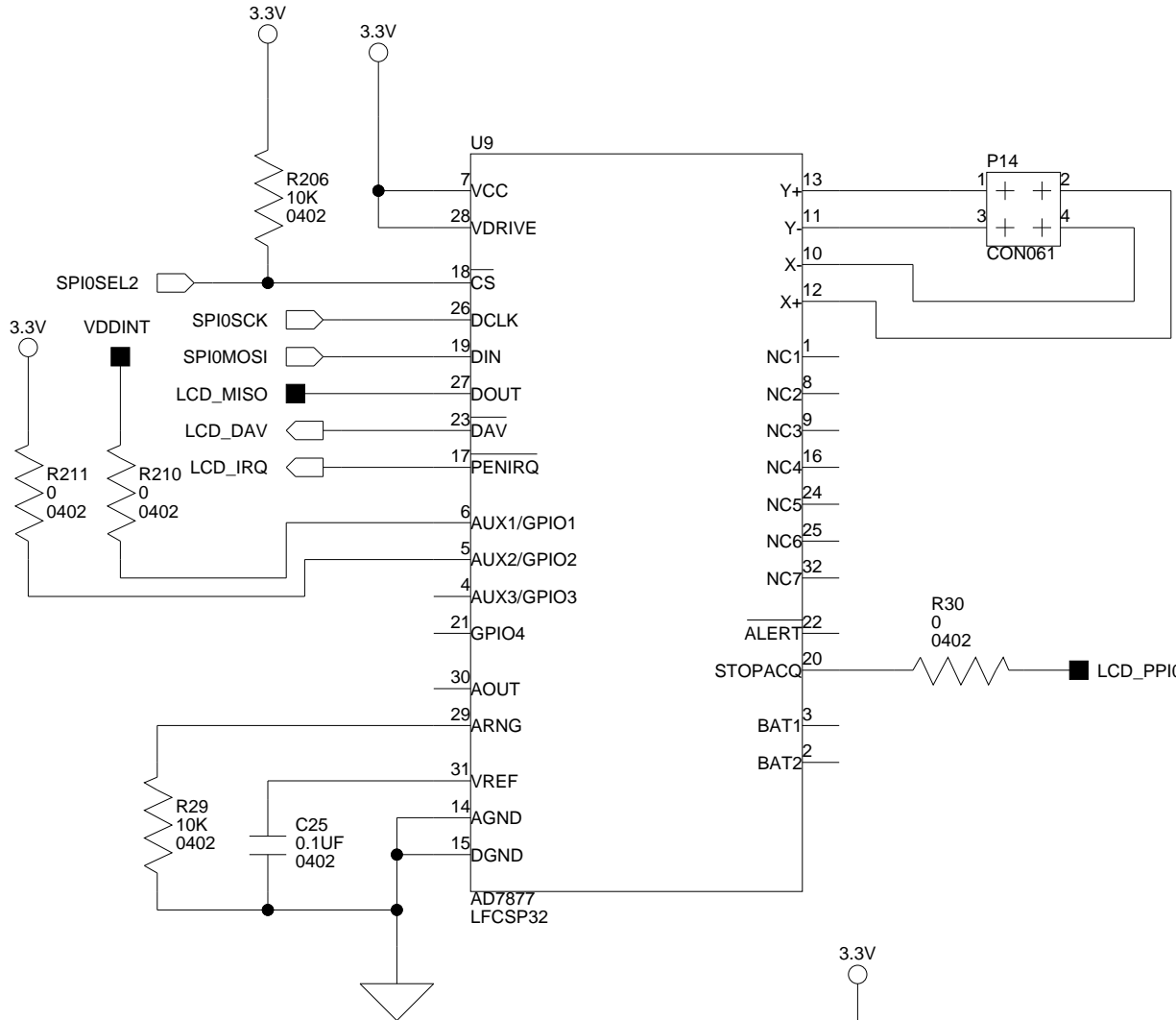
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Nashua, NH 03063
PH: 1-800-ANALOGD

Title ADSP-BF548 EZ-KIT LITE MXVR PORT, UART, SD CONN		
Size C	Board No. A0206-2006	Rev 1.4B
Date 4-17-2008_17:04	Sheet 11 of 17	

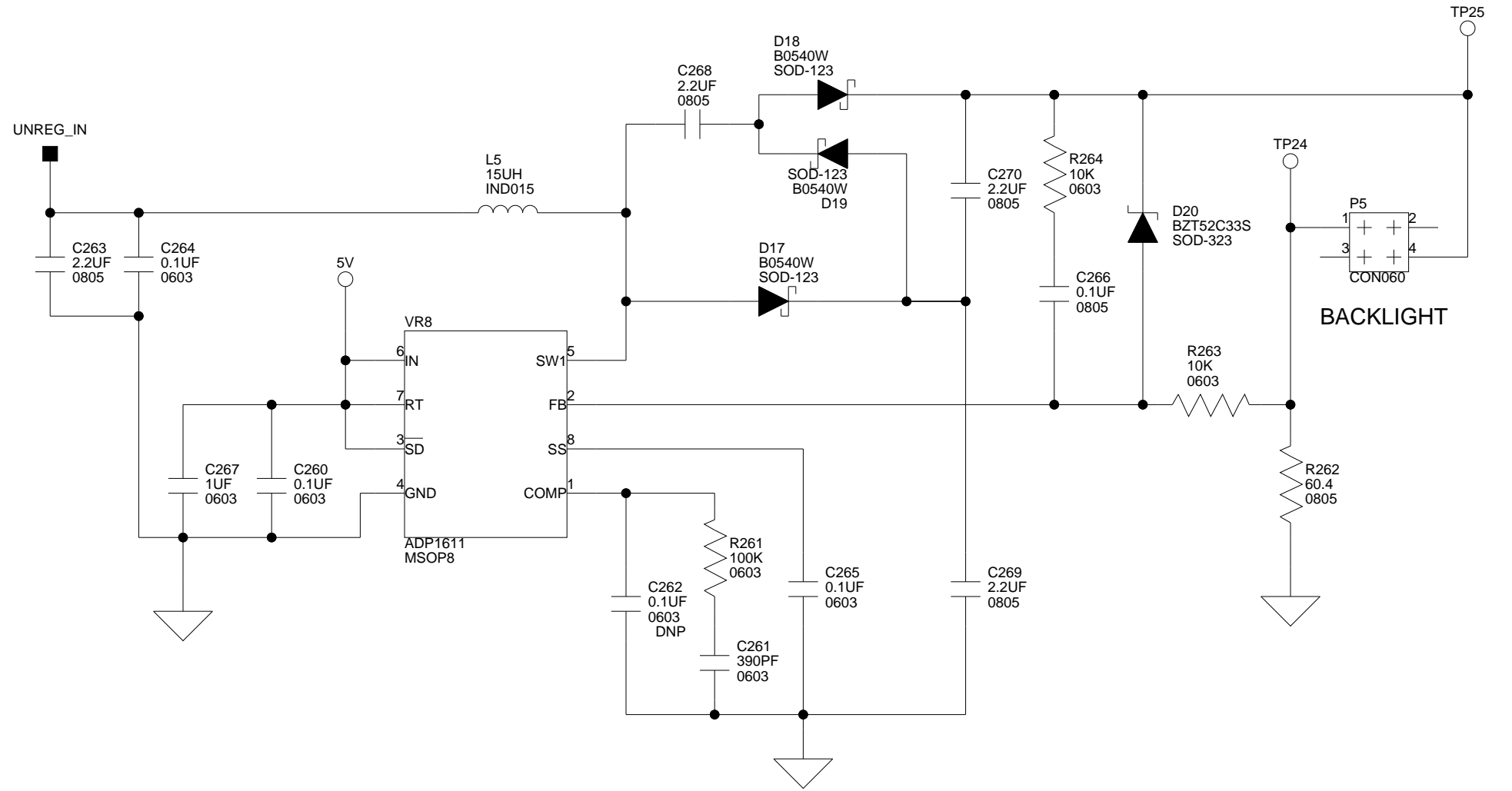
SW17: LCD Module Configuration Switch

SW17.1	SW17.2	SW17.3	SW17.4	MODE	ALTERNATE FUNCTION
OFF	OFF	OFF	N/A	LCD DISABLED	PPI0, PPI1, & HOST SIGNALS CAN BE USED ON EXPANSION INTERFACE, PPI1, HOST INERFACE
ON	ON	OFF	N/A	LCD IN 18-BIT MODE	PPI1, & HOST SIGNALS CAN BE USED ON EXPANSION INTERFACE, PPI1, HOST INERFACE
ON	OFF	ON	N/A	* LCD IN 24-BIT MODE	PPI0, PPI1, & HOST SIGNALS ALL USED FOR LCD

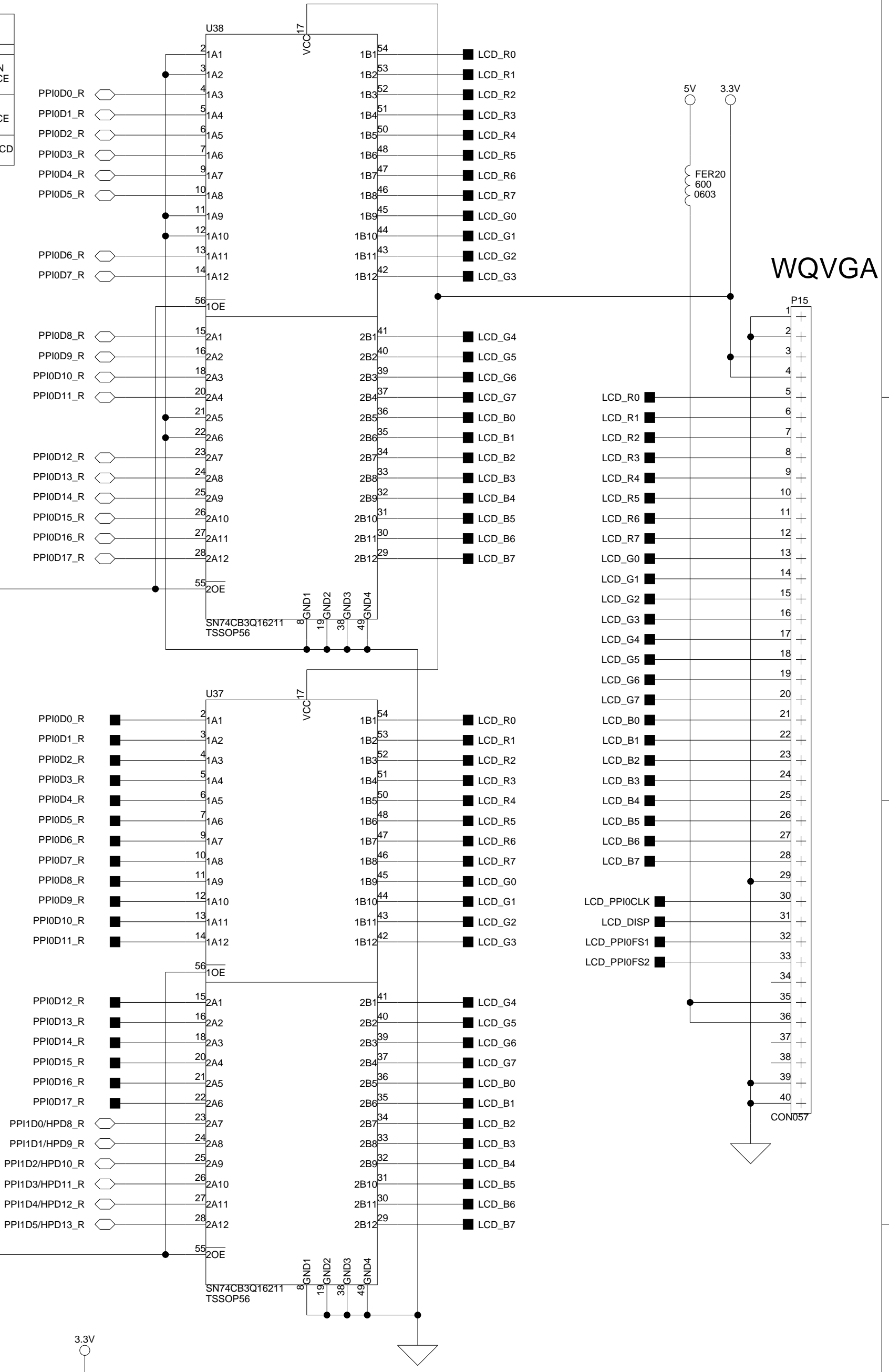
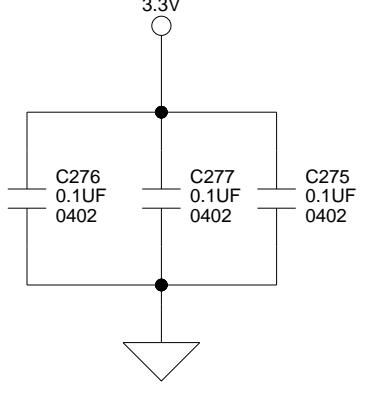
* DENOTES DEFAULT CONFIGURATION



SW17: LCD Module Configuration Switch



BACKLIGHT



WQVGA

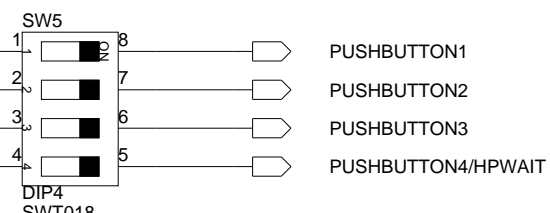
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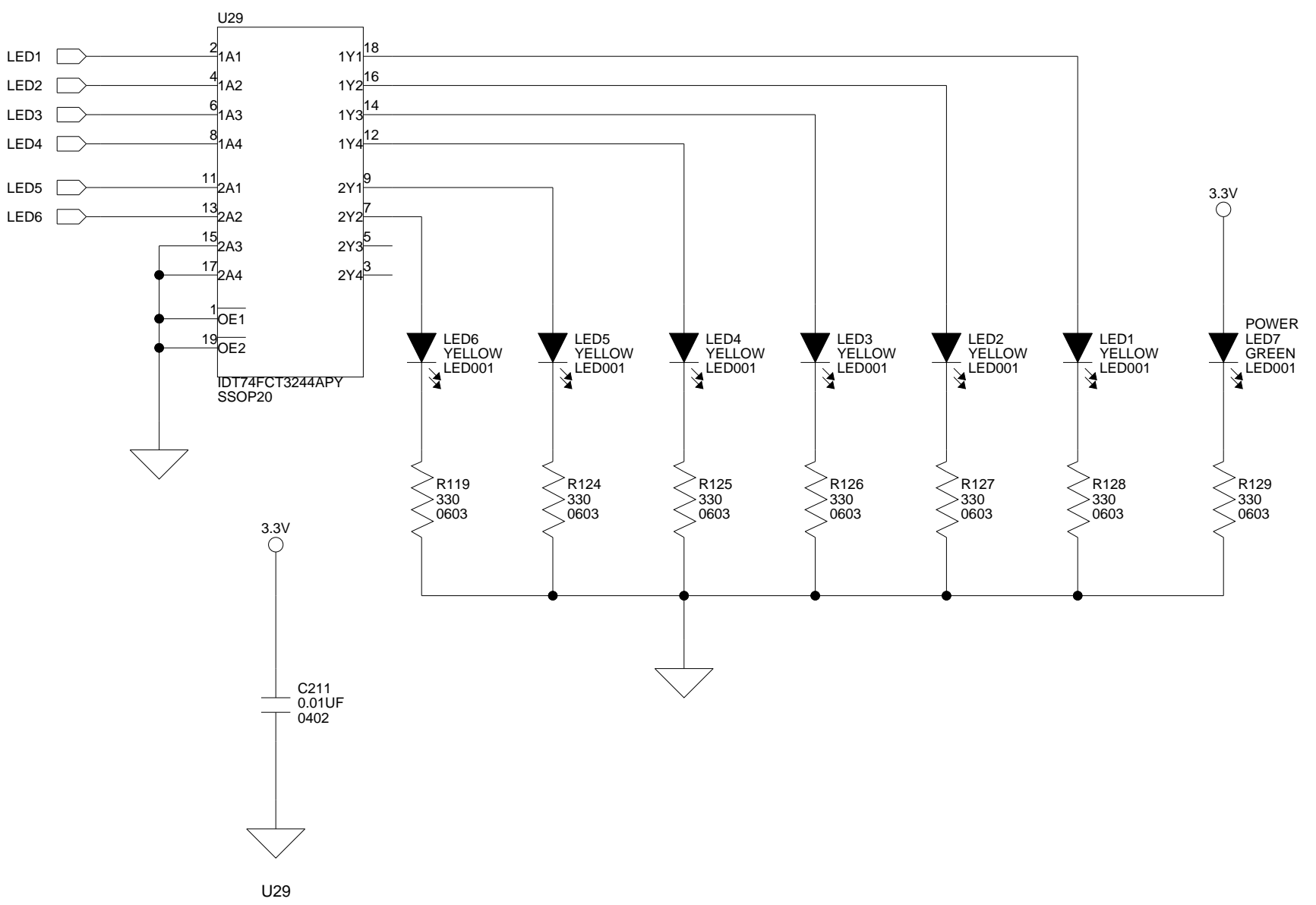
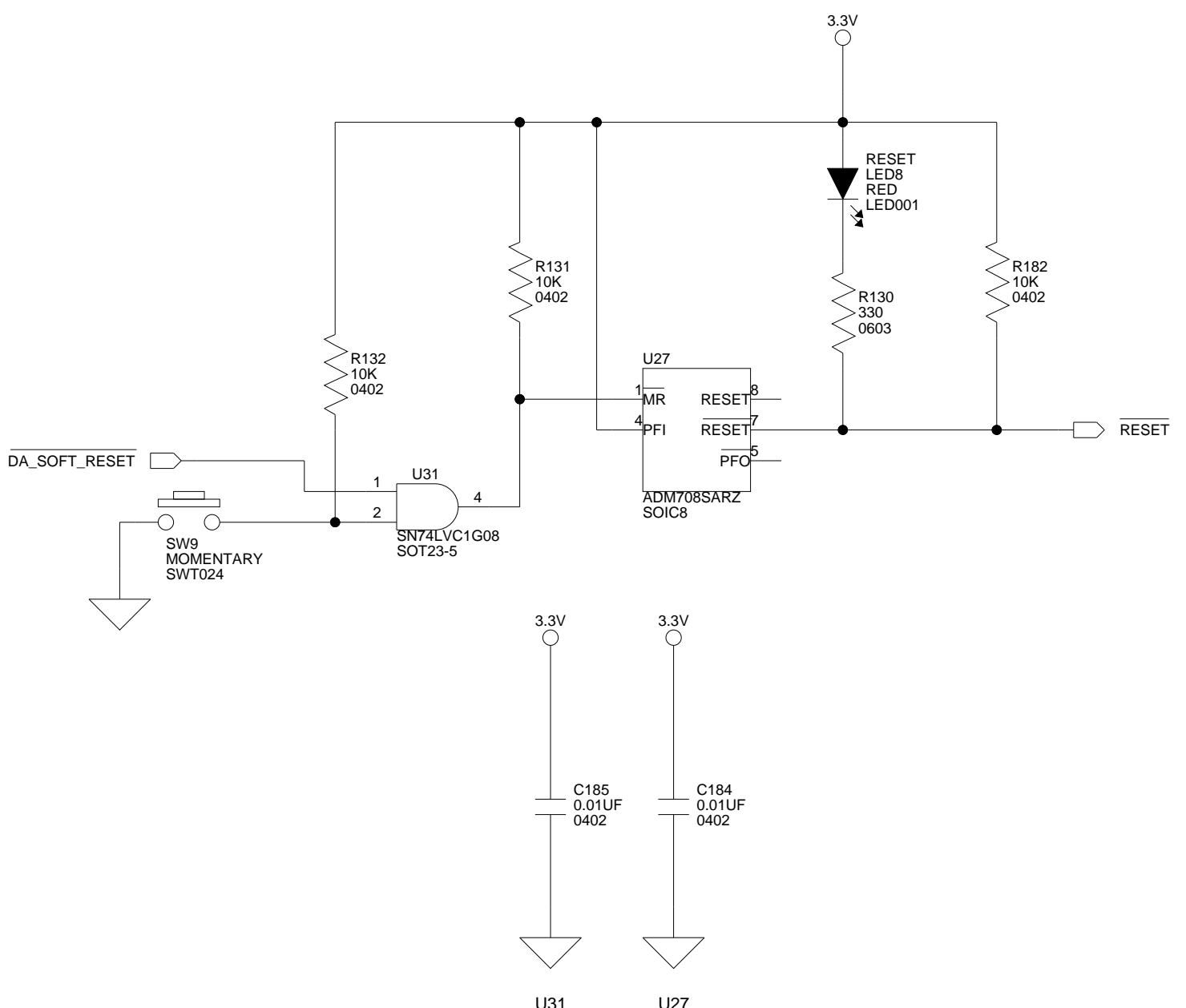
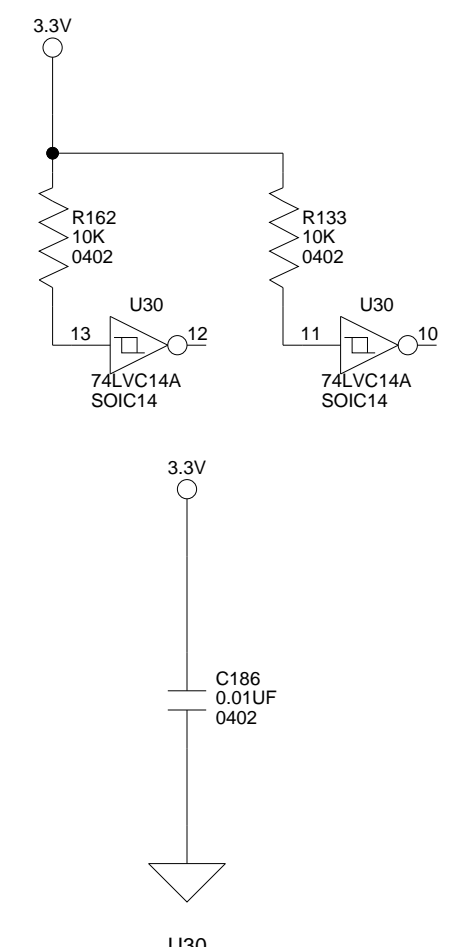
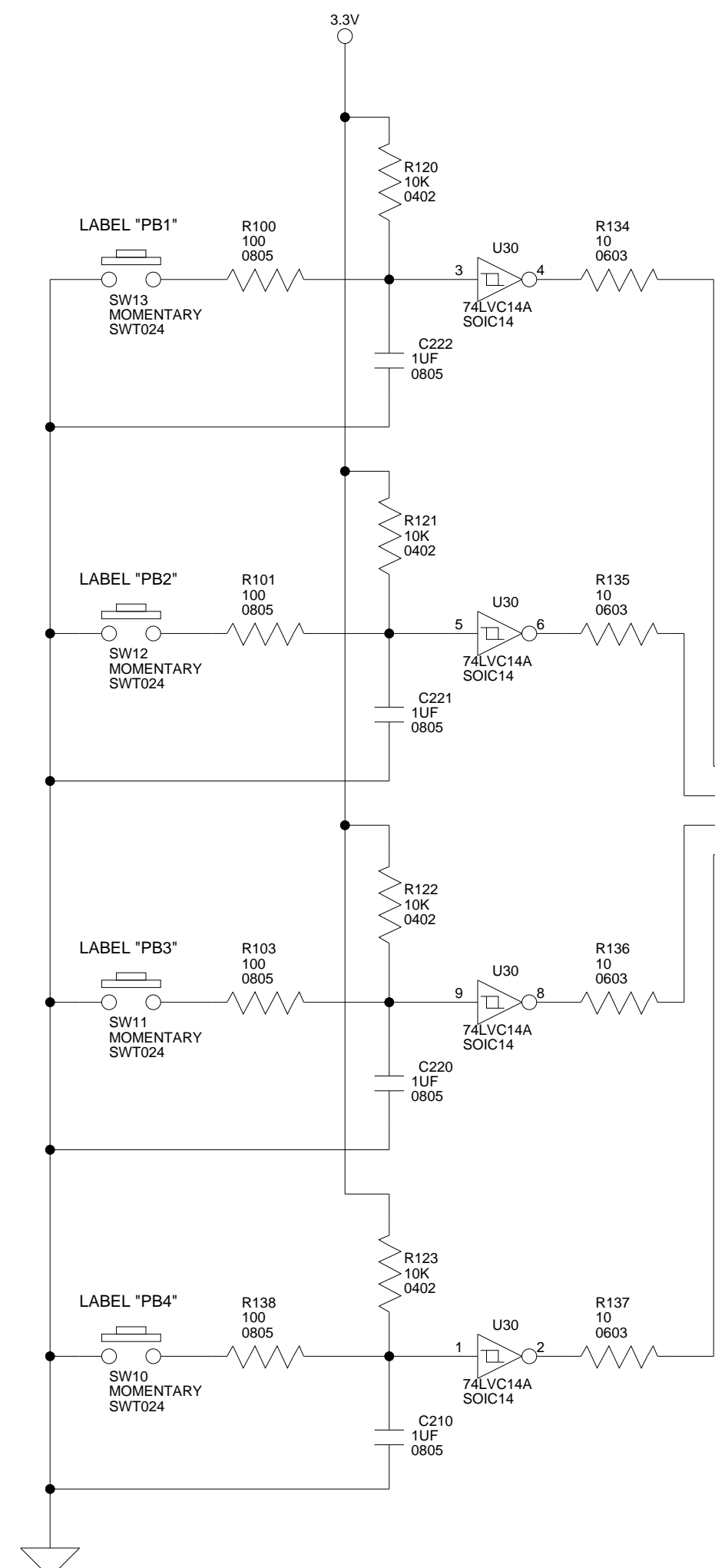
Title ADSP-BF548 EZ-KIT LITE LCD		
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SW5: Push Button Enable Switch

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW5.1	PUSHBUTTON1 (U2 - GPIO: PB8)	PB1 (SW13)	ON	EXPANSION INTERFACE (J2.7 & J2.26) TIMERS (P11.6), SPORT2 (P6.28), SPORT3 (P7.28)
SW5.2	PUSHBUTTON2 (U2 - GPIO: PB9)	PB2 (SW12)	ON	EXPANSION INTERFACE (J2.23), UART3 (P12.3) TIMERS (P11.8), SPORT2 (P6.30), SPORT3 (P7.30)
SW5.3	PUSHBUTTON3 (U2 - GPIO: PB10)	PB3 (SW11)	ON	EXPANSION INTERFACE (J3.31), UART3 (P12.5) TIMERS (P11.10), SPORT2 (P6.32), SPORT3 (P7.32)
SW5.4	PUSHBUTTON4/HPWAIT (U2 - GPIO: PB11)	PB4 (SW10)	ON	HOST INTERFACE (P3.12), NOR_RESET (SW16.4) EXPANSION INTERFACE (J1.85)



SW5: Push Button Enable Switch

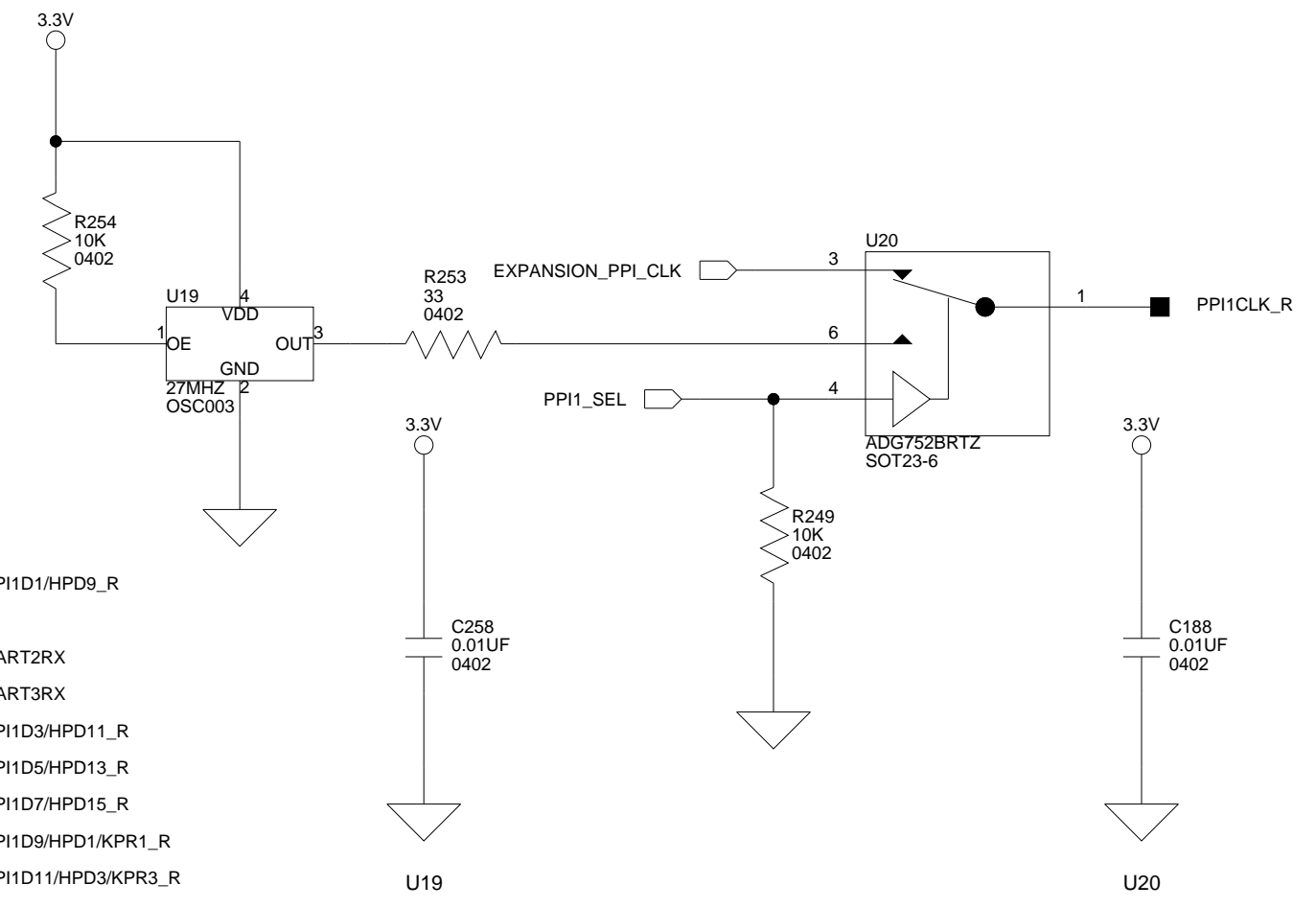
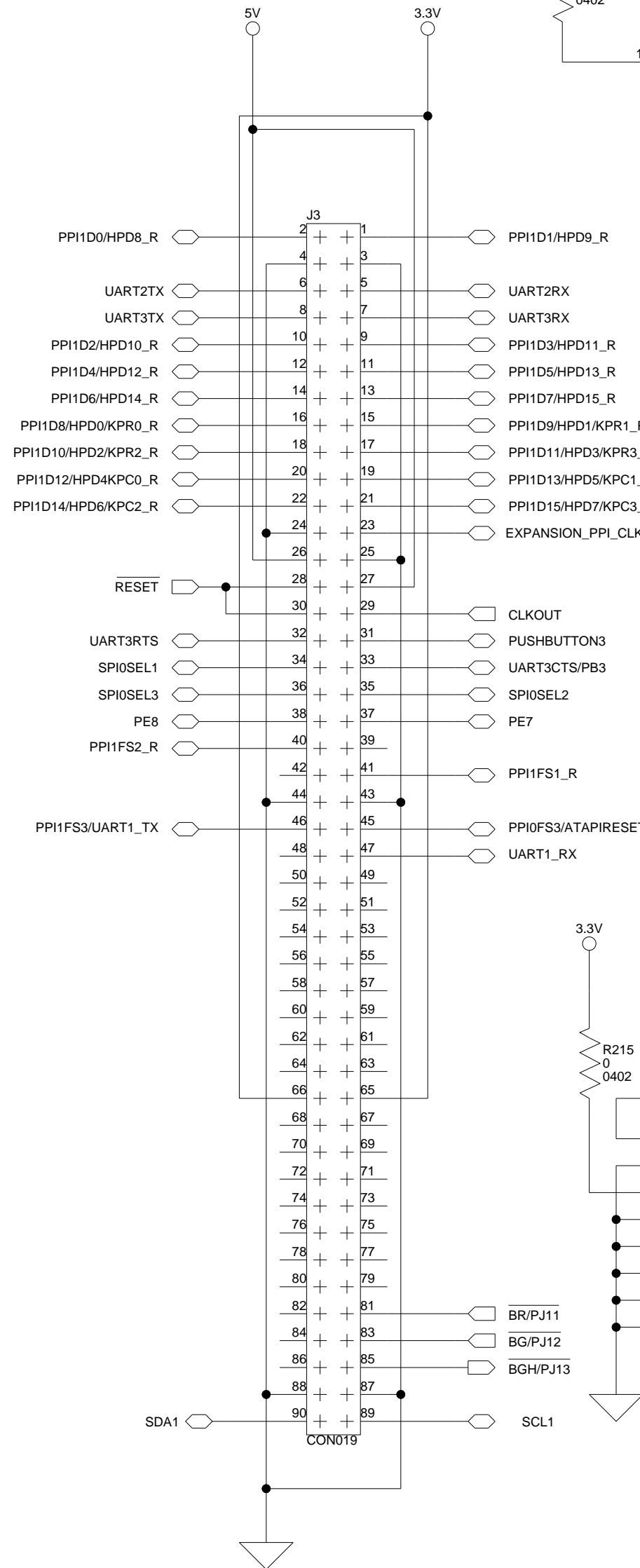
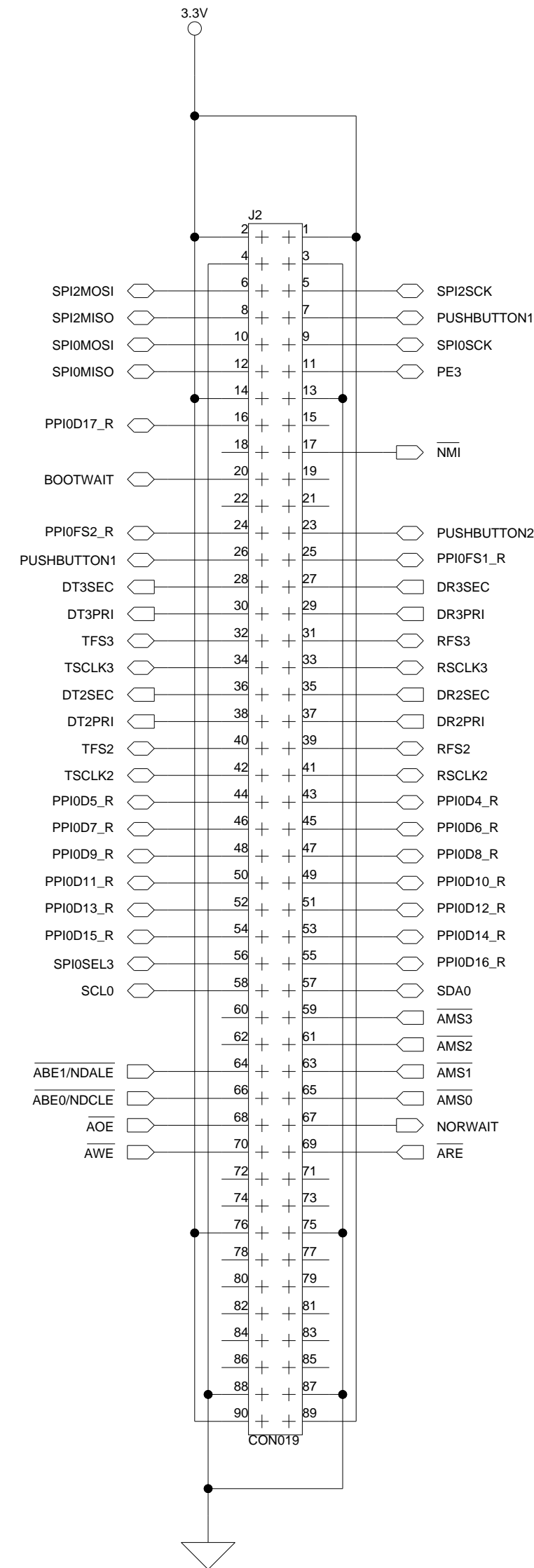
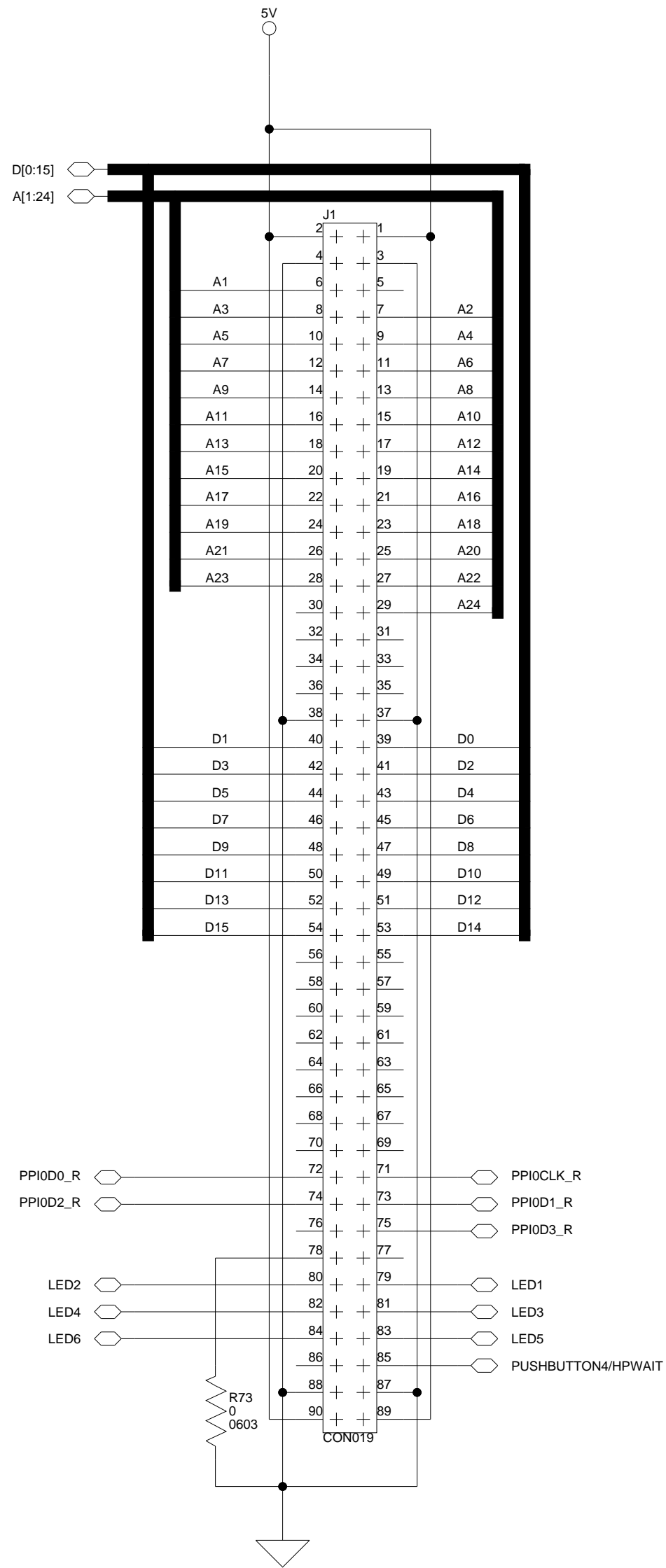


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Title			ADSP-BF548 EZ-KIT LITE PUSH BUTTONS, LEDS AND BOOT MODE		
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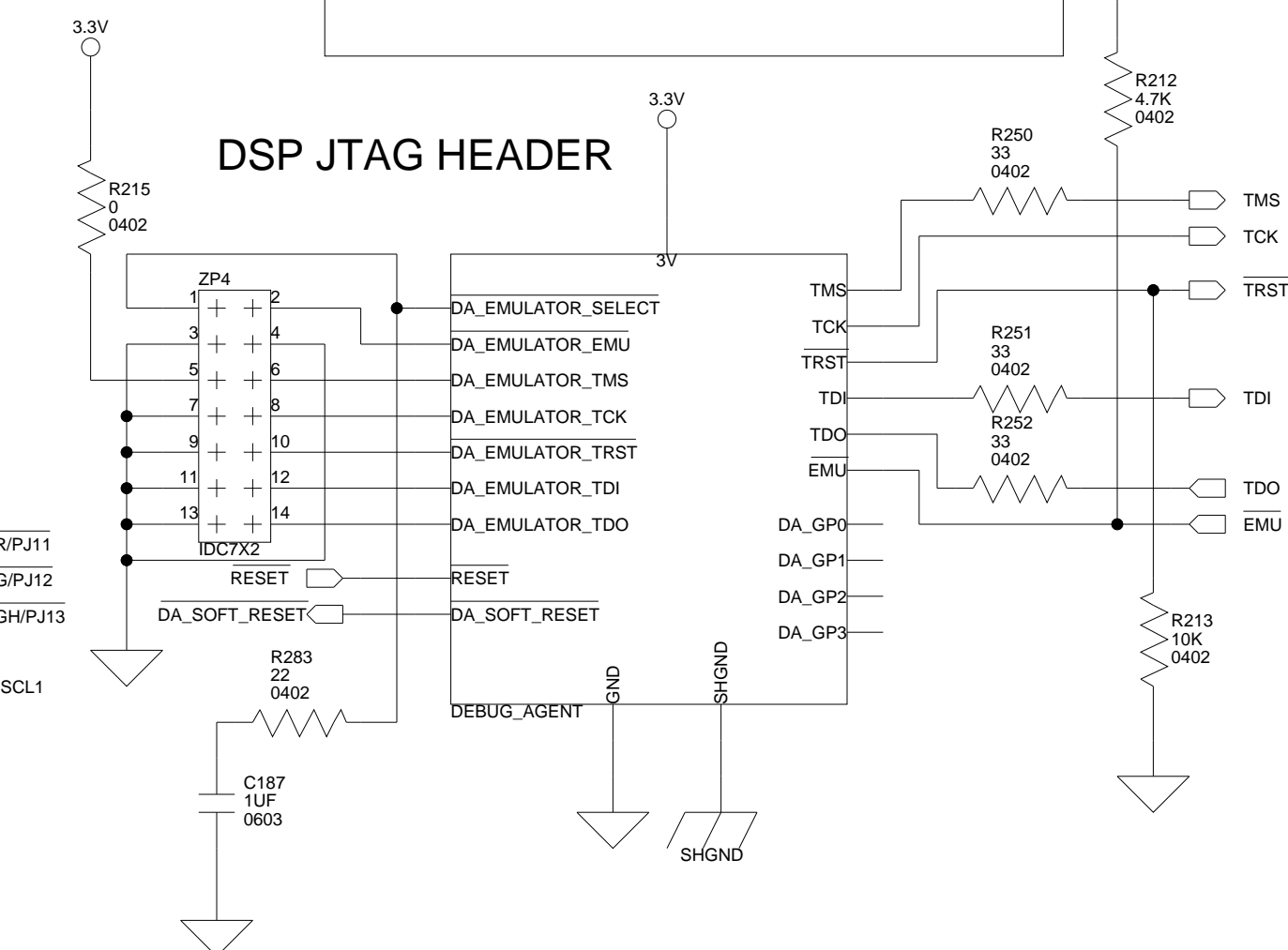
EXPANSION INTERFACE (TYPE B)



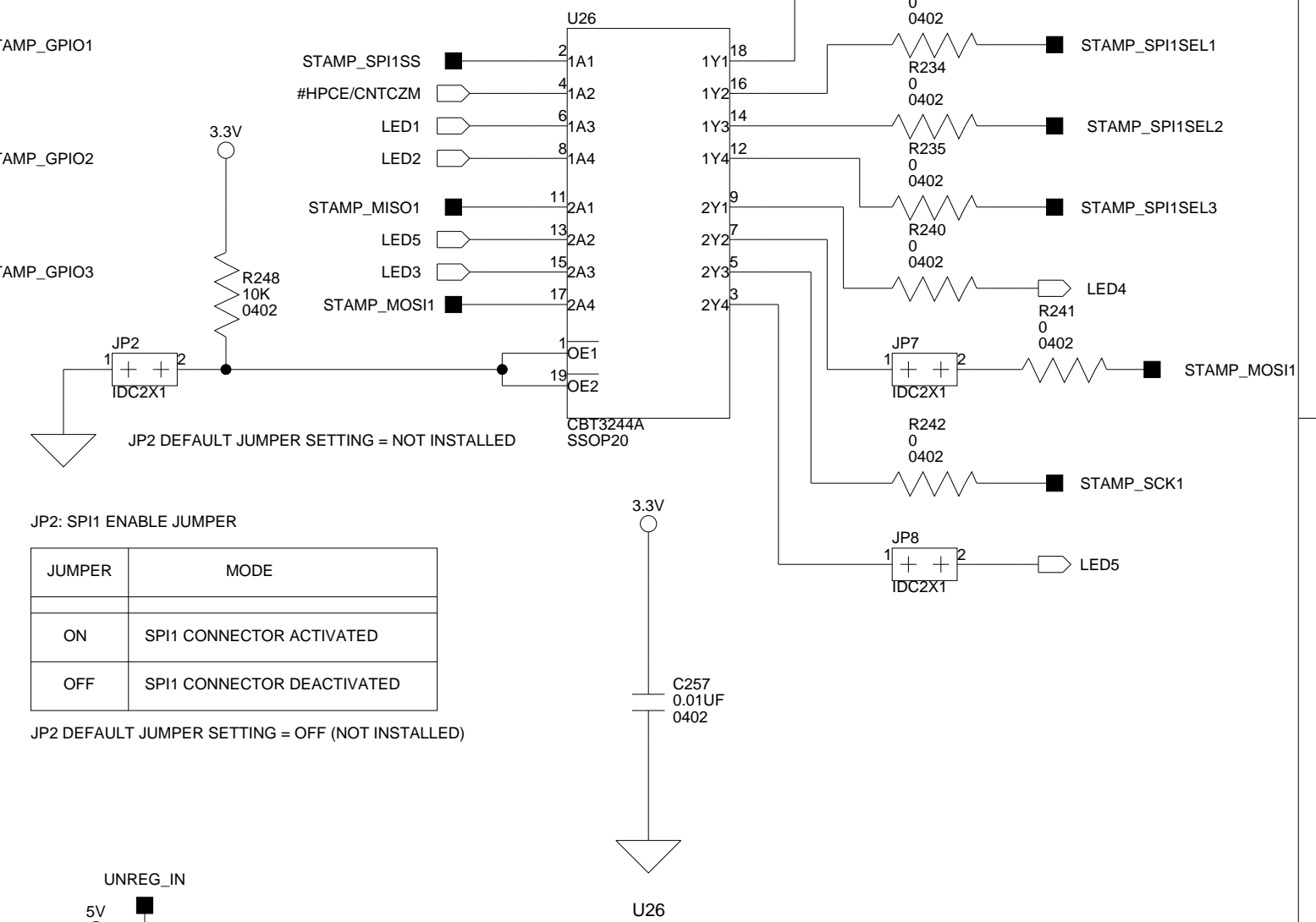
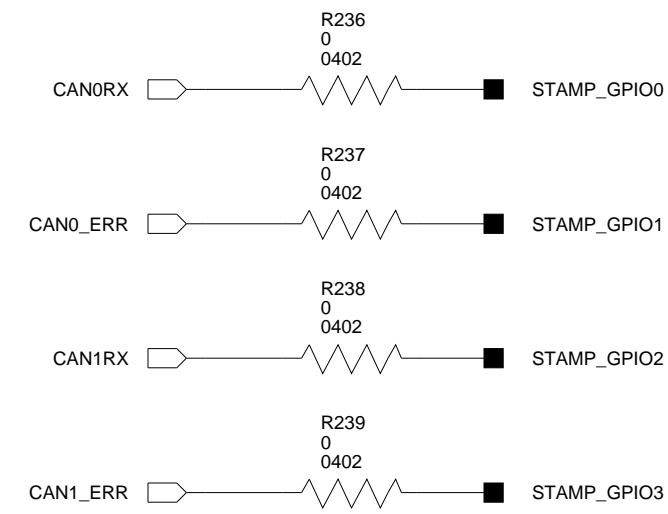
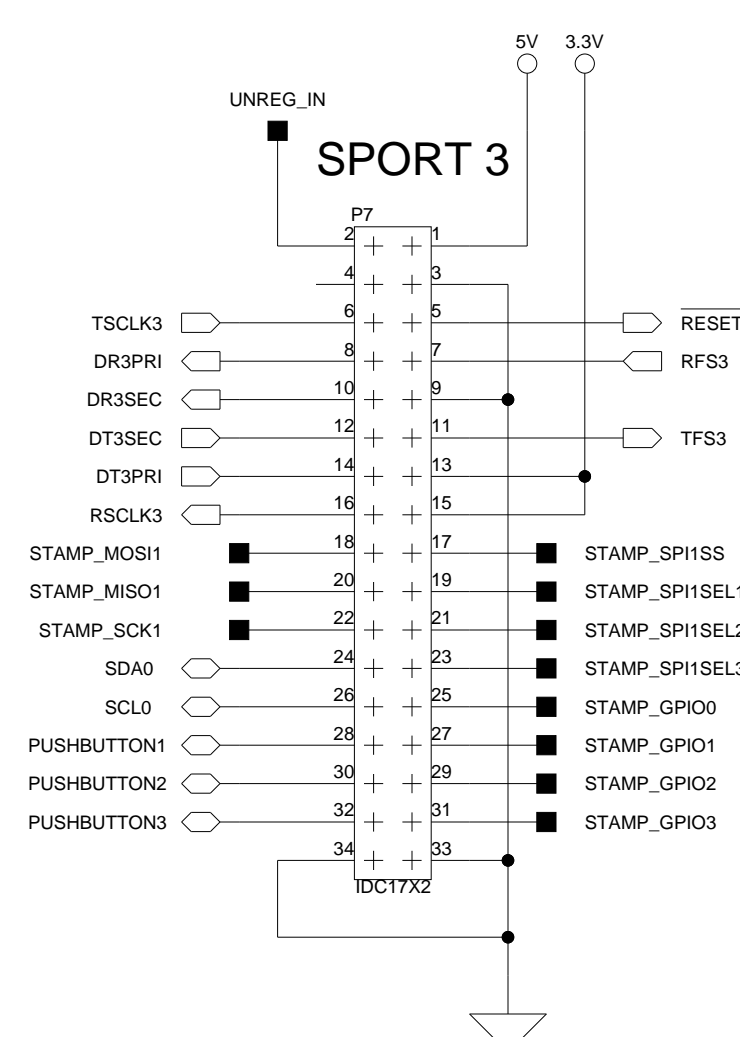
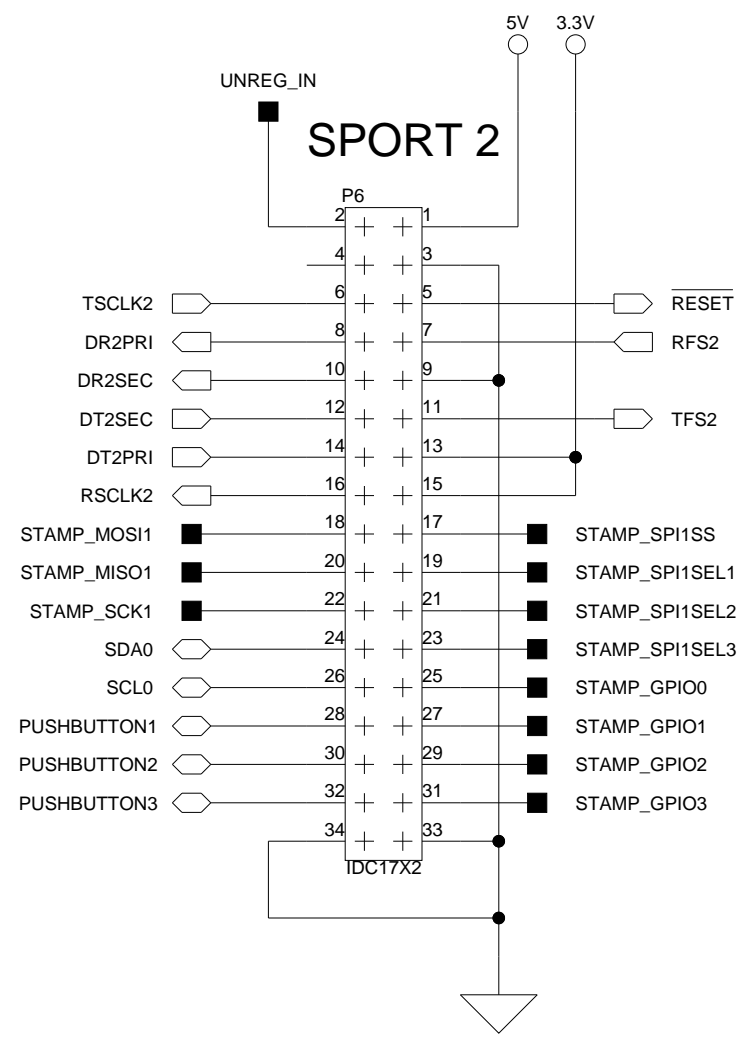
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at <http://www.analog.com>

DSP JTAG HEADER



ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD
Title ADSP-BF548 EZ-KIT LITE EXPANSION INTERFACE & JTAG		
Size C	Board No. A0206-2006	Rev 1.4B
Date 12-4-2007_10:10	Sheet 14 of 17	



JP2: SPI1 ENABLE JUMPER

JUMPER	MODE
ON	SPI1 CONNECTOR ACTIVATED
OFF	SPI1 CONNECTOR DEACTIVATED

JP2 DEFAULT JUMPER SETTING = OFF (NOT INSTALLED)

JP7: MOSI1 OUT JUMPER

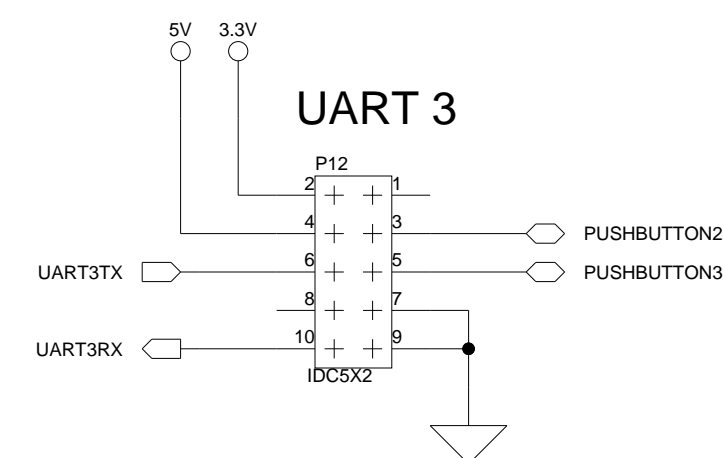
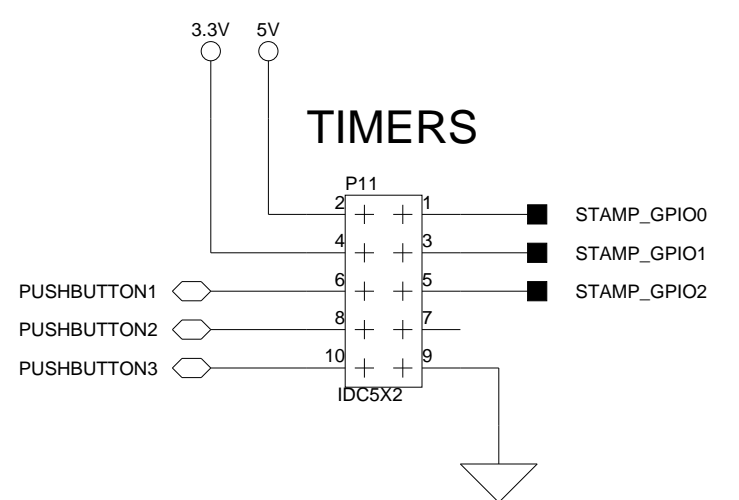
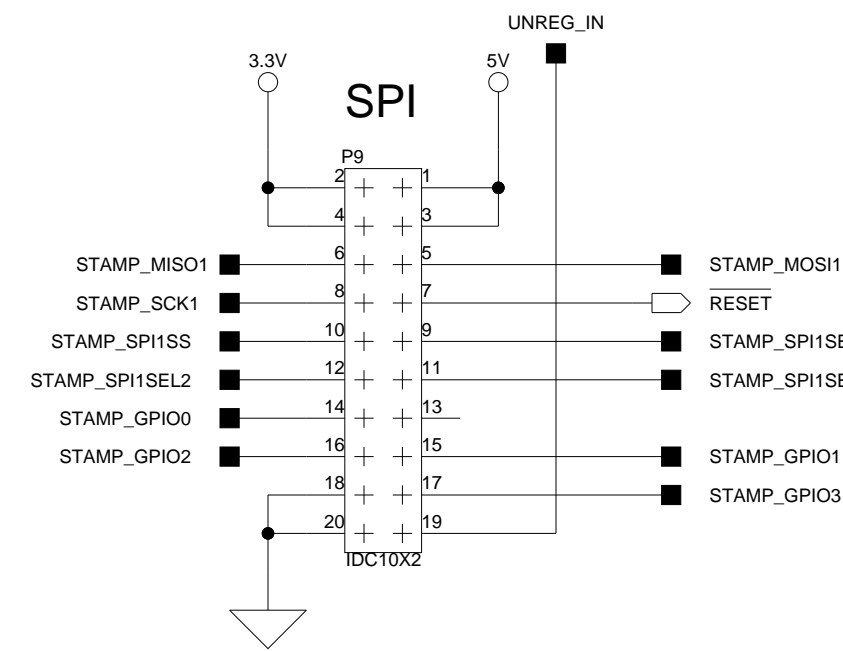
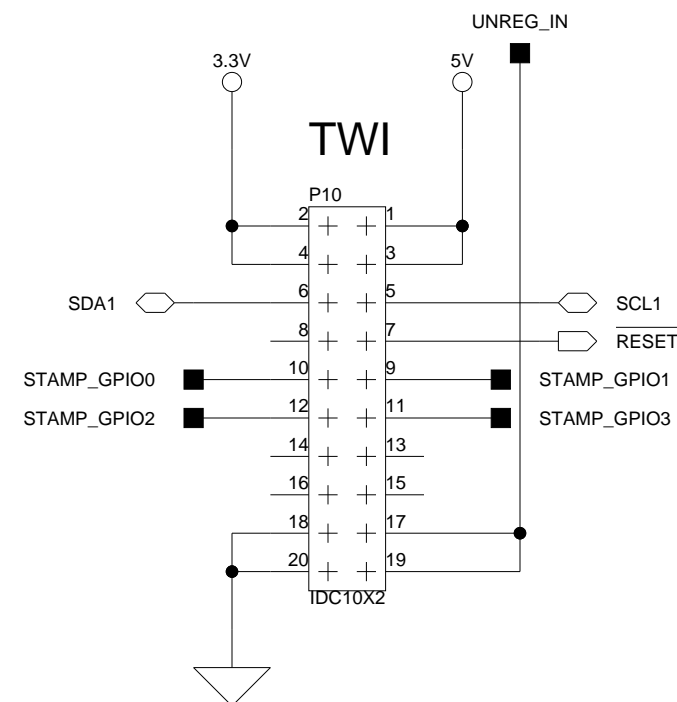
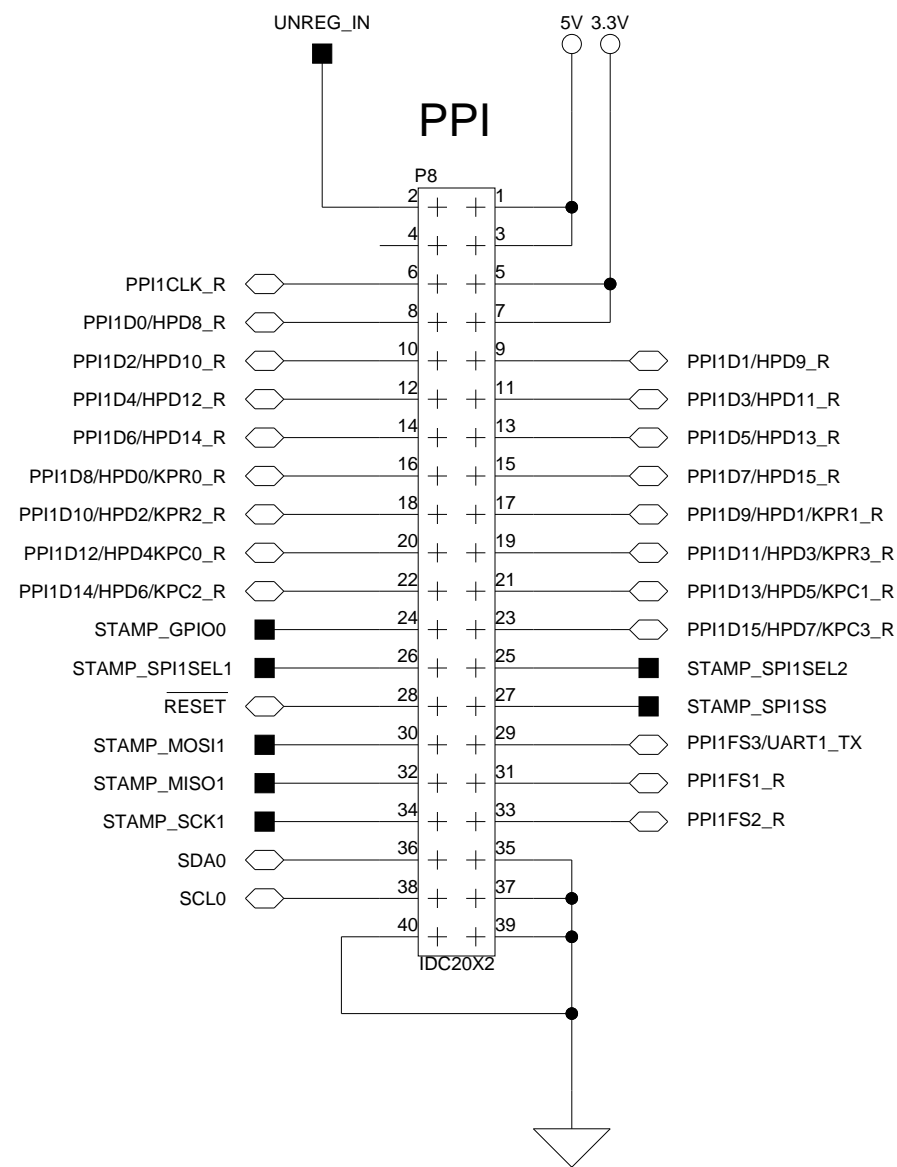
JUMPER	MODE
ON	MOSI1 OF U2 TRANSMITTING TO STAMP CONNECTORS
OFF	NO CONNECTION BETWEEN MOSI1 OF U2 TO STAMP CONNECTORS

JP7 DEFAULT JUMPER SETTING = OFF (NOT INSTALLED)

JP8: MOSI1 IN JUMPER

JUMPER	MODE
ON	MOSI1 OF U2 RECEIVING FROM STAMP CONNECTORS
OFF	NO CONNECTION BETWEEN MOSI1 OF U2 TO STAMP CONNECTORS

JP8 DEFAULT JUMPER SETTING = OFF (NOT INSTALLED)

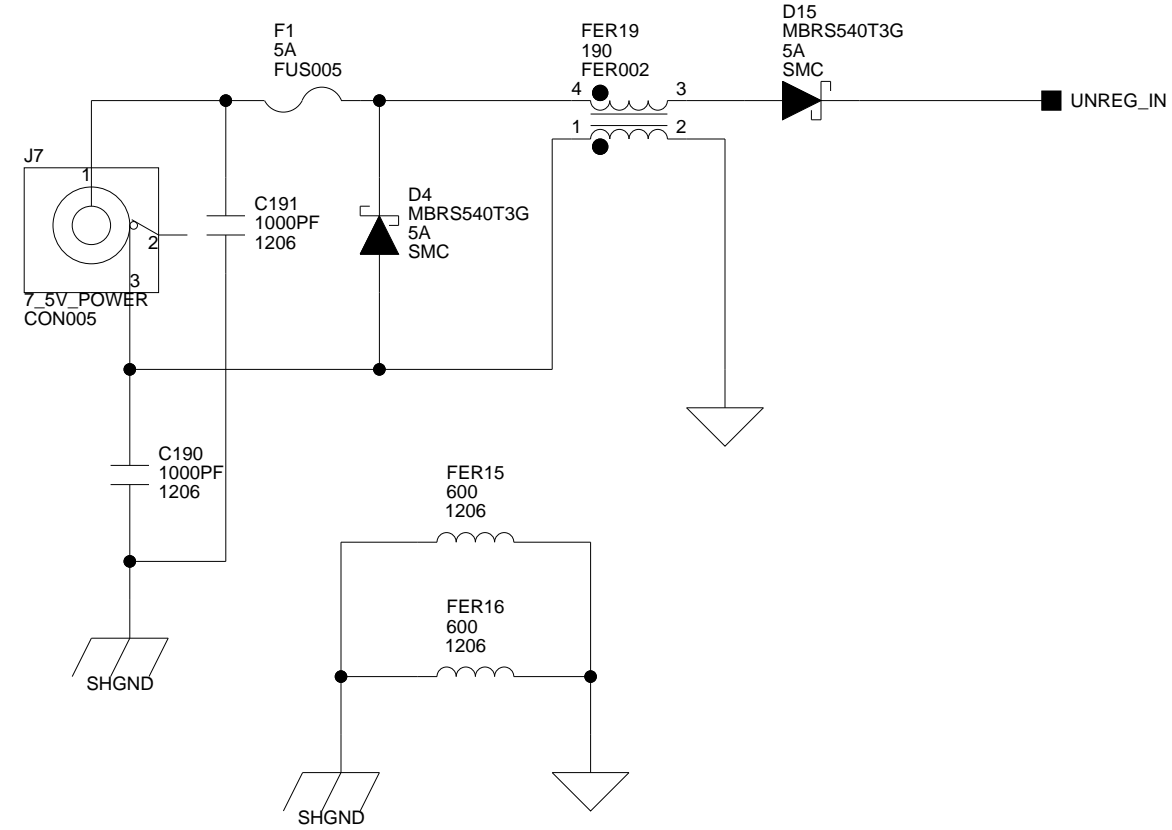


NOTE: PUSHBUTTONS AND TIMERS [2:0] SHARE THE SAME NET NAMES

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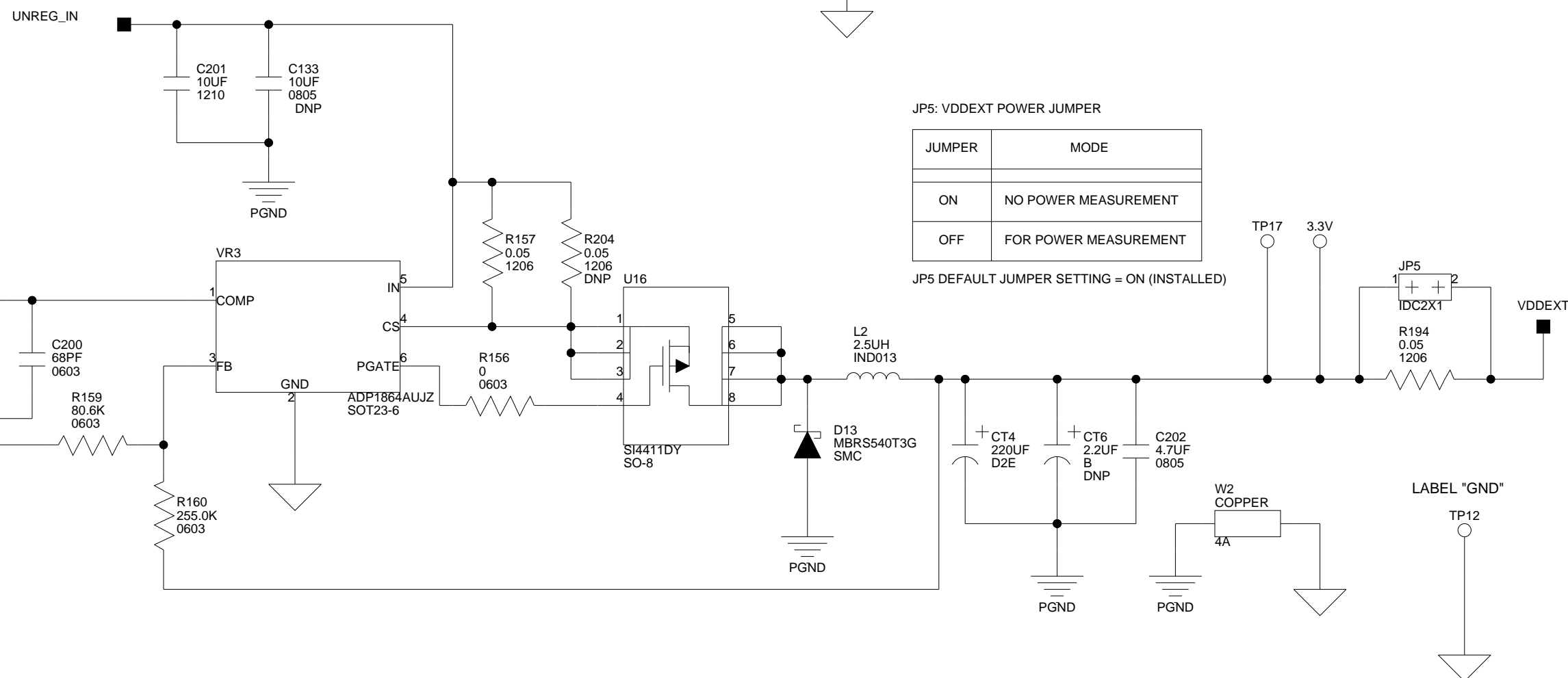
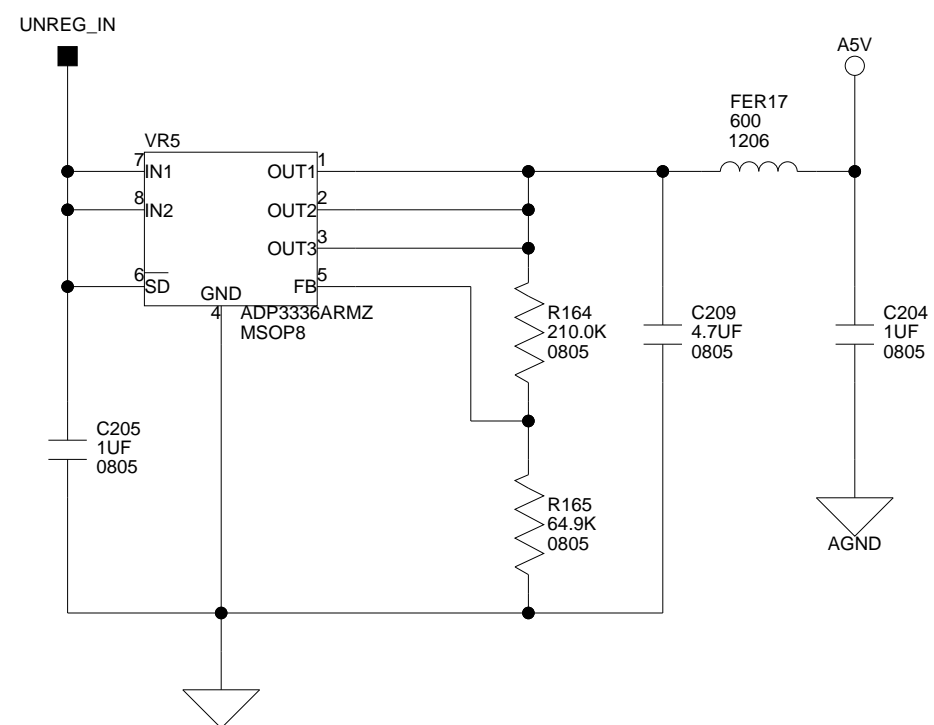
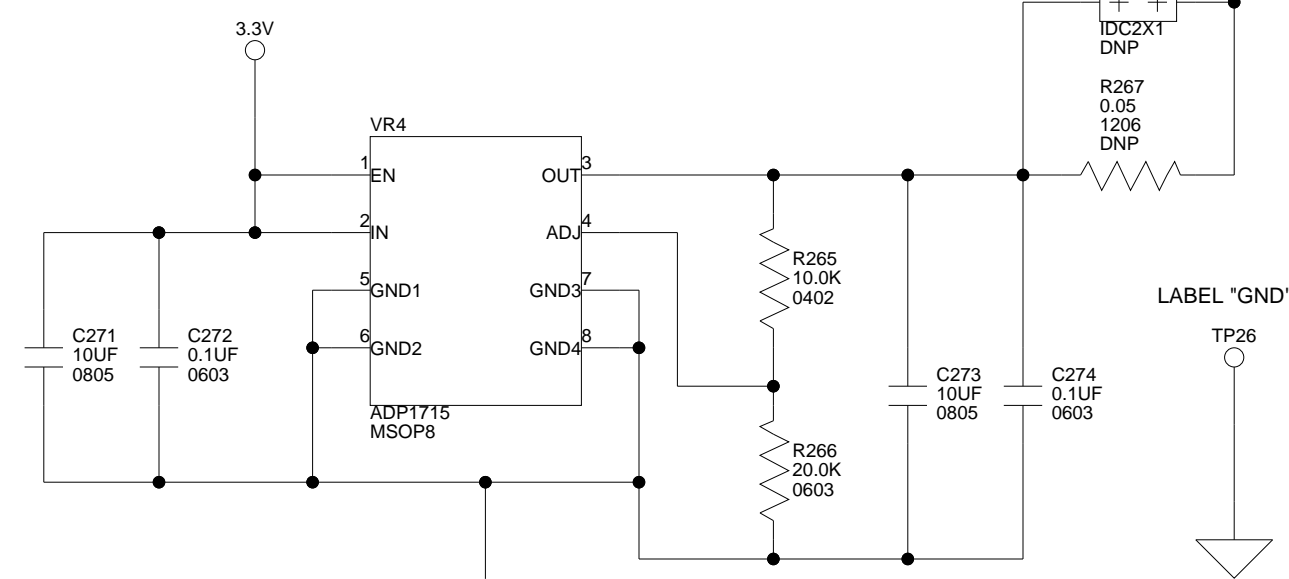
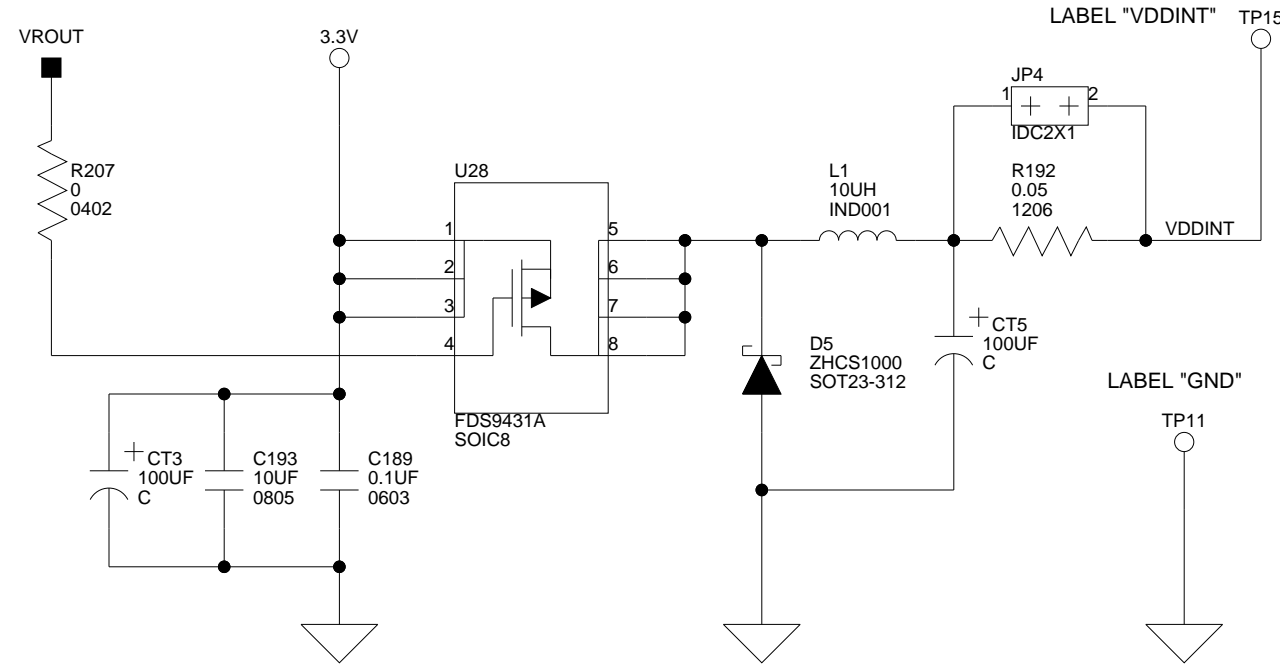
Title			ADSP-BF548 EZ-KIT LITE STAMP CONNECTORS		
Size	Board No.				Rev
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JP4: VDDINT POWER JUMPER

JUMPER	MODE
ON	NO POWER MEASUREMENT
OFF	FOR POWER MEASUREMENT

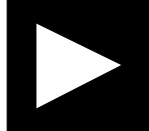
JP4 DEFAULT JUMPER SETTING = ON (INSTALLED)

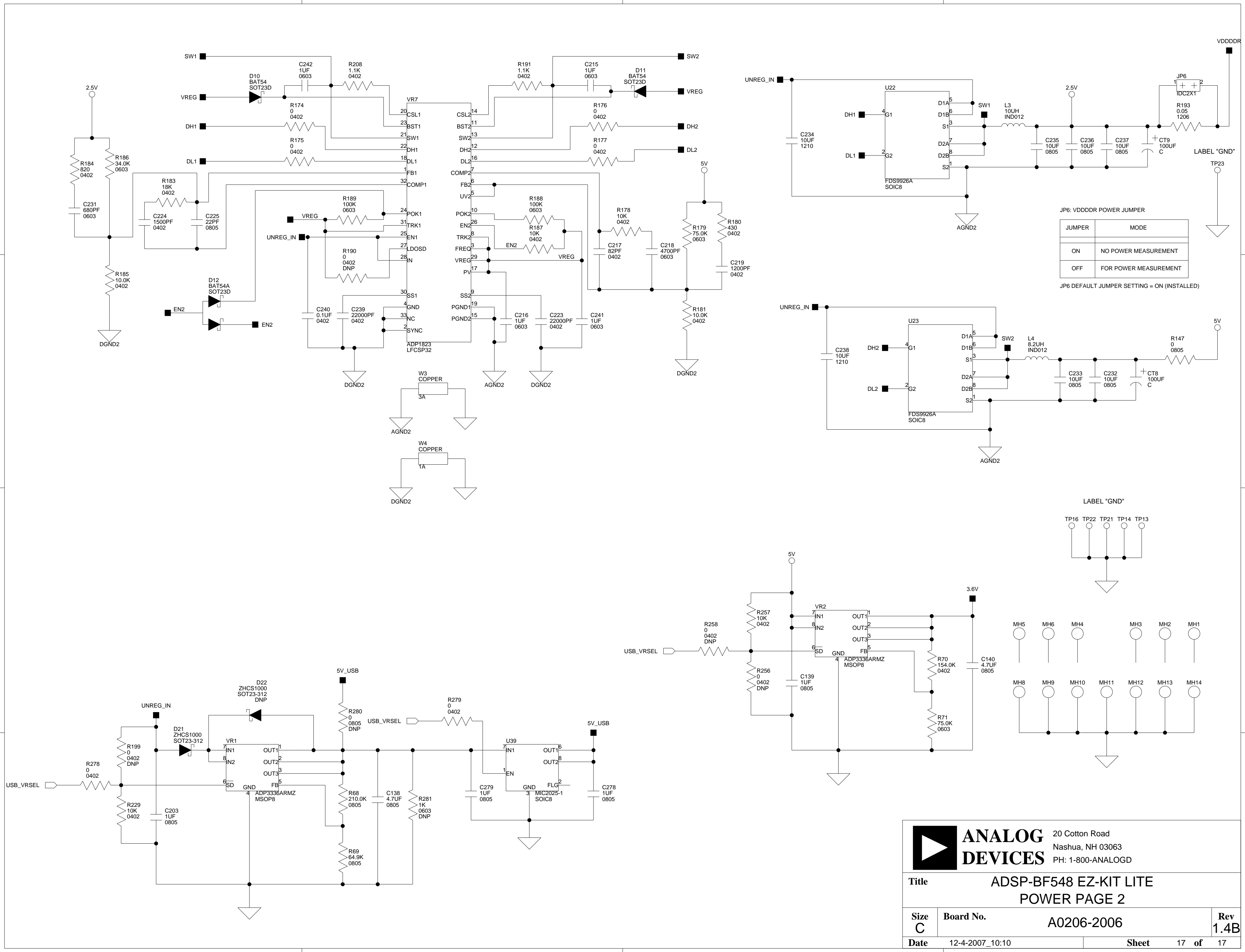


JP5: VDDEXT POWER JUMPER

JUMPER	MODE
ON	NO POWER MEASUREMENT
OFF	FOR POWER MEASUREMENT

JP5 DEFAULT JUMPER SETTING = ON (INSTALLED)

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		Title ADSP-BF548 EZ-KIT LITE POWER PAGE 1		
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JP6: VDDDDR POWER JUMPER

JUMPER	MODE
ON	NO POWER MEASUREMENT
OFF	FOR POWER MEASUREMENT

JP6 DEFAULT JUMPER SETTING = ON (INSTALLED)

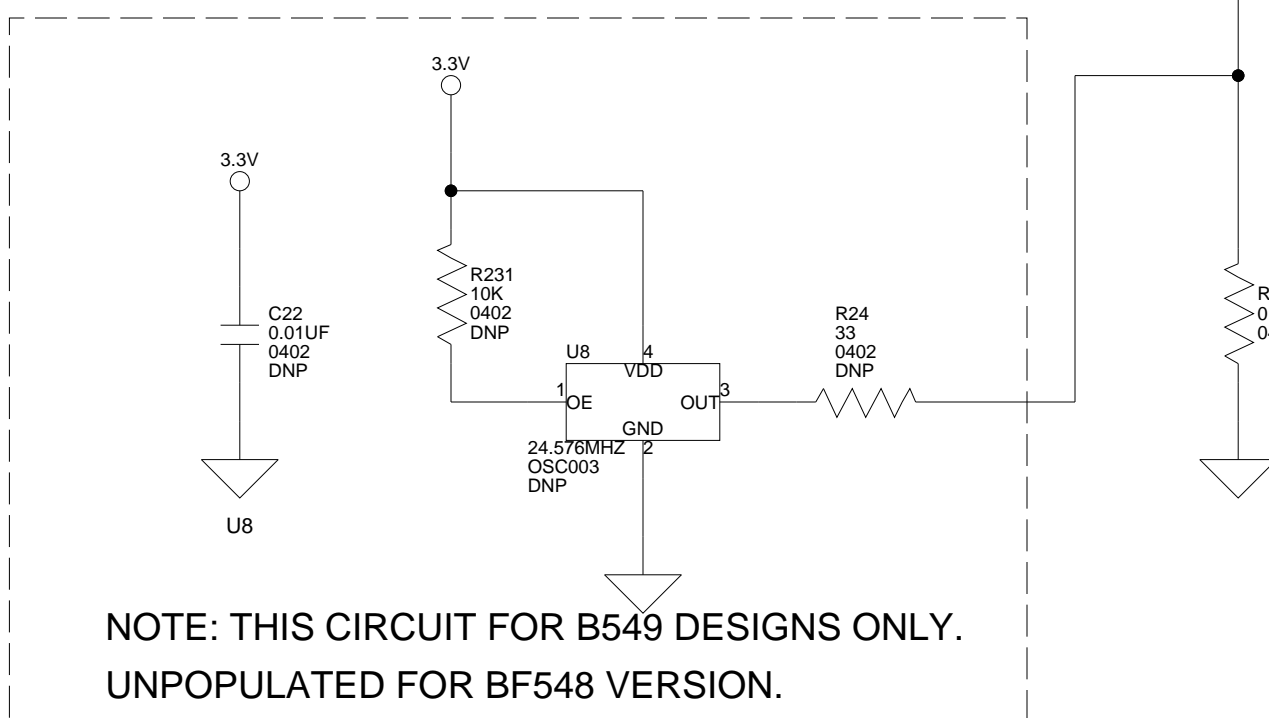
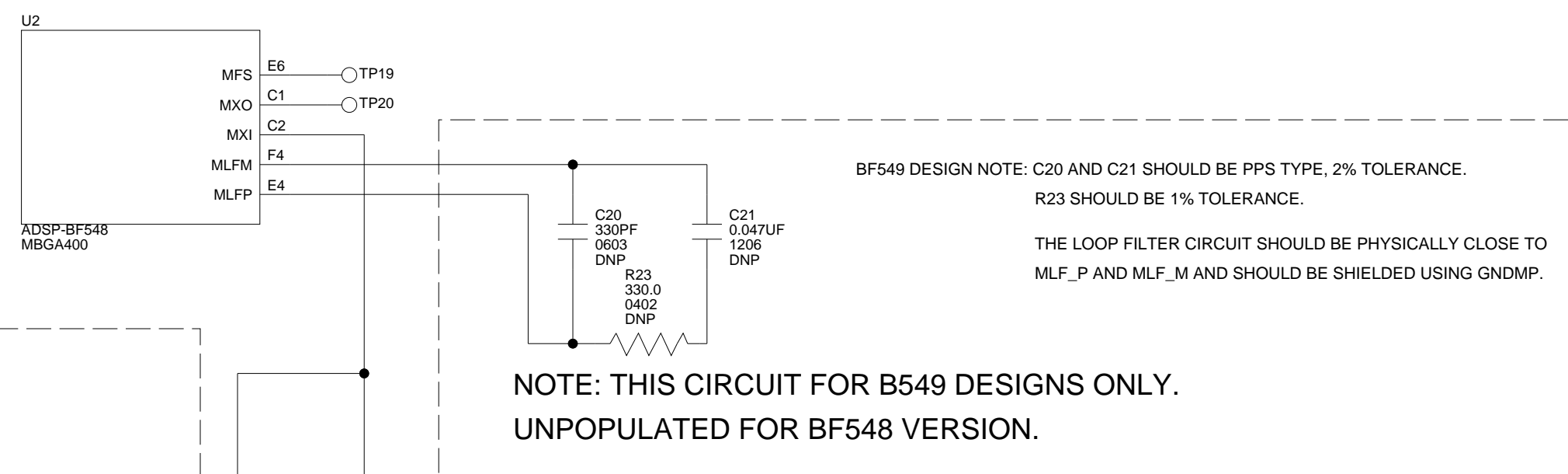
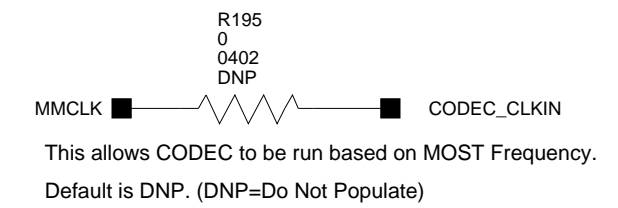
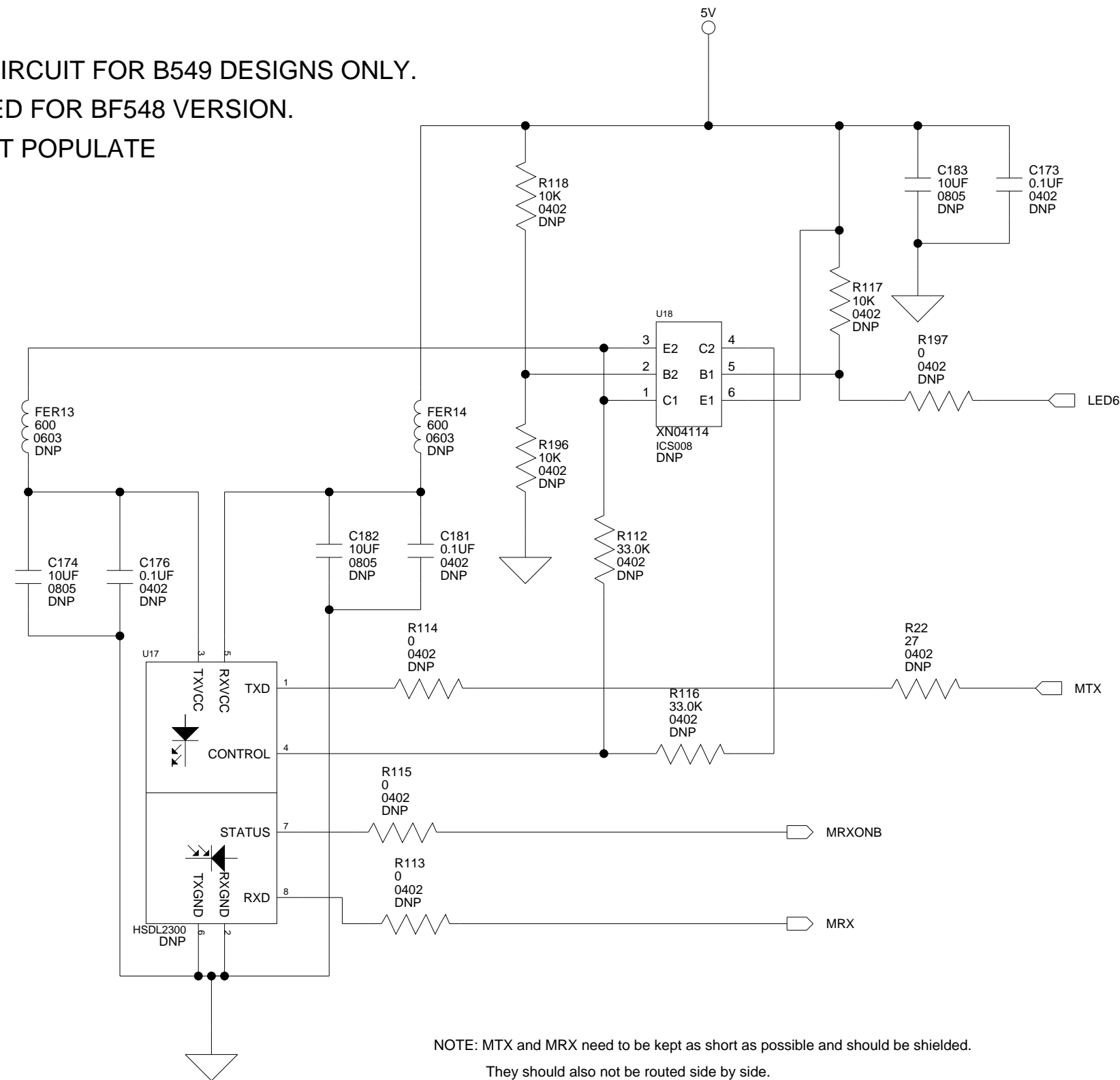
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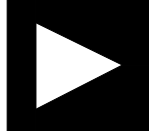
Title		ADSP-BF548 EZ-KIT LITE POWER PAGE 2	
Size C	Board No.	A0206-2006	Rev
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FOR BF549 DESIGNS USING MXVR ALL COMPONENTS
ON THIS PAGE ARE POPULATED EXCEPT: R195,R196,R284,TP19,TP20

NOTE: THIS CIRCUIT FOR B549 DESIGNS ONLY.
UNPOPULATED FOR BF548 VERSION.
DNP = DO NOT POPULATE



NOTE: PULL-DOWN ON MXI NEEDED WHEN NOT USING MXVR. (BF548)
PULL-DOWN SHOULD BE UNPOPULATED FOR MXVR USE. (BF549)

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		Title ADSP-BF548 EZ-KIT LITE MXVR	
Size C	Board No.	A0206-2006	Rev 1.4B
Date	Sheet	1 of	1