

Data

Writing to DAC Register:

P/ $\bar{W}$   $\downarrow$  writing to DAC Register address

0 0 0 1 [18-bits data] X X  
 $\underbrace{\hspace{10em}}$   
 don't care

Hardware control Pins:

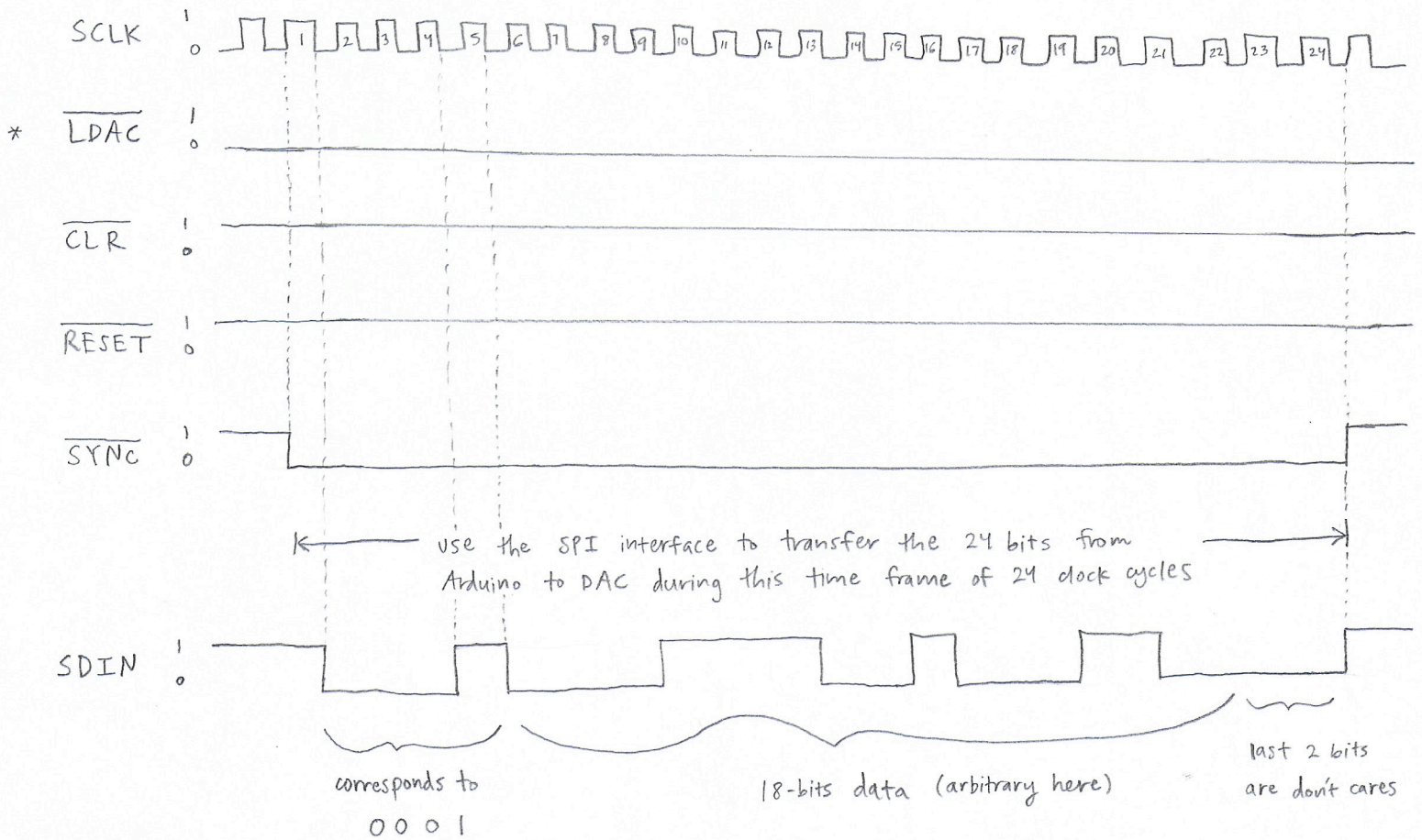
$\overline{LDAC} = 0$

$\overline{CLR} = 1$

$\overline{RESET} = 1$

} function:  
 output set according to DAC register value

Timing Diagram



Note: Data is clocked into the input shift register on the falling edge of the serial clock input (SCLK)

\* In order for output to be updated after writing,  $\overline{LDAC}$  must be taken low while  $\overline{SYNC}$  is high.