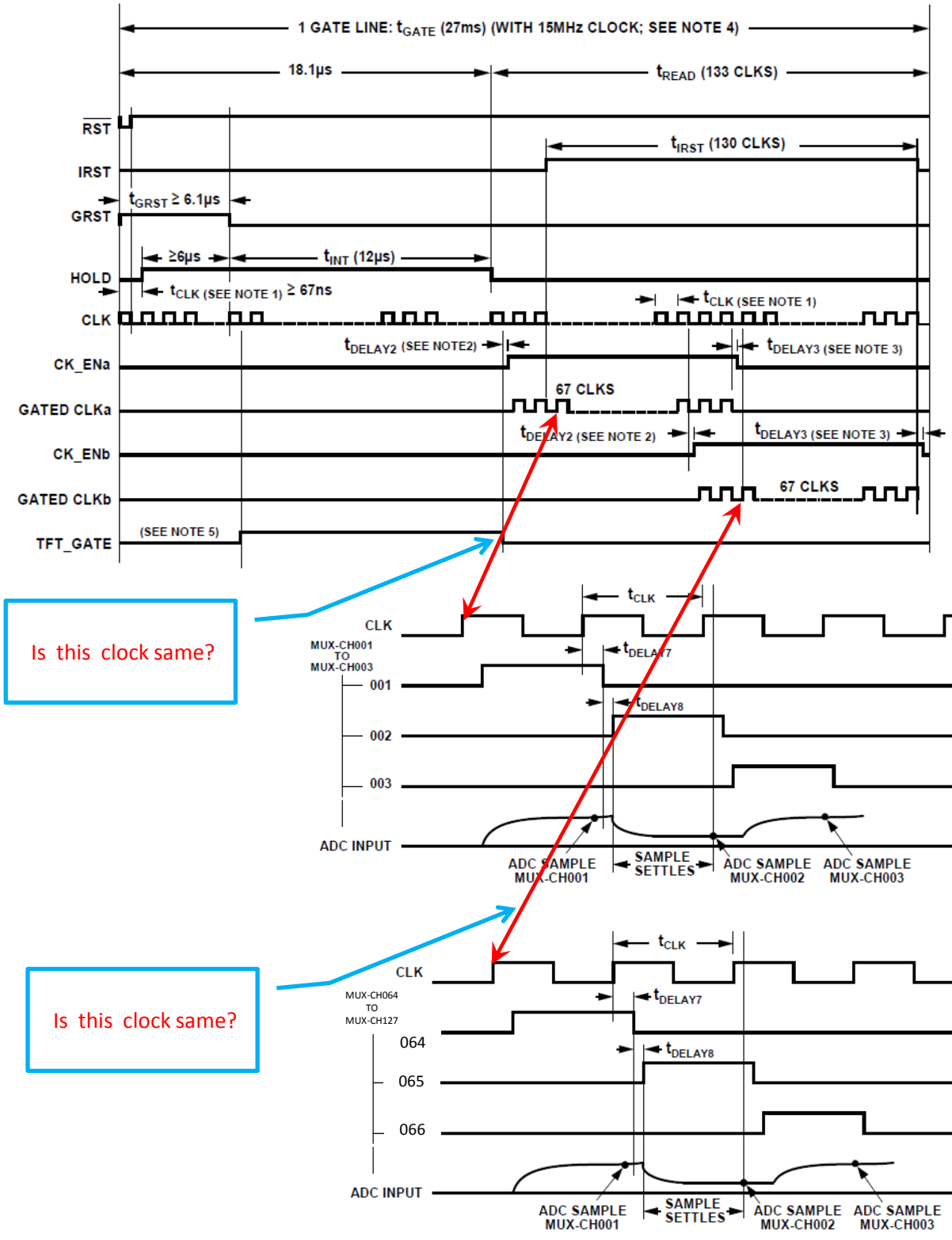
1 GATE LINE: t_{GATE} (27ms) (WITH 15MHz CLOCK; SEE NOTE 4)
18.1µs
t_{READ} (133 CLKS)
RST
IRST
t_{IRST} (130 CLKS)
t_{GRST} ≥ 6.1µs
GRST
≥6µs
t_{INT} (12µs)
HOLD
t_{CLK} (SEE NOTE 1) ≥ 67ns
t_{CLK} (SEE NOTE 1)
CLK
t_{DELAY2} (SEE NOTE2)
t_{DELAY3} (SEE NOTE 3)
CK_ENa
67 CLKS
GATED CLKa
t_{DELAY2} (SEE NOTE 2)
t_{DELAY3} (SEE NOTE 3)
CK_ENb
67 CLKS
GATED CLKb
(SEE NOTE 5)
TFT_GATE
Is this clock same?
t_{CLK}
CLK
MUX-CH001 TO MUX-CH003
t_{DELAY7}
001
t_{DELAY8}
002
003
ADC INPUT
ADC SAMPLE MUX-CH001
SAMPLE SETTLES
ADC SAMPLE MUX-CH002
ADC SAMPLE MUX-CH003
Is this clock same?
t_{CLK}
CLK
MUX-CH064 TO MUX-CH127
t_{DELAY7}
064
t_{DELAY8}
065
066
ADC INPUT
ADC SAMPLE MUX-CH001
SAMPLE SETTLES
ADC SAMPLE MUX-CH002
ADC SAMPLE MUX-CH003