FAQ-GENERAL MATCHING METHODOLOGY

Since the 9361 RF Ports are differential, there are multiple ways to model a given port impedance.

1. Series Equivalent Differential Impedance(SEDZ): Tables or Graphs.
2. Parallel Equivalent Differential Impedance(PEDZ): Tables or Graphs.
3. 2-Port "S" Data: Touchstone Files.

Note that:

- The RX LNA Input ports may be utilized in a "single-ended" mode. The "single-ended" by hand impedance matching techniques are the same as the bisected "differential" mode impedance matching techniques.
- The "single-ended" CAD based RX system modeling is different when compared to the "differential" mode CAD modeling setup. The main differences are the "S" data file and the system LNA simulation does not require a center-tapped transformer.

Choosing the best differential impedance format is a function of the impedance matching technique. Hand impedance matching calculations (calculator) are best supported with SEDZ data or PEDZ data. CAD based impedance matching is best supported with 2-Port "S" data.

Understanding the format of the Analog Devices provided differential impedance data (Tables or Graphs) is very important when hand calculating (calculator) impedance matching options.

Series Equivalent Differential Impedance (SEDZ) Model Details

The SEDZ format schematic is represented by Figure 55 and Equation 31.

$$SEDZ = R_s + JX_s \quad (1)$$

The "+" implies "in series". JX_s may be positive (inductive) or negative (capacitive).

Parallel Equivalent Differential Impedance (PEDZ) Model Details

The PEDZ format is represented by Figure 56 and Equation 32.

$$PEDZ = R_p \,//\, JX_p \quad (2)$$

The "//" implies "in parallel". JX_p may be positive (inductive) or negative (capacitive).

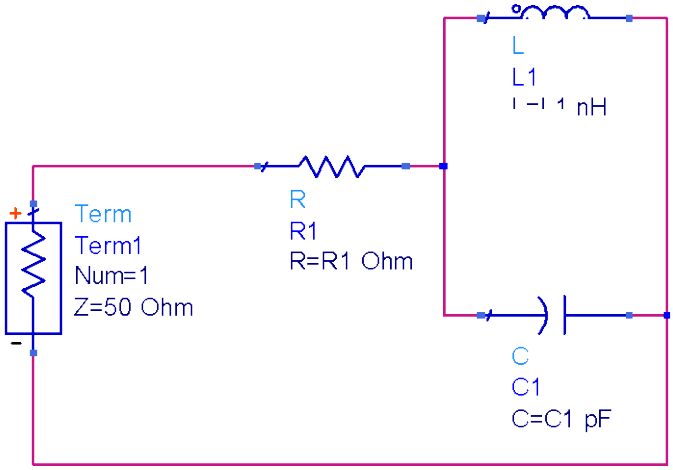

Figure 1. Series Equivalent Differential Impedance (SEDZ)

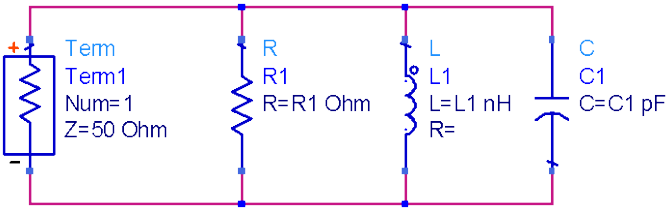

Figure 2. Parallel Equivalent Differential Impedance (PEDZ)

SEDZ to PEDZ Differential Impedance Model Conversion

From a network theory perspective, both impedance formats (SEDZ, PEDZ) are equivalent. The PEDZ format may be calculated from the SEDZ format. See Equation 33 and Equation 34.

$$R_P = 1 / real[SEDY] = 1 / real[(1 / (R_S + JX_S))] \quad (3)$$

$$JX_P = -1 / imag[SEDY] = -1 / imag[(1 / (R_S + JX_S))] \quad (4)$$

Example 1: SEDZ to PEDZ Conversion

SEDZ = 100-J20 Ω

$R_P = 1 / real[SEDY] = 1 / real[(1 / (R_S + JX_S))] = 1 / real[(1 / (100 + J(-20)))] = 104\ \Omega$

$JX_P = -1 / imag[SEDY] = -1 / imag[(1 / (R_S + JX_S))] = -1 / imag[(1 / (100 + J(-20)))] = -J520\ \Omega$

PEDZ = 104 // -J520 Ω

PEDZ to SEDZ Differential Impedance Model Conversion

The SEDZ format may be calculated from the PEDZ format. See Equation 35 and Equation 36.

$$R_S = real[1 / PEDY] = real[1 / ((1/R_P) - J(1/X_P))] \quad (5)$$

$$JX_S = imag[1 / PEDY] = imag[1 / ((1/R_P) - J(1/X_P))] \quad (6)$$

Example 2 : PEDZ to SEDZ Conversion

PEDZ = 104 // -J520 Ω

$R_S = real[1 / PEDY] = real[1 / ((1/R_P) - J(1/X_P))] = real[1 / ((1/104) - J(1/(-520)))] = 100\ \Omega$

$JX_S = imag[1 / PEDY] = imag[1 / ((1/R_P) - J(1/X_P))] = imag[1 / ((1/104) - J(1/(-520)))] = -J20\ \Omega$

SEDZ = 100-J20 Ω

SEDZ and PEDZ Impedance Modeling : Important Points

1. The SEDZ model is equivalent to the PEDZ model. Conversion between models is straightforward.
2. Understanding the differential impedance model format is critical when utilizing "by-hand" methods to design impedance matching networks.
3. The AD9361 Table or Graph based impedance data is delivered by Analog Devices in SEDZ format.

Hand (Calculator) Matching Overview

The hand calculation impedance matching process is fairly straightforward.

1. Define the "Source" and "Load" Impedance Models. Pay attention to the model type (SEDZ vs. PEDZ).
2. Utilize the equations that are associated with the selected impedance matching network topology to generate "rough" component values.
3. Utilize CAD to refine the impedance matching network "rough" component values.
4. Test the match performance in the lab.

Example 1: Matching to a 50 Ω Differential Source with a SEDZ Load Impedance Model. : Differential "L" Techniques

This example highlights the process to match a 50 Ω differential Source to a SEDZ modeled Load impedance of 100 –J20 Ω. The impedance matching network would be installed between Ports 1, 2, 3, and 4. See Figure 57.

Assuming a perfect differential system, one can bisect the network into a couple of "single-ended" sections. See Figure 58. Both the real(SEDZ) and the imag(SEDZ) are divided by2.

This bisected network enables easy calculations for the matching component values.

For simplicity, a differential "L" network will be designed.

A differential "L" network is three components. 1 "shunt" component and 2 "series" components. This network topology represents the most basic of all matching networks. Depending on the frequency bandwidth and the source/load impedance variance over frequency, a differential "PII" or cascaded differential "L" network topologies may also be a good/better choice.

We only need to concentrate on the upper half of Figure 58.

1. By inspection, the first element (traveling from the Load) is a series +J10 element. This will resonate out the Load reactance.
2. The next step is to calculate the "L" network required to match a pure 50 Ω Load to a pure 25 Ω Source.
3. A "shunt" matching element is always placed on the side (source or load) with the largest resistance. In this case, R_{large} is on the Load end. Calculate the Impedance Transformation Q.

   $$Q_t = \text{sqrt}(R_{large}/R_{small} - 1) \quad (7)$$

   $$Q_t = \text{sqrt}(50/25 - 1) = 1.0$$

4. Calculate the "shunt" element matching reactance with Equation 38.

   $$|X_{shunt}| = R_{large}/Q_t \quad (8)$$

   $$|X_{shunt}| = 50/1.0 = 50\ \Omega$$

5. Calculate the "series" element matching reactance with Equation 39.

   $$|X_{series}| = Q_t * R_{small} \quad (9)$$

   $$|X_{series}| = 1.0*25 = 25\ \Omega$$

6. Since the original system was bisected, the "shunt" matching reactance must be modified to work within a differential system. Equation 40 implements the conversion.

   $$|X_{shunt\_diff}| = 2*|X_{shunt}| \quad (10)$$

   $$|X_{shunt\_diff}| = 2*50 = 100\ \Omega$$

Given the "shunt" and "series" reactance magnitudes, the only constraint is they must be opposite signs. If the "shunt" reactance is selected as inductive (+) then the "series" reactance must be capacitive (-). If the "shunt" reactance is selected as Capacitive (-) then the "series" reactance must be Inductive (+).

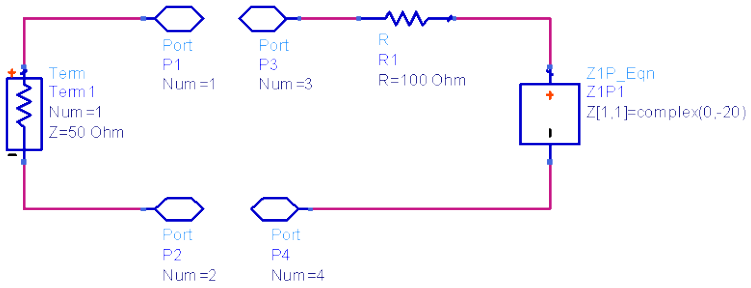

Figure 3. SEDZ Impedance Matching Schematic 1

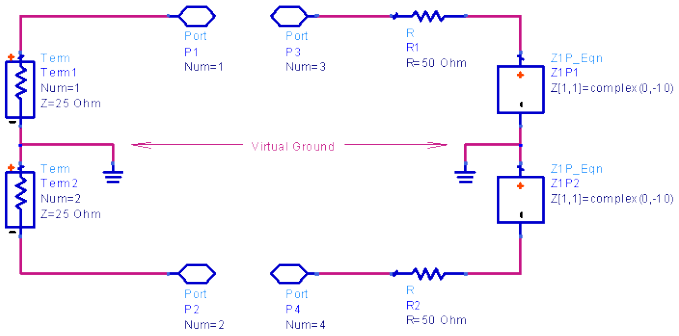

Figure 4. SEDZ Impedance Matching Schematic 2. Bisected network.

The overall matching network is a differential "T" type. See Figure 59.

Conclusions

1. The differential matching process is very straightforward.
2. Given this example, the "L" part of the matching network was designed with "shunt" Inductance and "series" Capacitance.

3. Starting with the SEDZ Load model, the resulting matching network is a “T” type.

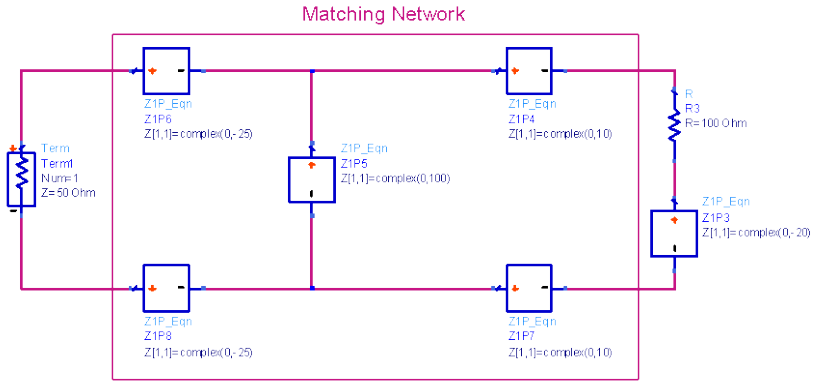

Figure 5. SEDZ Impedance Matching Schematic 3. The “T” Matching Network

Example 2: Matching to a 50 Ω Differential Source with a PEDZ Load Impedance Model. : Differential "L" Techniques

This example highlights the process to match a 50 Ω differential Source to a PEDZ modeled Load impedance of

104 // –J520 Ω. The impedance matching network would be installed between Ports 1, 2, 3, and 4. See Figure 60.

Compared to the SEDZ example, the only difference is the Load model "format" has changed. From an RF perspective, the Load functionality is the same. Similar to the SEDZ example, bisection of the system results in straightforward impedance matching element value calculations. The bisected schematic is shown in Figure 61.

This bisected network enables easy calculations for the matching component values. For simplicity, a differential "L" network will be designed. We only need to concentrate on the upper half of Figure 61.

1. By inspection, the first matching element value (traveling away from the load) is a shunt Inductance (+J260).
2. The next step is to calculate the "L" network required to match a pure 52 Ω Load to a pure 25 Ω Source.
3. A "shunt" matching element is always placed on the side (source or load) with the largest resistance. In this case, R_{large} is on the Load end. Calculate the Impedance Transformation Q.

$$Q_t = \text{sqrt}(R_{large}/R_{small} - 1) \quad (11)$$

$$Q_t = \text{sqrt}(52/25 - 1) = 1.0392$$

4. Calculate the "shunt" element matching reactance with Equation 42.

$$|X_{shunt}| = R_{large}/Q_t \quad (12)$$

$$|X_{shunt}| = 52/1.0392 = 50.0037\ \Omega$$

5. Calculate the "series" element matching reactance with Equation 43.

$$|X_{series}| = Q_t * R_{small} \quad (13)$$

$$|X_{series}| = 1.0392*25 = 25.98\ \Omega$$

6. At this point, we have the basics of the matching network calculated. However, we can simplify the "shunt" matching element value. There are 2 "shunt" values.

   Shunt Element Calculation 1 : +J260 : Resonate the Load Reactance.

   Shunt Element Calculation 2 : $|X_{shunt}| = 50.0037\ \Omega$: "L" Match element.

   These two elements are in parallel. They can be reduced down to 1 element. Since the first calculation yielded an Inductance, it is reasonable to select an Inductance for the second element. The total reactance is calculated with the standard formula for paralleled reactance.

$$X_t = JX_1 * JX_2 / (JX_1 + JX_2) \quad (14)$$

$$X_t = JX_1 * JX_2 / (JX_1 + JX_2) = (J260)*(J50.0037) / (J260 + J50.0037) = +J41.9381$$

   X_t is the revised X_{shunt} value.

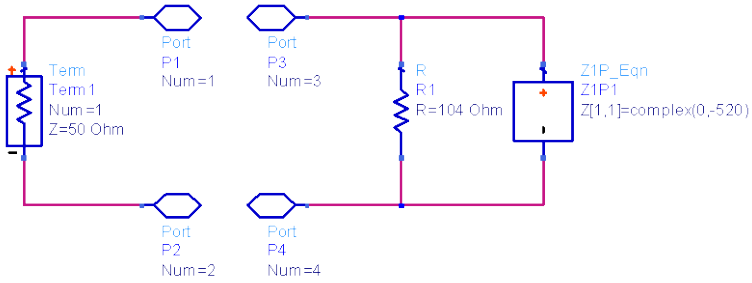

Figure 6. PEDZ Impedance Matching Schematic 4

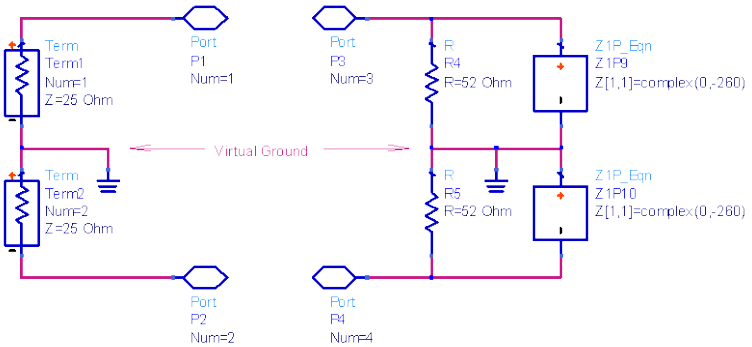

Figure 7. PEDZ Impedance Matching Schematic 5. Bisected network

4. Since the original system was bisected, the "shunt" matching reactance must be modified to work within a differential system. Equation 45 implements the conversion.

$$|X_{shunt\_diff}| = 2*|X_{shunt}| \quad (15)$$

$$|X_{shunt\_diff}| = 2*J41.9381 = 83.8762\ \Omega$$

Given the “shunt” and “series” reactance magnitudes, the only constraint is they must be opposite signs. If the “shunt” reactance is selected as inductive (+) then the “series” reactance must be capacitive (-). If the “shunt” reactance is selected as Capacitive (-) then the “series” reactance must be Inductive (+).

In this case, the “shunt” matching is an Inductance. Therefore, the “series” matching element must be a capacitance. The overall matching network is a differential “L” type. See Figure 62.

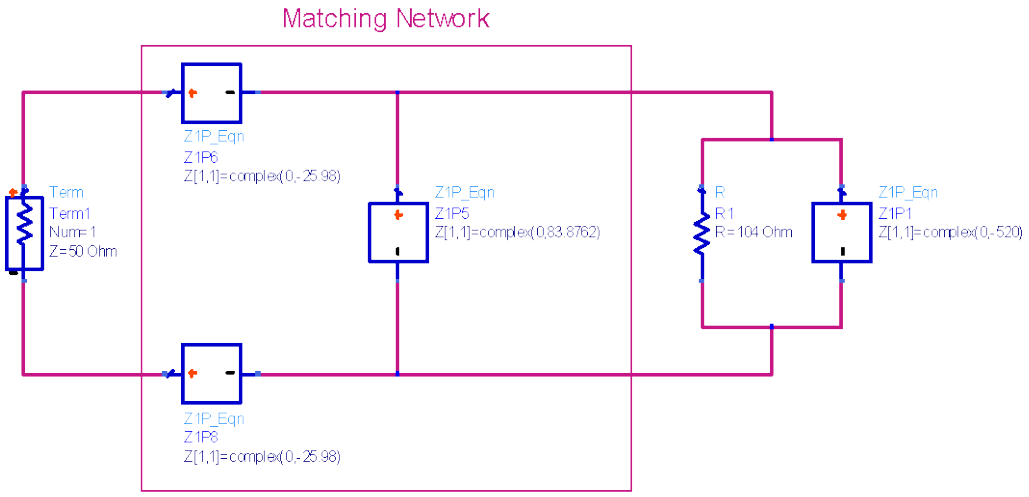

Figure 8. PEDZ Impedance Matching Schematic 6. The High-Pass Differential Matching Network

Example 3: Matching to a 50 Ω Differential Source with a PEDZ Load Impedance Model. : Differential "PII" Techniques

This example highlights the process to match a 50 Ω differential Source to a PEDZ modeled Load impedance of

104 //–J520 Ω. The impedance matching network would be installed between Ports 1, 2, 3, and 4. See Figure 63.

This matching exercise is very similar to Example 2 (Differential "L"). The only difference is a Differential "PII" network topology is utilized. A Differential "PII" network topology will have a minimum of 4 components.

The first step is to bisect the complete circuit. See Figure 64.

The Impedance Transformation "Q" for the "PII" network topology as follows.

$$Q_t = \text{sqrt}(R_{max}/R - 1) \quad (16)$$

Compared to the "L" matching network, the "PII" matching network Impedance transformation "Q" is variable. Varying the "R" term in equation 11 will modulate the Impedance Transformation Q. The lowest possible Impedance Transformation Q is desired for maximum Bandwidth and minimal component value tolerance issues.

The Impedance Transformation "Q" must be greater than 0. Therefore, the "R" value in Equation 61 must be less than both the Source Resistance and the Load Resistance.

$$R < R_{source} \quad (17)$$

$$R < R_{load} \quad (18)$$

Since the network is bisected, the R_{source} is 25 Ω and the R_{load} is 52 Ω. Assume a low Q solution is required.

Set R=24 Ω. Since R_{load} is higher than R_{source}, R_{load} is the high impedance side and R_{source} is the low impedance side.

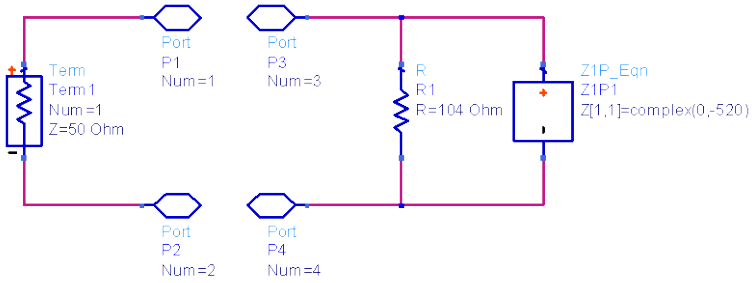

Figure 9. PEDZ Impedance Matching Schematic 7.

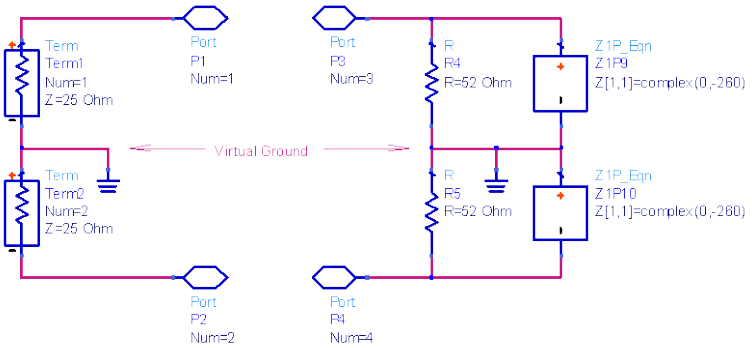

Figure 10. PEDZ Impedance Matching Schematic 8. Bisected network.

1. The high impedance side Transfomation Ratio is as follows.

   $Q_t = \text{sqrt}(R_{max\_high\_side}/R - 1)$ (19)

   $Q_t = \text{sqrt}(52/24 - 1) = 1.08$

2. Calculate the high impedance side preliminary "shunt" reactance value.

   $|X_{shunt\_high\_side}| = R_{large}/Q_t$ (20)

   $|X_{shunt\_high\_side}| = 52/1.08 = 48.14\ \Omega$

3. Calculate the high impedance side "series" (part 1) reactance value.

   $|X_{series\_high\_side}| = Q_t * R$ (21)

   $|X_{series\_high\_side}| = 1.08*24 = 25.92\ \Omega$

4. Calculate the low-impedance side Impedance Transformation Q.

   $Q_t = \text{sqrt}(R_{max\_low\_side}/R - 1)$ (22)

   $Q_t = \text{sqrt}(25/24 - 1) = 0.204$

5. Calculate the low-impedance side "shunt" reactance value.

   $|X_{shunt\_low\_side}| = R_{large}/Q_t$ (23)

   $|X_{shunt\_low\_side}| = 25/0.204 = 122.55\ \Omega$

6. Calculate the low-impedance side "series" (part 2) reactance value.

   $|X_{series\_low\_side}| = Q_t * R$ (24)

   $|X_{series\_low\_side}| = 0.204*24 = 4.90\ \Omega$

At this point, we have the basics of the matching network calculated. However, we can simplify the network. There are two constraints on the impedance matching network calculations.

- $\mathbf{X_{shunt\_high\_side}}$ reactance must be of the opposite sign compared to the $\mathbf{X_{series\_high\_side}}$ reactance.
- $\mathbf{X_{shunt\_low\_side}}$ reactance must be of the opposite sign compared to the $\mathbf{X_{series\_low\_side}}$ reactance.

Following the previous rules results in 4 possible PII network topologies.

- Low-Pass.
- High-Pass.
- Band-Pass 1.
- Band-Pass 2.

Similar to the "L" network examples, the initial component value calculations are based on real-only source and load termination values. These initial calculation results are then "normalized" to account for the source and load termination reactance values.

There are two ways to deal with the source and load reactive terminations.

- Utilize opposite sign matching reactance to resonate out the source and load reactance.
- Abosorb the source and load reactance into the overall matching network reactance values.

Low-Pass Simplification

A Low-Pass "PII" is made from "shunt" Capacitance and "series" Inductance.

The total "series" reactance includes two parts.

- Combine the $X_{series\_high\_side}$ and the $X_{series\_low\_side}$ reactances together. Use a (+) sign to denote a "series" Inductance.
- $Xseries\_total = X_{series\_high\_side} + X_{series\_low\_side} = +J25.92 + J4.90 = +J30.92.$ (25)

The total "shunt" reactance on the Load side includes multiple parts.

Based on the earlier calculations (real source and real load), the total high impedance side "shunt" reactance requirement is 48.14 Ω. This preliminary calculation must be normalized to account for the residual Load reactance.

Since the high-side "series" reactance sign is positive (+), the high-side "shunt" reactance sign must be negative(-). Therefore, the total high impedance side "shunt" reactance is –J48.14 Ω.

Normalization of the total high impedance side "shunt" reactance is accomplished in the susceptance domain.

$|X_{shunt\_high\_side\_norm}| = 1 / ((1/ X_{shunt\_high\_side}) - (1/X_{load}))$ (26)

$|X_{shunt\_high\_side\_norm}| = 1 / ((1/ -J48.14) - (1/-J260)) = -J59.08\ \Omega.$

Since the Differential system was bisected for these calculations, the final Load side "shunt" reactance must be normalized.

$|X_{load\_side\_shunt\_diff}| = 2*|X_{shunt\_high\_side\_norm}|$ (27)

$|X_{load\_side\_shunt\_diff}| = 2*(-J59.08) = -J118.16\ \Omega$

Since the Source termination is only real, the total Source side reactance calculation is straightforward. The reactance was calculated earlier.

$|X_{shunt\_low\_side}| = 25/0.204 = 122.55\ \Omega$ (28)

The selected low impedance side "series" reactance is Inductive. Therefore, we must set the sign for the low impedance side "shunt" reactance to a minus (-).

Since the Differential system was bisected for these calculations, the final Load side "Shunt" Reactance must be normalized.

$|X_{source\_side\_shunt\_diff}| = 2*|X_{shunt\_low\_side}|$ (29)

$|X_{source\_side\_shunt\_diff}| = 2*(-J122.55) = -J245.10\ \Omega$

The final Low-Pass Differential "PII" matching network is shown in Figure 65.

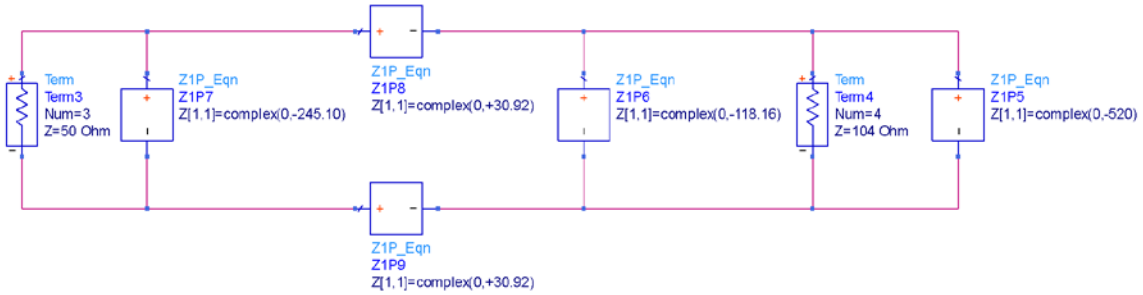

Figure 11. PEDZ Impedance Matching Schematic 9. The Low-Pass Differential "PII" Matching Network.

High Pass Simplification

A High-Pass "PII" is made from "shunt" Inductance and "series" Capacitance.

The total "series" reactance includes two parts.

- Combine the $X_{series\_high\_side}$ and the $X_{series\_low\_side}$ reactances together. Use a (-) sign to denote a "series" Capacitance.
- Xseries_total = $X_{series\_high\_side}$ + $X_{series\_low\_side}$ = -J25.92 + (-J4.90) = -J30.92. (30)

The total "shunt" reactance on the Load side includes multiple parts.

Since the "series" reactance is selected as negative (-), the "shunt" reactance must be positive(+).

The first step is to resonate the Load reactance. The bisected Load reactance is –J260. Therfore, the first Load side "shunt" component reactance is +J260.

Based on the earlier calculations (real source & real load), the total high impedance side "shunt" reactance requirement is 48.14 Ω. This preliminary calculation must be normalized to account for the residual Load reactance.

These two elements are in parallel. They can be reduced down to 1 element. Since the first calculation yielded an Inductance, it is reasonable to select an Inductance for the second element.

The total reactance is calculated with the standard formula for paralleled reactance.

$$X_{shunt\_high\_side\_norm} = (JX_1 * JX_2) / (JX_1 + JX_2) \quad (31)$$

$$X_{shunt\_high\_side\_norm} = (JX_1 * JX_2) / (JX_1 + JX_2) = (J260)*(J48.14) / (J260 + J48.14) = +J40.62$$

Since the Differential system was bisected for these calculations, the final Load side "shunt" reactance must be normalized.

$$|X_{load\_side\_shunt\_diff}| = 2*|X_t| \quad (32)$$

$$|X_{load\_side\_shunt\_diff}| = 2*(+J40.62) = +J81.24\ \Omega$$

Since the Source termination is only real, the total Source side reactance calculation is straightforward. The reactance was calculated earlier.

$$|X_{shunt\_low\_side}| = 25/0.204 = 122.55\ \Omega \quad (33)$$

The selected low impedance side "series" reactance is Capacitive. Therefore, we must set the sign for the low impedance side "shunt" reactance to a positive (+).

Since the Differential system was bisected for these calculations, the final Load side "Shunt" Reactance must be normalized.

$$|X_{source\_side\_shunt\_diff}| = 2*|X_{shunt\_low\_side}| \quad (34)$$

$$|X_{source\_side\_shunt\_diff}| = 2*(+J122.55) = +J245.10\ \Omega$$

The final High-Pass Differential "PII" matching network is shown in Figure 66.

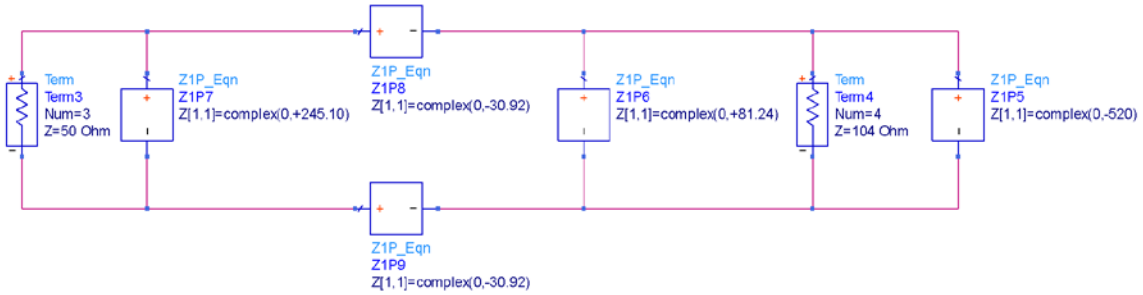

Figure 12. PEDZ Impedance Matching Schematic 10. The High-Pass Differential "PII" Matching Network.

Band-Pass 1 Simplification

A Band-Pass "PII" topology is developed by selecting opposite sign "series reactances. For this example, the low impedance side "series" reactance is positive (+) and the high impedance side "series" reactance is negative.

The preliminary calculations resulted in the following "series" reactance values.

$$|X_{series\_high\_side}| = 1.08*24 = 25.92\ \Omega \quad (35)$$

$$|X_{series\_low\_side}| = 0.204*24 = 4.90\ \Omega \quad (36)$$

For this example, the following reactance signs are utilized.

$$X_{series\_high\_side} = -J25.92\ \Omega$$

$$X_{series\_low\_side} = +J4.90\ \Omega$$

The total "shunt" reactance on the Load (high impedance side) includes multiple parts.

Since the "series" reactance is selected as negative (-), the "shunt" reactance must be positive(+).

The first step is to resonate the Load reactance. The bisected Load reactance is –J260. Therfore, the first Load side "shunt" component reactance is +J260.

Based on the earlier calculations (real source and real load), the total high impedance side "shunt" reactance requirement is 48.14 Ω. This preliminary calculation must be normalized to account for the residual Load reactance.

These two elements are in parallel. They can be reduced down to 1 element. Since the first calculation yielded an Inductance, it is reasonable to select an Inductance for the second element. The total reactance is calculated with the standard formula for paralleled reactance.

$$X_{shunt\_high\_side\_norm} = (JX_1 * JX_2) / (JX_1 + JX_2) \quad (37)$$

$$X_{shunt\_high\_side\_norm} = (JX_1 * JX_2) / (JX_1 + JX_2) = (J260)*(J48.14) / (J260 + J48.14) = +J40.62$$

Since the Differential system was bisected for these calculations, the final Load side "shunt" reactance must be normalized.

$$|X_{load\_side\_shunt\_diff}| = 2*|X_t| \quad (38)$$

$$|X_{load\_side\_shunt\_diff}| = 2*(+J40.62) = +J81.24\ \Omega$$

Since the Source termination is only real, the total Source side reactance calculation is straightforward. The reactance was calculated earlier.

$$|X_{shunt\_low\_side}| = 25/0.204 = 122.55\ \Omega \quad (39)$$

The selected low impedance side "series" reactance is Inductive. Therefore, we must set the sign for the low impedance side "shunt" reactance to a minus (-).

Since the Differential system was bisected for these calculations, the final Load side "shunt" Reactance must be normalized.

$$|X_{source\_side\_shunt\_diff}| = 2*|X_{shunt\_low\_side}| \quad (40)$$

$$|X_{source\_side\_shunt\_diff}| = 2*(-J122.55) = -J245.10\ \Omega$$

The final Band-Pass 1 Differential "PII" matching network is shown in Figure 67.

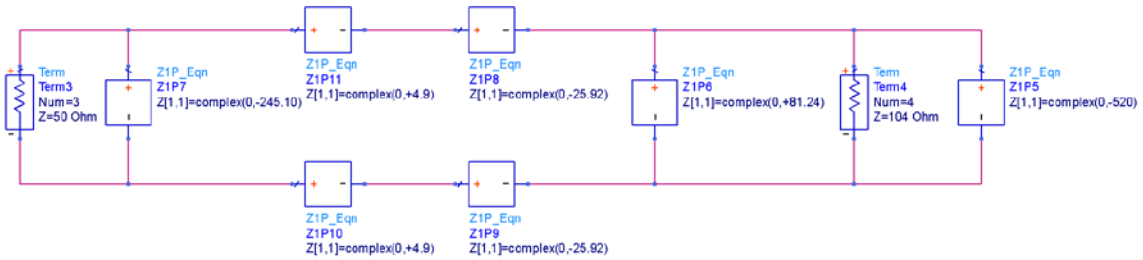

Figure 13. PEDZ Impedance Matching Schematic 11. The Band-Pass 1 Differential "PII" Matching Network.

Band-Pass 2 Simplification

The Band-Pass 2 option is very similar to the Band-Pass 1 option.

A Band-Pass "PII" topology is developed by selecting opposite sign "series reactances. For this example, the low impedance side "series" reactance is negative (-) and the high impedance side "series" reactance is positive (+).

The preliminary calculations resulted in the following "series" reactance values.

$$|X_{series\_high\_side}| = 1.08*24 = 25.92\ \Omega \quad (41)$$

$$|X_{series\_low\_side}| = 0.204*24 = 4.90\ \Omega \quad (42)$$

For this example, the following reactance signs are utilized.

$X_{series\_high\_side} = +J25.92\ \Omega$

$X_{series\_low\_side} = -J4.90\ \Omega$

The total "shunt" reactance on the Load side includes multiple parts.

Based on the earlier calculations (real source and real load), the total high impedance side "shunt" reactance requirement is 48.14 Ω. This preliminary calculation must be normalized to account for the residual Load reactance.

Since the high-side "series" reactance sign is positive (+), the high-side "shunt" reactance sign must be negative(-). Therfore, the total high impedance side "shunt" reactance is –J48.14 Ω.

Normalization of the total high impedance side "shunt" reactance is accomplished in the susceptance domain.

$$|X_{shunt\_high\_side\_norm}| = 1 / ((1/ X_{shunt\_high\_side}) - (1/X_{load})) \quad (43)$$

$|X_{shunt\_high\_side\_norm}| = 1 / ((1/ -J48.14) - (1/-J260)) = -J59.08\ \Omega$.

Since the Differential system was bisected for these calculations, the final Load side "shunt" reactance must be normalized.

$$|X_{load\_side\_shunt\_diff}|=2*|X_{shunt\_high\_side\_norm}| \quad (44)$$

$|X_{load\_side\_shunt\_diff}|=2*(-J59.08) = -J118.16\ \Omega$

Since the Source termination is only real, the total Source side reactance calculation is straightforward. The reactance was calculated earlier.

$$|X_{shunt\_low\_side}|= 25/0.204 = 122.55\ \Omega \quad (45)$$

The selected low impedance side "series" reactance is Capacitive. Therefore, we must set the sign for the low impedance side "shunt" reactance to a positive (+).

Since the Differential system was bisected for these calculations, the final Load side "Shunt" Reactance must be normalized.

$$|X_{source\_side\_shunt\_diff}|=2*|X_{shunt\_low\_side}| \quad (46)$$

$|X_{source\_side\_shunt\_diff}|=2*(+J122.55) = +J245.10\ \Omega$

The final Band-Pass 2 Differential "PII" matching network is shown in Figure 68.

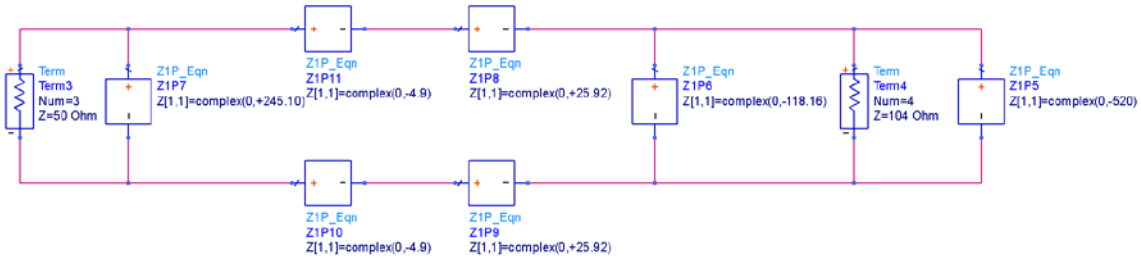

Figure 14. PEDZ Impedance Matching Schematic 12. The Band-Pass 2 Differential "PII" Matching Network.

Impedance Modeling/Matching Conclusions

- The differential matching process is very straightforward.
- The most important point is to recognize the format (SEDZ or PEDZ) of the Load and/or Source impedance data.
- Given an RX system, the Load is the 9361 LNA input impedance.
- Given a TX system, the Source is the 9361 Buffer output impedance.
- RX LNA input Noise Figure (NF) "Gamma-Opt" effects and TX Buffer Output "Load-Pull" effects are not part of this analysis.
  - The intent is to highlight "basic" matching techniques. A good starting point for any matching exercise.
  - To date, the 9361 has not exhibited significant Noise Figure "Gamma-Opt" effects.
  - The RX LNA Noise Figure "gamma-Opt" represents the change in Noise Figure as a function of the Driving-Source Impedance.
    - RX systems without a significant Noise Figure "Gamma-Opt" may be impedance matched by optimizing just the Transducer Gain (TG) through the system.
    - RX systems with a significant Noise Figure "Gamma Opt" affect, may be optimized by trading off the TG performance for the best(lowest Noise Figure) Driving-Source Impedance.
    - The TX Output "Load-Pull" represents the power delivered as a function of Load Impedance.
  - The TX Output "Load-Pull" represents the change in Power Delivered as a function of Load impedance.
    - TX systems without significant Load-Pull affects may be impedance matched by optimizing just the Transducer Gain (TG) through the system.
    - TX systems with significant Load-Pull affects, may be optimized by trading off the TG performance for the best(maximum delivered power) Load Impedance.
- The hand calculations are good for 1st pass matching option analysis. Given matching over wide RF Bandwidths, CAD based matching techniques are much more accurate and time efficient.

CAD (Computer Aided Design) Matching: General Overview

The simpler "by hand" calculation approach will result in the quickest development of potential impedance matching solutions. CAD based matching techniques will provide the most accurate "theoretical" impedance matching solutions. The preferred approach is to use both. The "by hand" methods can quickly find a wide range of impedance matching topology options. The CAD techniques can refine this range of options into the top two or three impedance matching candidates. The goal is to "theoretically" design a matching network where the component values are within +/- 1 standard value compared to the lab based empirically (cycle-tuned) derived component values.

There are many references within this section to the Agilent ADS CAD package. Any CAD package with similar functionality is a reasonable substitution.

The following models are required to build a CAD based impedance matching simulation.

- RX Path Model Requirements:
  - Source Impedance vs. Frequency : Usually 50 Ω for a conducted-only simulation.
  - Board Artwork Model (N-Port "S" Matrix) from the Source Termination to the Load Termination.
  - Lumped Element Component Models : R, L, and C.
  - Balun / Filter "S" parameter Models.
  - Load Impedance vs. Frequency : The LNA Input Impedance Model.
    - LNA Noise-Figure Gamma-Opt effects (if present) are not yet included.
- TX Path Model Requirements:
  - Source Impedance vs. Frequency : The TX Buffer Output Impedance Model.
    - TX Buffer "Load-Pull" effects (if present) are not yet included.
  - Board Artwork Model (N-Port "S" Matrix) from the Source Termination to the Load Termination.
  - Lumped Element Component Models : R, L, and C.
  - Balun / Filter "S" Parameter Models.
  - Load Impedance vs. Frequency : Usually 50 Ω for a conducted-only simulation.

CAD Based Impedance Matching : System Example

One CAD modeling example is included within this section. This "RX Path" model is based on "power" matching. In other words, the system is designed to transfer the most amount of power from the Source to the Load.

Step 1

Create a model of the board artwork. Electro-Magnetic (E&M) simulation is the best approach. Analog Devices has utilized the ADS Momentum E&M simulator to successfully model boards.

E&M Simulation Set-Up Hints:

- Directly import the board Gerbers into the E&M tool.

- Set the #Cells/Wavelength at the highest simulation frequency to >= 90.
- Set realistic dielectric and metal parameters.
- Simulate the “local” area of interest. There is no need to simulate the whole board.
- Simulate only the active board layers. Simulate between the Top or Bottom Layer and the associated Reference-Ground Layer.
- Set-Up RF Ports for the system Input, Output, Ground, and each SMD component pad.
- Each RF Port should be associated with a close-proximity Ground Reference Port. The Ground Reference Ports should be placed on the Reference-Ground Layer.

Figure 69 is a cropped view of a 9361 Evaluation PWB. A board artwork example.

9361 Ball Pads : Yellow oval areas.

Balun / Filter Pads : Green rectangular areas.

A TX Path is on the left. An RX path is on the right. The path physical length is quite different!

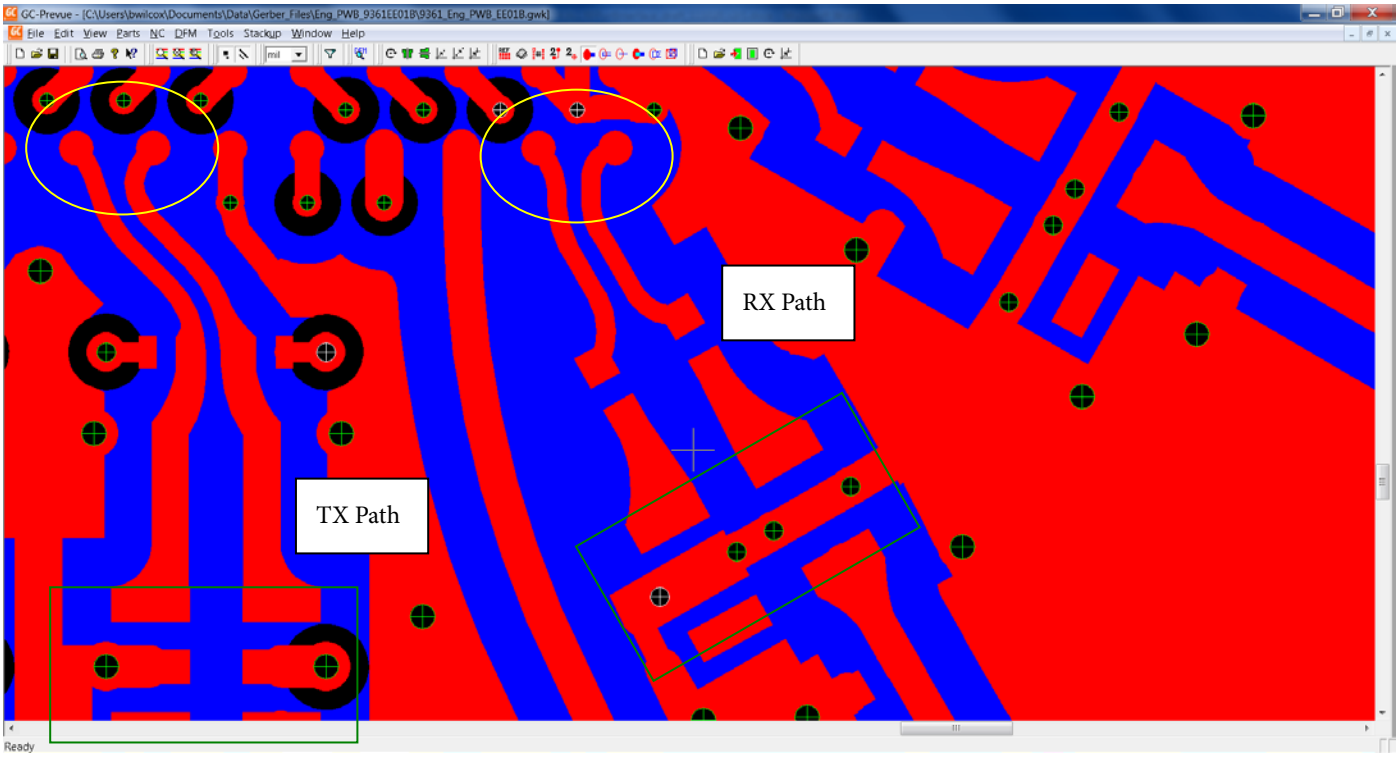

Figure 15.Artwork Example

The most important point to note is the Balun/Filter reference-plane is quite different when compared to the actual 9361 Ball Pad reference plane.

The result is the differential impedance seen at the Balun/Filter port may be quite different when compared to the published 9361 port impedance data. Utilizing an E&M simulation to model the artwork will not only help to design matching networks, but also help to select the Baluns/Filters that integrate well into the system.

For example, assume the 9361 RX Port Impedance is 200 Ω at the Ball Pad reference-plane. Further assume that the board has translated the 200 Ω impedance at the Ball Pad reference plane to 100 Ω at the Balun/Filter reference-plane. It makes good sense to select a 2:1 (100 to 50) Balun/Filter as opposed to a 4:1 (200 to 50) Balun/Filter. The optimum Balun/Filter selection (impedance viewpoint) is a function of the board layout design. In particular, the RF line impedance and the RF line electrical length.

Of course, shorter RF differential line systems exhibit less impedance transformation when compared to longer differential line systems. If easier impedance matching is the goal, shorter RF lines are desired.

The main conclusion is E&M simulation of a "local" board area is fundamental to the goal of achieving the best possible system performance. Both from an impedance matching development perspective and a component selection perspective.

It is possible to simulate the board layout with non E&M based techniques. However, all of the coupling mechanisms within the layout would not be fully captured. Less accurate simulation results would be expected.

Step 2

Create a model of the LNA Input Port.

Note that:

- Analog Devices can supply "S" data for the LNA Input ports as measured on the Analog Devices Evaluation Platform. Contact Analog Devices and request the "S" data. Indicate if the 9361 is set-up in a "single-ended" mode or a "differential" mode. Follow steps 3 though 5 in this section to build the LNA Input Impedance model.
- If the end user application artwork is significantly different when compared to the Analog Devices Evaluation Platform, it may be a good idea(simulation accuracy viewpoint) to measure the LNA Input Impedance when the 9361 is mounted on the end user board. Then, follow steps 1 through 5 within this section to build the LNA Input Impedance model.

There are many methods associated with "Black-Box" modeling of a Differential LNA Input Port. The selected method is based on a "center-tapped" transformer methodology. The overall process is as follows.

1. Measure the LNA Input Port 2-Port "S" matrix. The VNA power should be <= -30 dBm .
2. Convert the measured and de-embedded 2-Port "S" matrix to a 1-Port "S" matrix.
3. Utilize a DAC (data access component) to "read" the 1-Port "S" matrix into the system simulator.
4. Port the data from the DAC "read" to the System Simulation LNA termination port.
5. Utilize a 1:1 "center-tapped" transformer to transition from a single-ended system to a differential system.

Figure 70 is an ADS schematic of the LNA Input Impedance model.

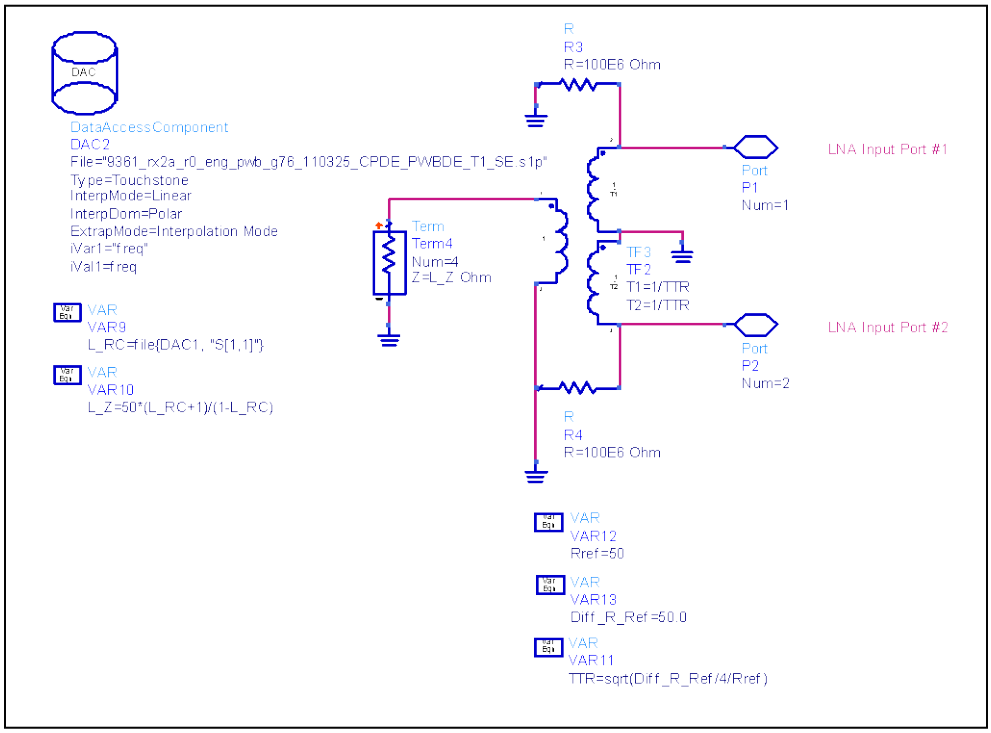

Figure 16. LNA Model Example

LNA Model Operation Highlights

- The DAC (Data Access Component) is utilized to read the 1-port format differential impedance into the L_Z variable. This impedance is calculated from the 2-Port LNA Input "S" matrix.
- The L_Z variable terminates the transformer common-mode port.
- The 1:1 transformer is used to convert the 1-port differential impedance into the 2-port equivalent.
- The 2-port impedance includes the differential impedance across the ports and both common mode impedances.
- This model not only allows for proper port impedance termination but also Gain/Loss analysis from an Input Port to the Output Port.
- Common-mode return currents are resolved by the transformer "center-tap" (grounded). These currents are created by Amplitude-Balance and Phase-Balance errors.

Note that a single-ended mode LNA Input Impedance model does not require the center-tapped transformer. However, a DAC component is utilized to read the single-ended mode LNA Input Impedance Data into the L_Z variable.

Step 3

Create Lumped Element models.

Inductors, Capacitors, and sometimes resistors (zero Ω thru) are utilized in matching networks. Accurate models of these components are critical to accurate simulation output data.

Resistors in matching networks are usually reserved for low-loss series "thru" elements. The best approach to modeling these devices is to measure and de-embed the 2-Port "S" matrix. Utilize this 2-port "S" matrix within the system simulations.

Capacitors are best modeled with a LEE (Lumped Element Equivalent) approach. 2-Port "S" data is taken on a range of capacitance values and the data is utilized in fitting a LEE model to the measured and de-embedded "S" data. A simple LEE capacitance model is shown in Figure 71.

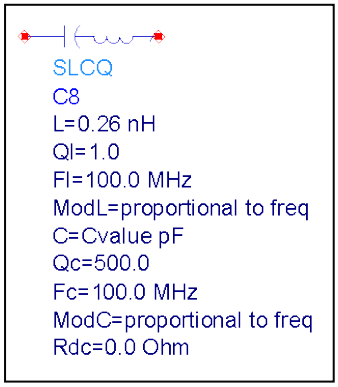

Figure 17. LEE Capacitor Model Example

This simple LEE Capacitor Model includes : Parasitic Inductance, ESR, Dielectric Q, and the Capacitance Value. More complicated LEE Capacitance Models are built with DAC functions. DAC functions allow parameter value look-up as a function of the Capacitance Value. This is useful for cases where the capacitor parasitics are a function of the capacitance value.

Inductors are also best modeled with a LEE approach. An example Inductor Model is shown in Figure 72.

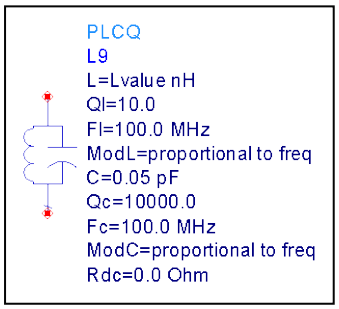

Figure 18. LEE Inductor Model Example

This simple LEE Inductor Model includes : Parasitic Capacitance, ESR, Q, and the Inductance Value. More complicated LEE Inductance Models are built with DAC functions. DAC functions allow parameter value look-up as a function of the Inductance Value. This is useful for cases where the inductor parasitics are a function of the inductance value.

Note that:

- These simple LEE Models work well for SMD Multi-Layer Ceramic Capacitors (NPO) and SMD Multi-Layer (thin or thick film) Inductors. Wire-Wound SMA Inductors require a slightly more complicated model.
- It is best to characterize the SMD components (RLC) when installed in the application environment. Not the vendor test fixture. Ground plane proximity and other unintentional coupling mechanisms may change the intrinsic behavior of the device.
  - If possible, design and build a test fixture to measure these devices. This fixture would have the same board stack-up, board materials, and Pad sizes as the actual application environment.
- At higher (> 800 Mhz) frequencies, the Solder associated with the component mounting significantly effects the device performance. Capturing this effect within the LEE models will result in lower simulation to measurement error. The goal is to simulate lumped element component values to within +/- 1 standard value of what is determined in the lab. Not accounting for these solder effects may result in substantial simulated component value error. High-Q systems are much more sensitive to modeling errors when compared to Low-Q systems. Do not settle for non-soldered device data.

Step 4

Create Balun / Filter "S" Data Models.

Accurate modeling of these devices is critical to simulation accuracy. There are two general approaches.

- Obtain "S" data from the vendor.
- Measure the "S" data utilizing a fixture that is very similar to the actual applications environment.

Be careful with vendor supplied data! In some cases, the vendors "match" the devices and include the effects of the external matching components within the "S" matrix that is delivered to their customers. For accurate system level simulations, the "S" matrix of just the Balun / Filter is required. The optimum external matching component values will be determined with the system simulations and lab based fine tuning. Ask for "S" data for just the device.

Make sure the vendor supplied data accounts for the following:

- Solder effects.
- The raw measurement data has been de-embedded to the device pad solder connection reference plane . The test fixture connectors, rf lines, and pads have been de-embedded.

"Local" measurements of a Balun / Filter is the best approach. Make sure the ground is very low resistance / inductance. Poor grounding is one way to destroy the "S" data accuracy.

Step 5

Build the System Simulation.

Figure 73 represents the "RF Connections" associated with the system simulation.

The RF Power flows from Port 1, through the network to Port 2. Port 1 is defined as a broad-band 50 Ω termination. Port 2 is defined (DAC and Equations) as the LNA Input Port differential impedance. Port 2 is terminated with the actual LNA Input Port impedance vs. frequency.

L1 and C1 represent 0201 size lumped element SMD models. In this case, they are both multi-layer type devices. Very typical for TDK and Murata.

The "Board_Model" 11-Port "S" matrix represents the board artwork E&M simulation output data. All points within the RF System where power either enters or exists have an associated port.

The 3-Port "S" matrix is a Murata Saw filter. The "S" data only represents the device. The Saw filter ground reference reports into the "Board_Model" as opposed to simulation ground. The "Board_Model" was developed with a Saw filter Ground Pad Port. This is important because the filter is terminated in a non-ideal ground as opposed to an ideal simulation ground. The end result is a much more realistic simulation of the Saw filter when installed in the application RF environment.

The system model simulation has two modes. See Figure 73.

- High Frequency Resolution "S" Parameter Simulation. The "SP1" controller.
- Narrow Frequency Range High Resolution Component Optimization Simulation. The "SP2" controller.

Figure 74 highlights a mode 2 (Optimization) example simulation control set-up.

The simulation control defined in Figure 73/Figure 74 is set-up for "Optimization Mode". The system "dB(S21)" is optimized for minimum loss. C1 and L1 are the "optimized" matching component values. Example simulation results highlighted by Figure 75.

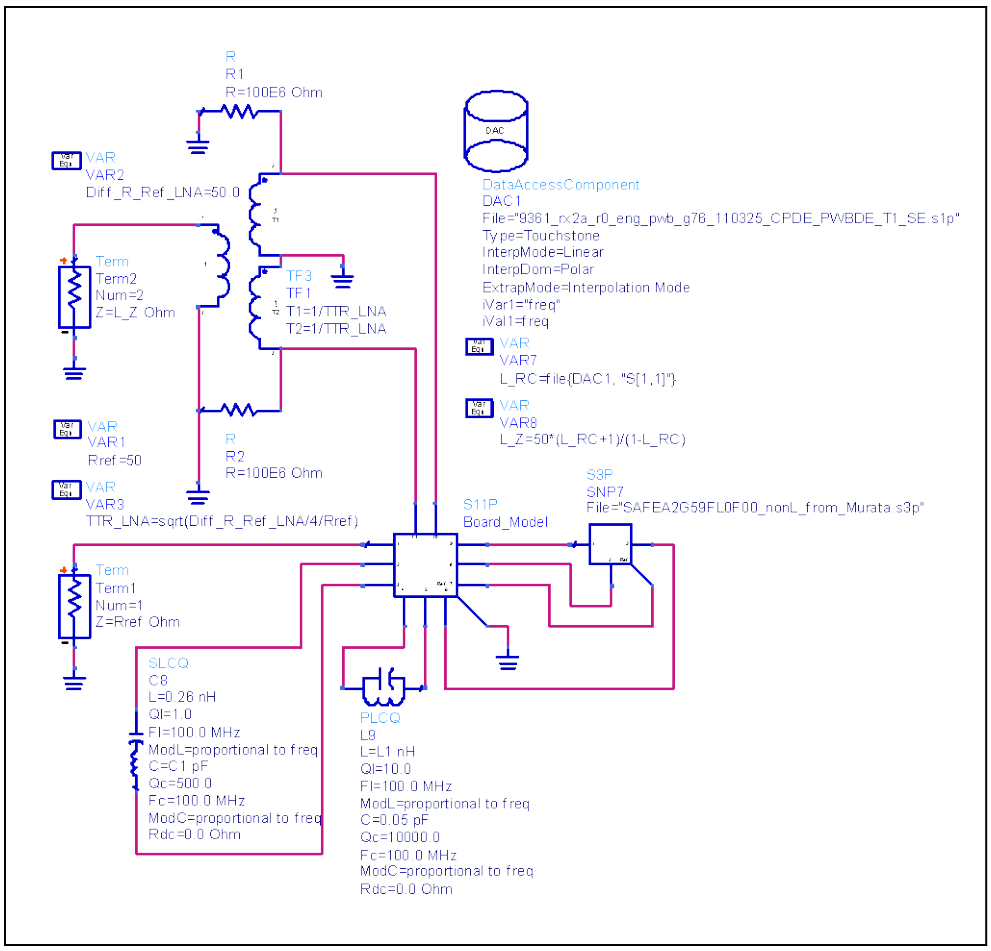

Figure 19. System Simulation Model Example – RF Connections.

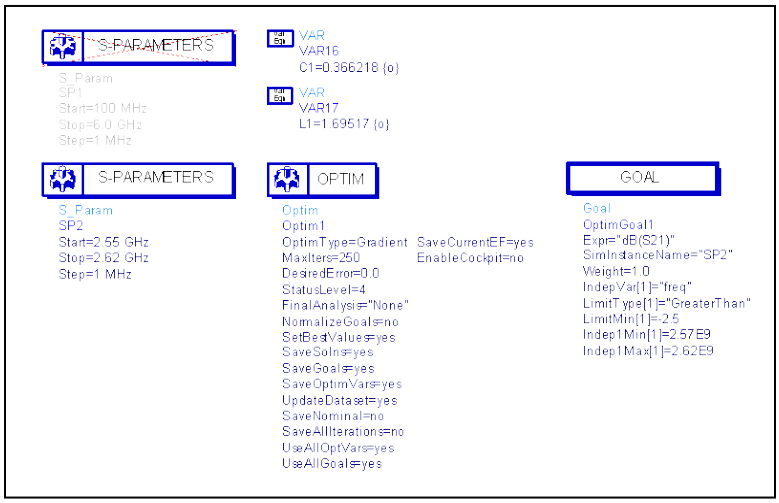

Figure 20. System Simulation Model Example – Control.

Note that:

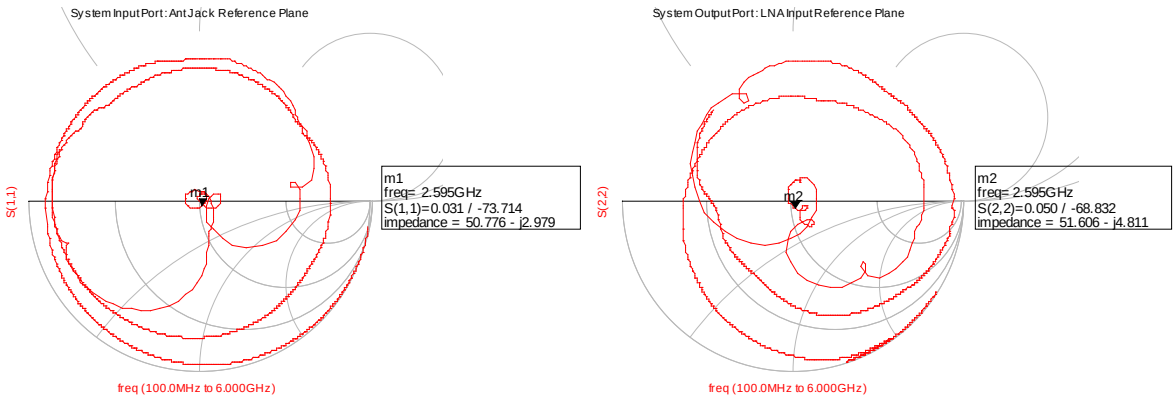

Figure 21. System Simulation Results – Post Optimization Port Reflection Coefficients.

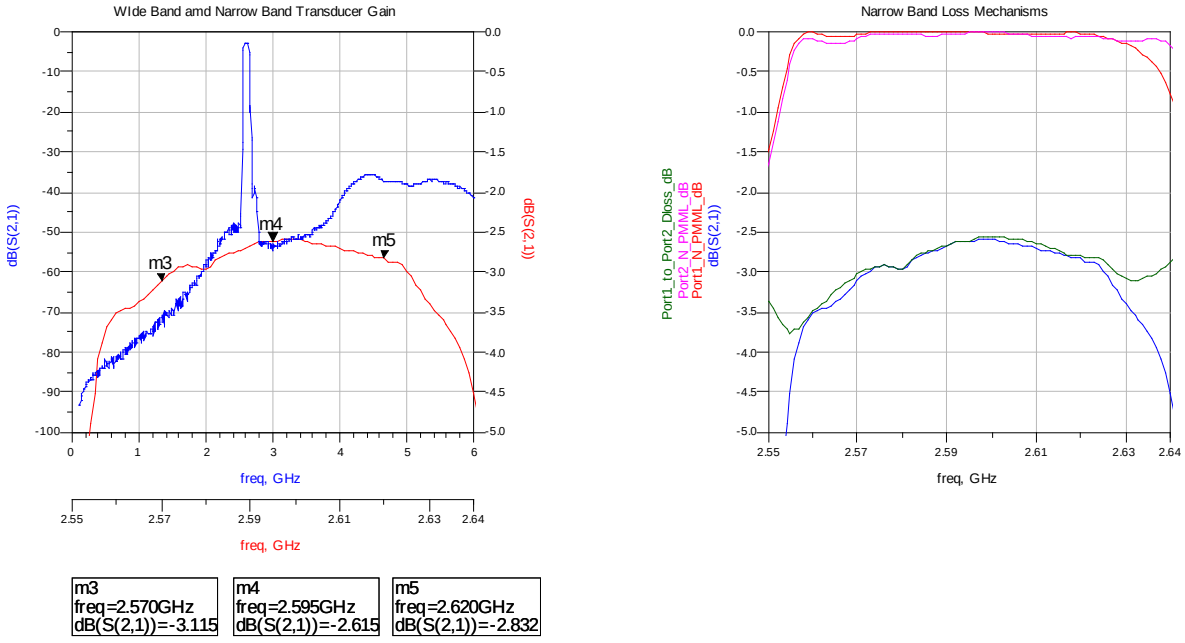

Figure 22. System Simulation Results – Post Optimization Port Reflection Coefficients.

The RF Ports are well matched and the overall Transducer Gain is dominated by the “dissipative” (Dloss) mechanism.

BOARD LAYOUT DESIGN SUGGESTION

The RF Line systems between the 9361 Ball-Pad reference-plane and the Balun / Filter reference plane should be designed for a Differential Impedance (Z_{diff}) of 100 Ω for the RX and **50** Ω for the TX.

This is a compromise impedance with respect to the 9361 frequency range. A good design starting point. The Z_{diff} can be optimized to fit a narrower frequency range. It is desirable to design the lines for reasonable coupling (-10 dB to -20 dB). This will promote decent EMI suppression performance.

The "high-level" differential line design equations are as follows

Z_{diff} = 100 Ω: Line System Differential Impedance Goal

$Z_{odd} = Z_{diff} / 2$ = 50 Ω: Line System Odd Mode Impedance

$Z_o = \text{sqrt}(Z_{even} * Z_{odd})$: Line System Characteristic Impedance

$C_{UL} = \text{sqrt}(Dk) / (Z_o * C)$: Line System Capacitance per Unit Length

$L_{UL} = (Z_o * \text{sqrt}(Dk)) / C$: Line System Inductance per Unit Length

$Z_o = \text{sqrt}(L_{UL} / C_{UL})$; Line Characteristic Impedance – Calculation Checking

where:
Dk is Media Relative Dielectric Constant.
C is Speed of Light (example : 1.1803E13 mil/s)

The Z_{even} parameter is a function of the line coupling. As the line coupling increases, both the Z_{even} and associated Z_o increase. Given the 9361 Ball Pad diameter (14 mil) and pitch (315 mil), Coupled MicroStrip differential lines are a preferred design choice.

Table 1. Example Differential MicroStrip #1 : Z_{diff} = 100 Ω

Can you provide a title for this column?	Ditto
Line Width: 10.25 mil	Z_{diff} = 98.92 Ω
Line Spacing: 7 mil	Z_{odd} = 49.46 Ω
Dielectric Height: 10 mil	Z_{even} = 78.62 Ω
Relative Dielectric Constant: 4.5	Z_o = 62.36 Ω
Dielectric Loss Tangent: 0.025	C_{UL} = 2.883 fF/mil
Metal Conductivity: 4.1E7 Siemens	L_{UL} = 11.21 pH/mil
Metal Thickness: 1.34 mil (1 oz)	Line Coupling = -12.85 dB

Table 2. Example Differential MicroStrip #2 : Z_{diff} = 100 Ω

Line Width: 14.00 mil	Z_{diff} = 99.88 Ω
Line Spacing: 14.75 mil	Z_{odd} = 49.94 Ω
Dielectric Height: 10 mil	Z_{even} = 62.1 Ω
Relative Dielectric Constant: 4.5	Z_o = 55.69 Ω
Dielectric Loss Tangent: 0.025	C_{UL} = 3.228 fF/mil
Metal Conductivity: 4.1E7 Siemens	L_{UL} = 10.010 pH/ml
Metal Thickness: 1.34 mil (1 oz)	Line Coupling = -19.29 dB

Table 3. Example Differential MicroStrip #2 : Z_{diff} = 50 Ω

Line Width: 35.00 mil	Z_{diff} = 50.62 Ω
Line Spacing: 4.00 mil	Z_{odd} = 25.31 Ω
Dielectric Height: 10 mil	Z_{even} = 62.1 Ω
Relative Dielectric Constant: 4.5	Z_o = 37.62 Ω

Dielectric Loss Tangent: 0.025	C_{UL} = 4.777 fF/mil
Metal Conductivity: 4.1E7 Siemens	L_{UL} = 6.761 pH/mil
Metal Thickness: 1.34 mil (1 oz)	Line Coupling = -14.47 dB

As seen within Table 79 to Table 81, many design trade-offs exist. Highly coupled lines require less physical space and exhibit better EMI suppression. However, the expected manufacturing tolerance is worse.

The best line design is one the fits the overall design goals for the end product. These designs are just illustrative examples.

The differential line design may be implemented in 2 phases. During the first phase a tool similar to the ADS LineCalc is utilized to balance the line physical requirements (size, tolerance) against the impedance and coupling goals. Phase 2 would involve E&M simulating the differential line system and then “fine” tuning the line width and spacing.