BIST SIGNAL GENERATOR

The AD9361 has an internal signal generator which can be used to inject a signal into either the output of the Tx data port or the input of the Rx data port. This is useful when testing the connectivity of the Rx data port or the Tx RF output. It is useful tool when debugging effects in the Tx chain of the AD9361. It allows the user to rule out the Tx data port as the source of issues, as it allows the user to generate a signal and inject it at the output of the Tx data port.

The BIST Signal generator is enabled by setting 0x3F4[D0] high. The injection point is chosen by programming bits 0x3F4 according to Table 1.

0x3F4[D3:D2]	Injection Point	"Clk" used for BIST Tone Frequency	Comments
00	Input of Tx (output of Data Port)	Tx Sample Rate	Tx Only
01	Not Used	N/A	N/A
10	Input of Data Port	Rx Sample Rate	Rx Only
11	Not Used	N/A	N/A

Table 1: BIST Injection Point.

Figure shows a graphical representation of Table 1.

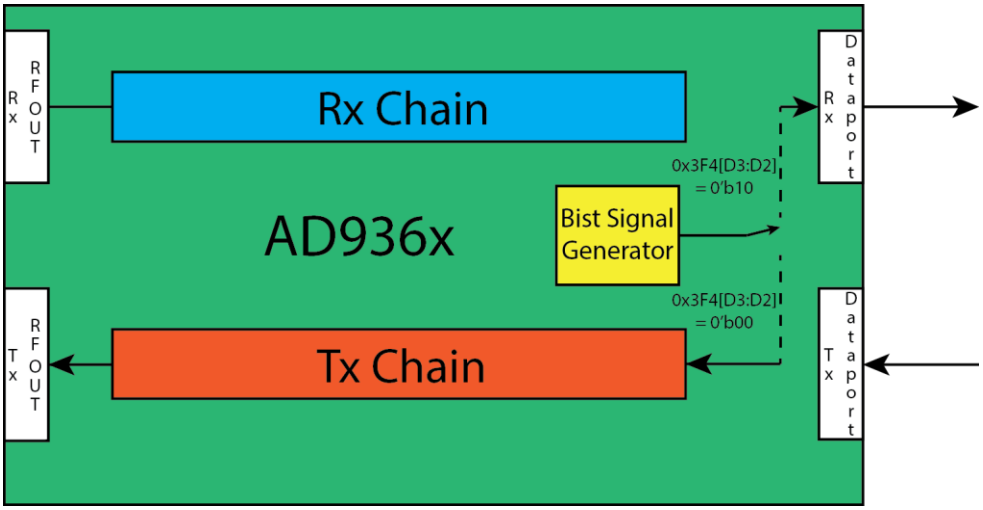

Figure 1: BIST Signal Generator Injection Points.

The BIST Signal Generator can output either a tone or a Pseudo-Random Bit Sequence (PRBS). The output is controlled with bit 0x3F4[D1].

0x3F4[D1]	Output
0	PRBS
1	Tone

Table 2: BIST Signal Generator Output Selection.

If a tone is selected there are two parameters that can be controlled. These are the frequency and the amplitude. The frequency of the tone is controlled by bits 0x3F4[D7:D6]. Equation 1 relates the numerical value of these bits to the frequency of the BIST Tone generated.

$$\boldsymbol{BIST\ Tone\ Frequency} = \frac{\boldsymbol{Clk} * (0x3F4[D7:D6] + \mathbf{1})}{\mathbf{32}}$$

Equation 1

where "Clk" is the frequency of the clock noted in column 3 of Table 1: BIST Injection Point.

The amplitude of the tone level is set using bits 0x3F4[D5:D4]. It is set as a fraction of the Full Scale (FS) digital input/output.

0x3F4[D5:D4]	Tone Amplitude
00	±FS
01	±FS/2
10	±FS/4
11	±FS/8

Table 3: BIST Tone Level.

Figure 2 shows a spectrum analyzer plot of a tone generated by the BIST Signal generator. For this example, the data port frequency of Tx1 was 15.36MHz, 0x3F[D7:D6]=0'b01, which from Equation 1 leads to a tone at 960kHz offset from the LO frequency of 2.01GHz. The tone is generated at half Full Scale (0x3F4[D5:D4]=0'b01), and the Tx1 attenuation (0x073, 0x074) is set to 5dB.

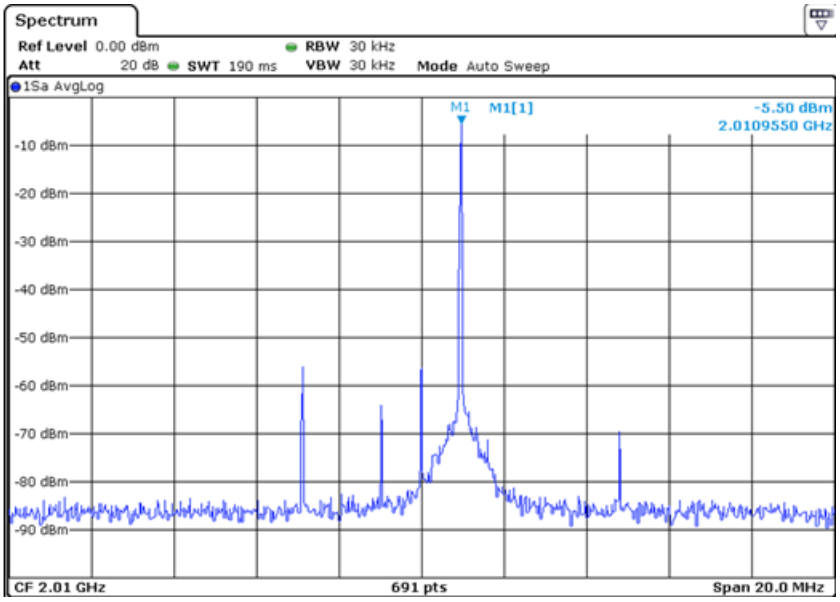

Figure 2: Spectrum analyzer plot showing the BIST Tone generated.

The PRBS is a 16-stage, 14-tap generator that uses the 16th order polynomial shown in Equation 2.

$$G(x) = x^{16} + x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^3 + x^2 + 1$$

Equation 2

The AD9361 implements this polynomial as a 16-bit shift register, 14 taps of which are XORed and then fed into the input of the bit 15 of the shift register. See Figure 3.

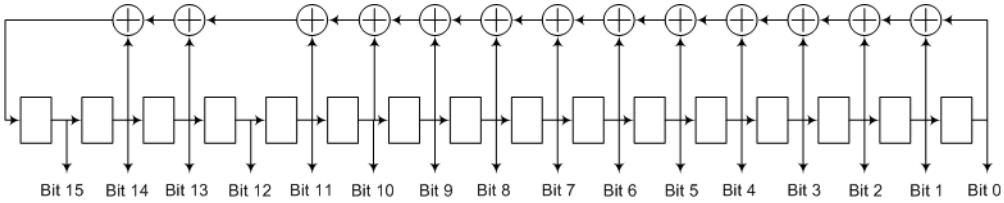

Figure 3.PRBS Shift Register and XOR implementation. "I" Word Shown.

The polynomial exponents 1 to 16 map to bit positions 15 to 0. Since x^1 and x^4 are not part of the polynomial, the outputs of shift registers 15 and 12 are not tapped. The PRBS is implemented using the code shown below.

```
// PRBS polynomial - 16 15 14 13 12 11 10 9 8 7 6 5 3 2
//--------------------------------------------------------------------------
always @ ( posedge I_bist_clk )
 if ( ~O_bist_enable )
   prbs_data <= 16'h0A54;              /*this is the seed value  */
 else
   prbs_data <= { (prbs_data[ 0] ^ prbs_data[ 1] ^ prbs_data[ 2] ^ prbs_data[ 3] ^
              prbs_data[ 4] ^ prbs_data[ 5] ^ prbs_data[ 6] ^ prbs_data[ 7] ^
              prbs_data[ 8] ^ prbs_data[ 9] ^ prbs_data[10] ^ prbs_data[11] ^
              prbs_data[13] ^ prbs_data[14] ), prbs_data[15:1] };


assign prbs_data_rev = { prbs_data[ 0], prbs_data[ 1], prbs_data[ 2], prbs_data[ 3],
```

prbs_data[4], prbs_data[5], prbs_data[6], prbs_data[7],
prbs_data[8], prbs_data[9], prbs_data[10], prbs_data[11],
prbs_data[12], prbs_data[13], prbs_data[14], prbs_data[15] };

Where

prbs_data is the “I” PRBS data

prbs_data_rev is the “Q” PRBS data and is a bit inversion of the “I” data (e.g. bit 0 of “I” is bit 15 of “Q”).

MASKING THE BIST GENERATOR OUTPUT

The Signal that the BIST generator is configured to output will be routed to all active Rx channels, if the injection point is chosen to be the input of the Rx data port from Table 1. The same is true for Tx channels. Thus there are up to 4 signals, CH1 I, CH1 Q, CH2 I, CH2 Q that are generated by the BIST signal generator. The BIST signal generator has the ability to zero the output of each of these signals. This is achieved using bits 0x3F6[D5:D2].

0x3F6	Data set to Zeros
Bit [D5]	CH_2 Q
Bit [D4]	CH_2 I
Bit [D3]	CH_1 Q
Bit [D2]	CH_1 I

Table 4: BIST Signal Generator Mask Bits.

Setting a bit high instructs the BIST Signal Generator to send zeros data to the corresponding data channel listed in Table 4

STEP 1: VERIFY THE RX DATA PORT

The Rx Data Port can be verified by generating a signal and applying it to the input of the Rx data port.

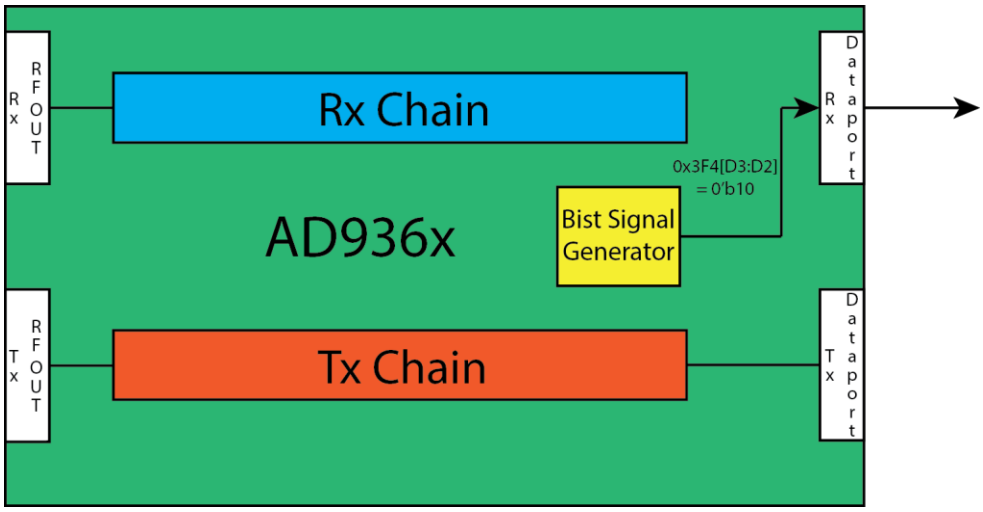

Figure 4: BIST Signal Generator applied to Rx data port.

AD9361 is configured to output a 960 kHz tone through the Rx data port by writing 0x3F4=0x5B. If the tone is correctly received by the Baseband Processor or FPGA, then the Rx data port has been verified.

STEP 2: VERIFYING THE TX DATA PORT (DATA LOOPBACK TEST)

The AD9361 data port has loopback capability. This is a useful way to test the integrity of the data port connection. Data loopback is enabled by setting 0x3F5[D0] high, with data sent to the Tx data port being routed back out the Rx data port. A BER of zero in such a loopback test verifies that the data connection is sound.

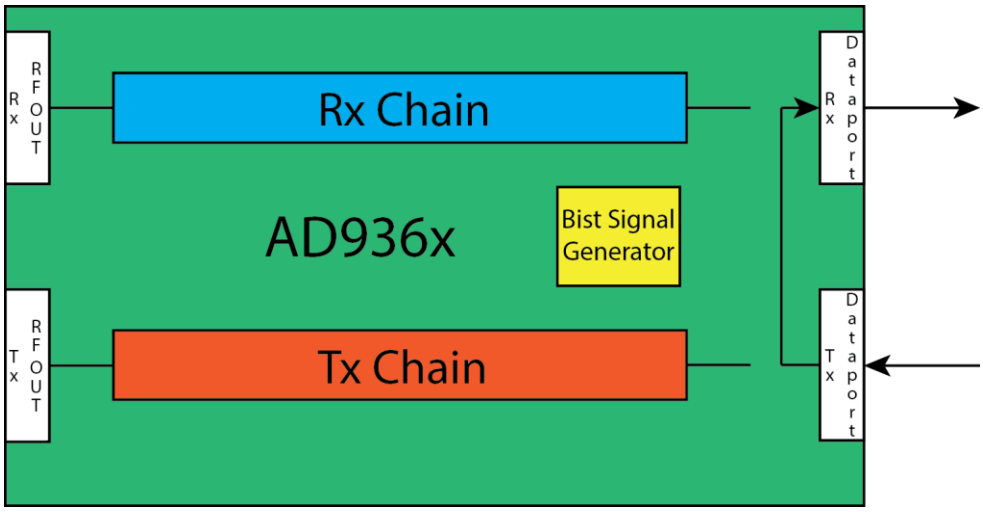

Figure 5: AD9361 Data Loopback.

Both data ports must be enabled for this test to be performed. There are two ways that this can be achieved when the digital interface is setup as follows:

1. **Dual-Port, Full Duplex:** The Enable State machine must be in the FDD state for this. Rx is assigned one port, Tx the other port and data is routed from Tx to Rx data ports.
2. **Single-Port, Half-Duplex:** The Enable State machine must be in the TDD state for this. The same port is used for both Rx and Tx but time multiplexed. By setting bit 0x3F5[D7], Tx data bits sent to this data port will be routed back out the data port not being used.