AD9361, AD9363, AD9364
Documentation changes.

This document captures the documentation changes planned for User guide and Register map for AD9361, AD9363 and AD9364 Radio Verse Transceivers. Document update and release will take time and until that time this document will be maintained for reference.

Current version of documents is as given below. If you don't have the latest, please download same from design file package under below link.
http://www.analog.com/en/design-center/landing-pages/001/integrated-rf-agile-transceiver-design-resources.html

	AD9361	AD9363	AD9364
Data Sheet	Rev F	Rev D	Rev C
User Guide	UG-570 REV A	UG-1040 REV 0	UG-673 REV 0
Register Map	UG-671 REV 0	UG-1057 REV 0	UG-672 REV 0

Below table captures the changes required for documents and their reference. If you have any comments or suggestions to improve documentation, please feel free to post your comments below.

REFERENCE MANUAL CHANGES:

Sl No	Reference	Current statement	Changes
1	UG-570-page 95 to 96, UG-1040-page 79 to 80	Headings and timing diagrams for receive or transmit data needs to be corrected.	Refer appendix A.
2	UG-570-page 8 equation:1 UG-1040-page 7 equation:1 UG-673-page 7 equation:1	There is no definition of the term "Divide Setting".	To be included.
3	UG-673-page-100 table 53 (for LVDS)	Column 2 of table 53 mentions data rate as 122.88 Msps	Data rate needs to be changed to 61.44Msps. The term "combined I and Q words" is to be removed.
4	Reference manuals of all versions of Catalina	Ball J6 "CLK_OUT" has multiple name aliases including "CLOCK_OUT", "CLKOUT" and "CLK Out"	CLK_OUT naming convention to be followed
5	UG-570-page-92 table 48 UG-1040-page-76 table 47 UG-673-page-88 table 51	In CMOS mode in DDR TDD mode, sample rate can be up to 122.88M instead of 61.44M.	Refer appendix B The term "combined I and Q words" is to be removed.

6	Required for all register map	Rise in image frequency at higher power levels. Increase in correction word decimation, i.e., Register x16F (registers x16C-x16F) have been removed from the register map.	Refer appendix C
7	UG-570-page-85 UG-673-page-81 UG-1040-page-72	Register 0x20 = 0x24(toggle the GPO_1 pin in Rx and GPO_2 in Tx) Register 0x20 contains the bits that determine how the GPOs respond to state changes from Alert	If 0x20=0x24, From alert to RX, GPO will go from 0xF to 0x2 (3 GPOs will toggle) From alert to TX, GPO will go from 0xF to 0x4 (3 GPOs will toggle). Register 0x20 defines the "state" or value of GPO upon entering RX or TX state.
8	UG-1040-page-27	Tx HB3 has the following coefficients: [+36, −19, 0, −156, −12, 0, +479, +223, 0, −1215, −993, 0, +3569, +6277, +8192, +6277, +3569, 0, −993, −1215, 0, +223, +479, 0, −12, −156, 0, −19, +36]. Note that the full-scale range for the Tx HB3 filter is 8192 (2^{13}).	The TX HB3 has the following coefficients: [1, 2, 1].The TX INT3 has the following coefficients: [36, -19, 0, -156, -12, 0, 479, 223, 0, -1215, -993, 0, 3569, 6277, 8192, 6277, 3569, 0, -993, -1215, 0, 223, 479, 0, -12, -156, 0, -19, 36]. Note that the full-scale range for the TX INT3 filter is 8192 (2^{13}). The full-scale range for the TX HB3 filter is 2.
9	UG-570-page-10 UG-1040-page-9 UG-673-page-9	Actual BBBW column in table 6 is as follows: Table 6. Typical Tx Baseband Filter Calibration Times Standard / Desired BBBW (MHz) / BBPLL Frequency (MHz) / TxBBF Divider (decimal) / Actual BBBW (MHz) / Max Calibration time (µs) LTE 5 MHz / 2.5 / 983.04 / 28 / 35.1086 / 10.1115 LTE 10MHz / 5 / 983.04 / 14 / 70.2171 / 5.0558 LTE 15 MHz / 7.5 / 737.28 / 7 / 105.326 / 3.3705 LTE 20 MHz / 10 / 983.04 / 7 / 140.434 / 2.5278	The actual BBBW(MHz)(as per equation 7) column in table 6 should be as follows: 2.420688 4.841375 7.262063 9.682751
10	UG-570-page-124 UG-1040-page-105 UG-673-page-115	D3 | VDDA1P3_RX_TX | Short to E3 | Power supply for Tx Low pass filter, Tx monitor, Rx trans impedance amplifier, Rx low pass filter, AuxDAC	Power supply for Tx Low pass filter, Tx monitor, Rx trans impedance amplifier, Rx low pass filter.
11 A calibration can reduce the uncertainty of the temperature sensor reading but even with a calibration, there is significant uncertainty and the sensor should only be used for non-critical functions. A document explaining that is given in the link: https://ez.analog.com/docs/DOC-17804-ad936x-temperature-sensor			
12 Signals closer than 7.5 kHz to DC and which are large in the digital domain can cause the DC offset algorithms to remove those signals, affecting the the algorithm and the desired signals. A document explaining that is given in the link: https://ez.analog.com/docs/DOC-17785-ad936xdcoffsetissue			

DATASHEET CHANGES:

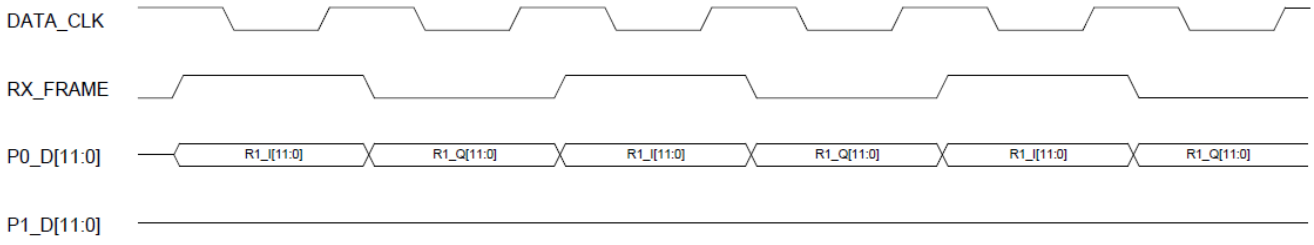
1	Datasheet of AD936X	In the reference clock voltage specification, move the 1.3V pk-pk value to the max column instead of putting it in the typical columns of the specs table (Adding a comment that lower values can degrade performance)	To be updated
2	Table 13 of AD9361 datasheet, Table 12 of AD9363 datasheet, Table 13 of AD9364 datasheet	All Rx and TX data pairs have optional termination	Remove the termination text from RX_Dx_p/n and Termination needs to be added to the definition for FB_CLK and TX_FRAME.
3	Page 18 of AD9363 datasheet	The description of pin no J6 states: ”This pin can be configured to output either a buffered version of the external input clock (the digital controlled crystal oscillator (DCXO)) or a divided down version of the internal ADC sample clock (ADC_CLK)”.	The words“(the digital controlled crystal oscillator (DCXO))” are to be removed. The AD9363 only allows reference injection via pin M12, i.e. XTALN; its neighbor M11 is DNC (in AD9361/64 this is XTALP), so unlike its sister parts, the AD9363 does not support the DCXO option.

REGISTER MAP CHANGES:

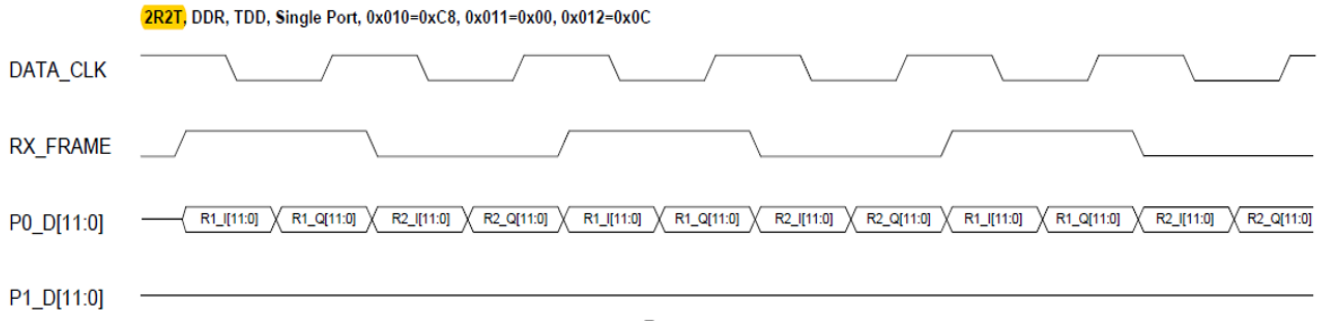
1	UG-671-page16, UG-1057-page-16, UG-672-page-16	Applies to the fast AGC. The AGC Attack Delay prevents the AGC from starting its algorithm until the receive path has settled	Applies to slow and fast AGC.
2	UG-671-page-65 and 60, UG-1057-page-63 and 68,UG-672-page-60 and 65	In registers x238 and x278 we need to put VCO Cal Offset back into the register words, those were zero-ed out by mistake.	To be updated
3	UG-671-table 9, UG-672-table 9, UG-1057-table 9	For ADC_CLK /2 and ADC_CLK/3 works fine but for ADC_CLK/4 onwards it gives wrong clk_out as after MUX 1, output is routed to HB3 clk.	Table 9 needs to be updated as in appendix D
4	UG-671-table 84 UG-672-table 84, UG-1057-table 83	If tones are injected in RX, the mask bit always flips the IQ i.e. if I is masked Q samples are zero.	Naming convention needs to be changed in reg map document register 0X3F6
5	UG-671-page 18, UG-1057-page 20, UG-672-page 18	The register definitions (0x03c, D5) refers to the setting as "Rx On Chip Term" and say all data path bits plus TX_FRAME and FB_CLK.	That needs to be changed from the "all data path pins" to TX_Dx_p/n pins.

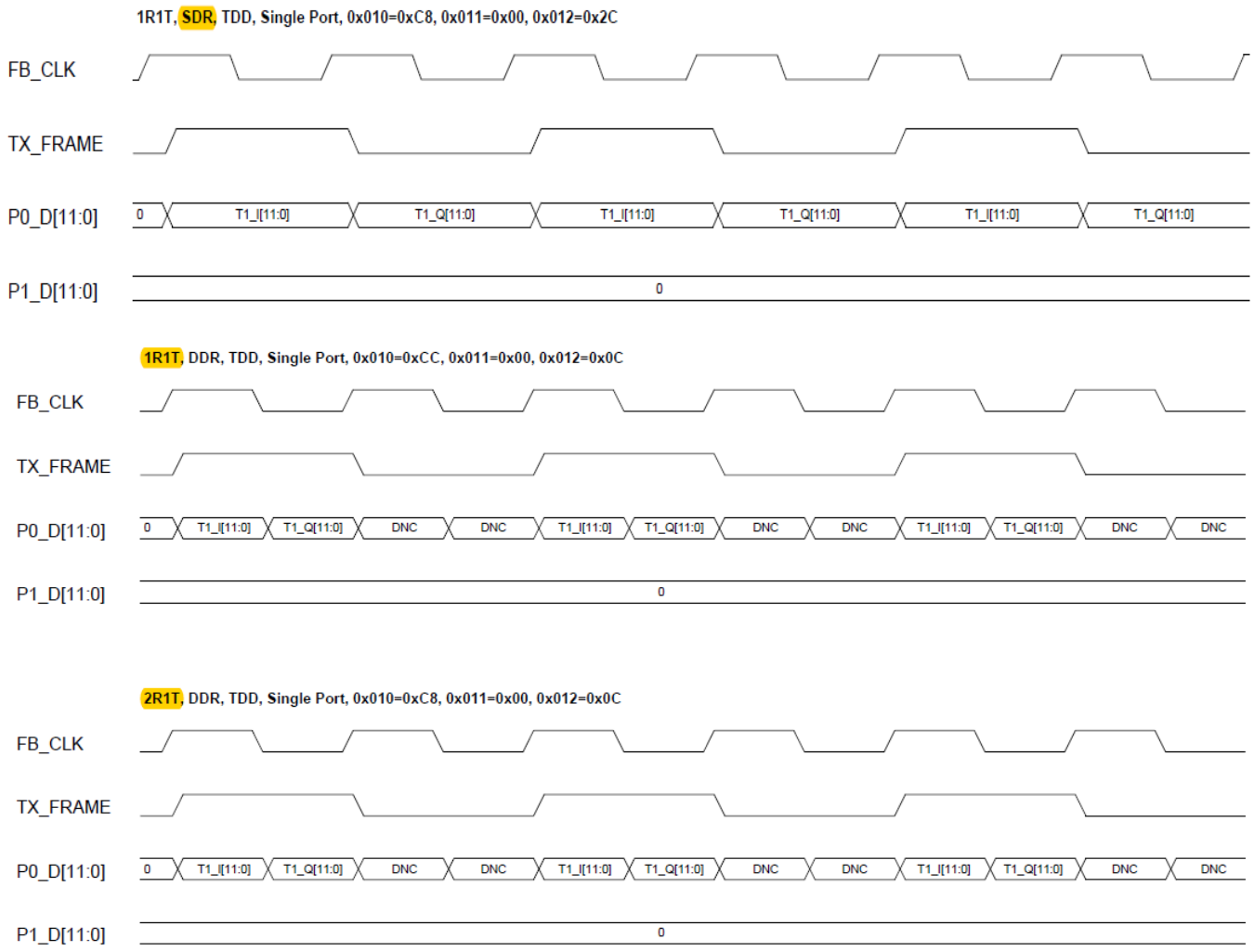
6	UG-671-page 33	Resolution: 1pF/LSB. Total capacitance is 12pF + Capacitor<5:0> *1pF (required for the calculation of 3db cut off frequency)	To be updated
7	UG-671-page 15 UG-672-page 15 UG-1057-page 15	This nibble controls which GPO_x pins change state when the ENSM enters the Rx state	It defines the "state" or value of GPO upon entering RX or TX state.
8	UG-671-page 60 and page 65 UG-672-page 60 and page 65 UG-1057-page 63 and page 68	For register 0x23D and 0x27D,Bit [D5] in the reg map is an “open” bit. Bit [D4] however, is described as “CP Offset Off Setting this bit disables the charge pump bleed current. Clear to use the value in “Charge Pump Offset” (0x23C[D5:D0]) as the offset current.”	CP offset current needs to be disabled by setting the CP Offset Off bit (0x23D[D5] for Rx and 0x27D[D5] for Tx)

APPENDIX A:



DESCRIPTION





APPENDIX B:

OPERATING MODE	DATA RATE	
	SDR	DDR
Single Port Half Duplex	30.72	61.44
Single Port Full Duplex	15.36	30.72
Dual Port Half Duplex	61.44	61.44*
Dual Port Full Duplex	30.72	61.44

* Limited by data clock rate

APPENDIX C:

SPI Register 0x16E—Rx Quad Cal Gain1

This is the receiver gain used when the AD9361 runs an Rx Quadrature Calibration using a test tone. The LNA gain is not relevant since the tone injects into the mixer input. For a full gain table (0x0FB[D3] clear), this register is the Gain Table Index and 0x16E[D4:D0] is not used. For a split gain table, 0x16E specifies the LMT Index and 0x16E[D4:D0] specifies the LPF index.

SPI Register 0x16F—Rx Quad Cal Gain 2

[D7:D5] Correction Word Decimation M<2:0> These bits control the decimation used by the accumulate and dump block of the Rx Quad Cal algorithm and are only applicable if 0x169[D2] = 1.

[D4:D0] LPF Gain See 0x16E.

APPENDIX D:

CLKOUT Select[2:0]	CLKOUT Frequency
000	XTALN (or DCXO) (buffered)
001	ADC_CLK/2
010	ADC_CLK/3
011	ADC_CLK/(X *2)
100	ADC_CLK/(X *4)
101	ADC_CLK/(X *8)
110	ADC_CLK/(X *16)
111	ADC_CLK/(X *32)

X = 2 for HB3 dec = 1,2
X= 3 for HB3 dec = 3