High Speed ADC's

Hardware:
HSC-ADC-EVALB-DC
HSC-ADC-FPGA-8
HSC-ADC-EVALC

Software:
ADC Analyzer
Visual Analog

Analog Devices © 2007 Applications Note by Martin Murnane

General Interface

There are several High Speed ADC Evaluation PCB's available from Analog Devices, and there are a number of various data capture boards that are used to evaluate these ADC. This document will throw some light on the various types of ADC evaluation boards and how they are connected to the various data capture board.

The control boards currently available are the:

HSC-ADC-EVALB-DC**
(dual channel)
HSC-ADC-EVALC
HSC-ADC-EVALCZ

This replaces the HSC-ADC-EVALA**-SC, HSC-ADC-EVAL**A**-DC, and HSC-ADC-EVALB-SC**,** which are no longer available.

HSC-ADC-EVALB-DC

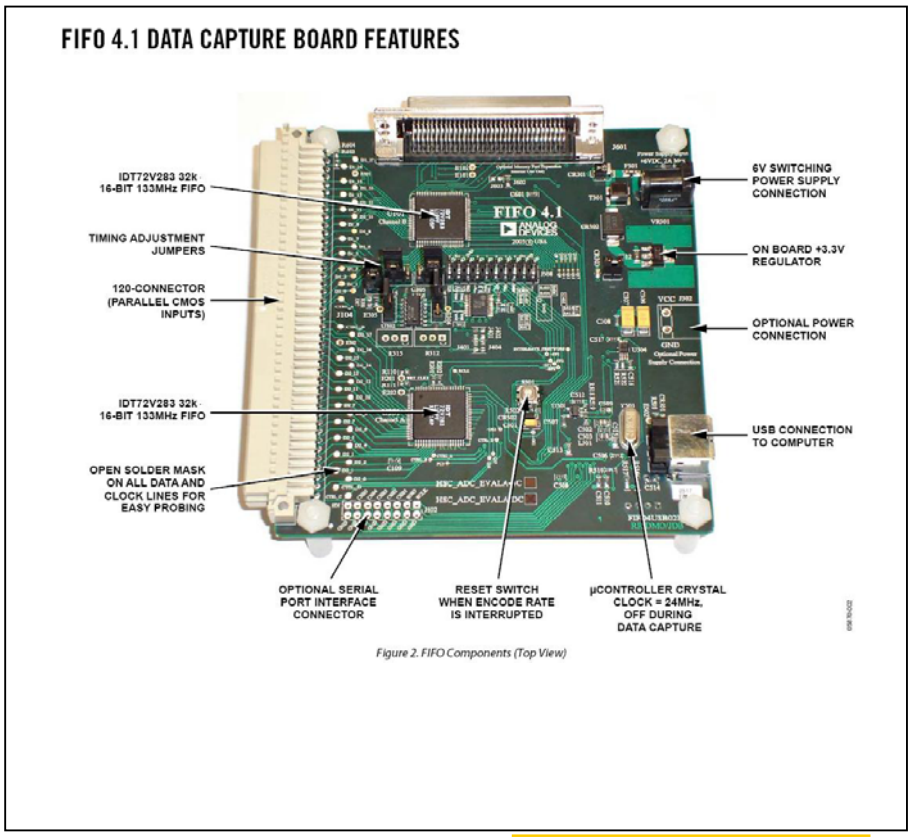


Figure 2. FIFO Components (Top View)

HSC-ADC-EVALB-DC (FIFO4.1)

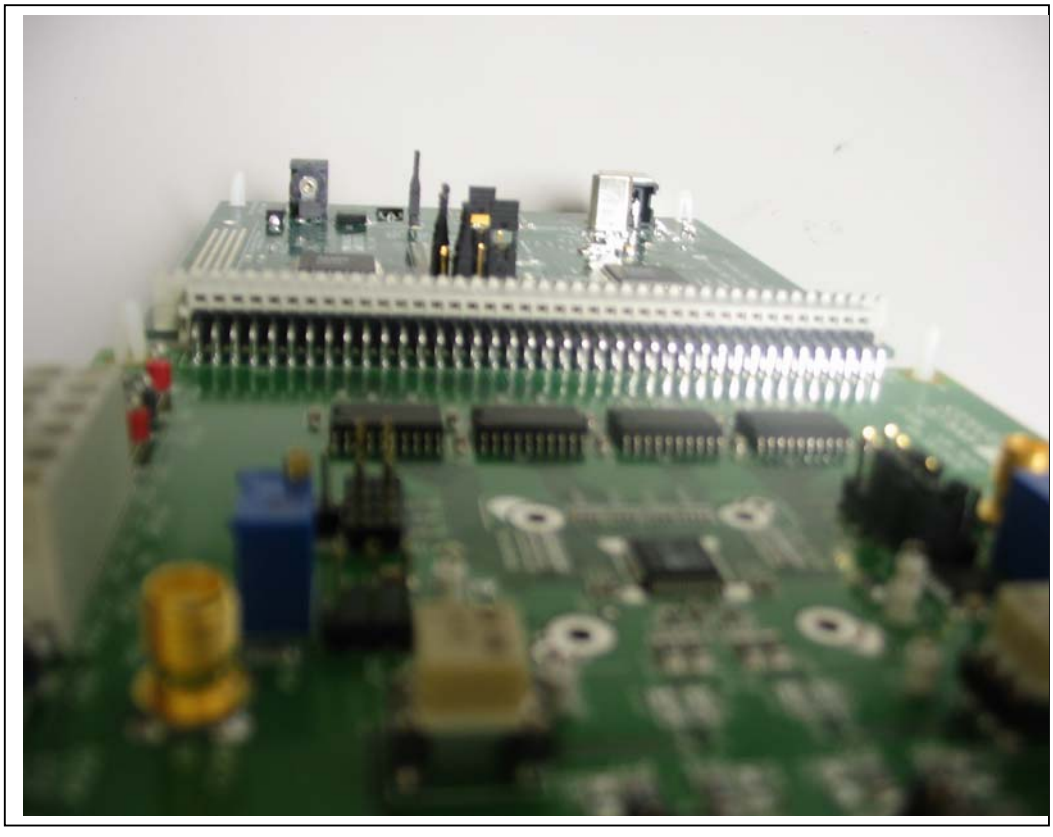
This device shown in the previous page is the HSC-ADC-EVALB-DC board with 2 FIFO Channels. The FIFO device is the IDT72V283 133MHZ FIFO. The top FIFO device is channel B and the lower one is channel A. In the Photo, you will notice a Centronic's Connector and a USB connector on the board.

HSC-ADC-EVALB-XX (FIFO4.1)

"The bottom two rows of pins are identical between the HSC-ADC-EVALA – SC/DC and the HSC-ADC-EVALB-DC …. ."

The HSC-ADC-EVALB-DC Boards have a 120 pin connector to interface with the ADC evaluation PCB's. The older HSC-ADC-EVALA-SC/DC had a 80 pin connector. So there is an extra row on this new EVALB cards and the main reason for this, is primarily to route the Serial Port (SPI) signals over to our newer ADC's which feature SPI interfaces. The bottom two rows of pins are identical between HSC-ADC-EVALA–SC/DC and HSC-ADC-EVALB-DC.

For example, taking a look at the interface of the AD9238, evaluation PCB, and the HSC-ADC-EVALB-DC data capture board in the photo below, you will see that the bottom two rows are used, leaving the top row unconnected. This is how the ADC evaluation boards are interfaced to the new data capture board.

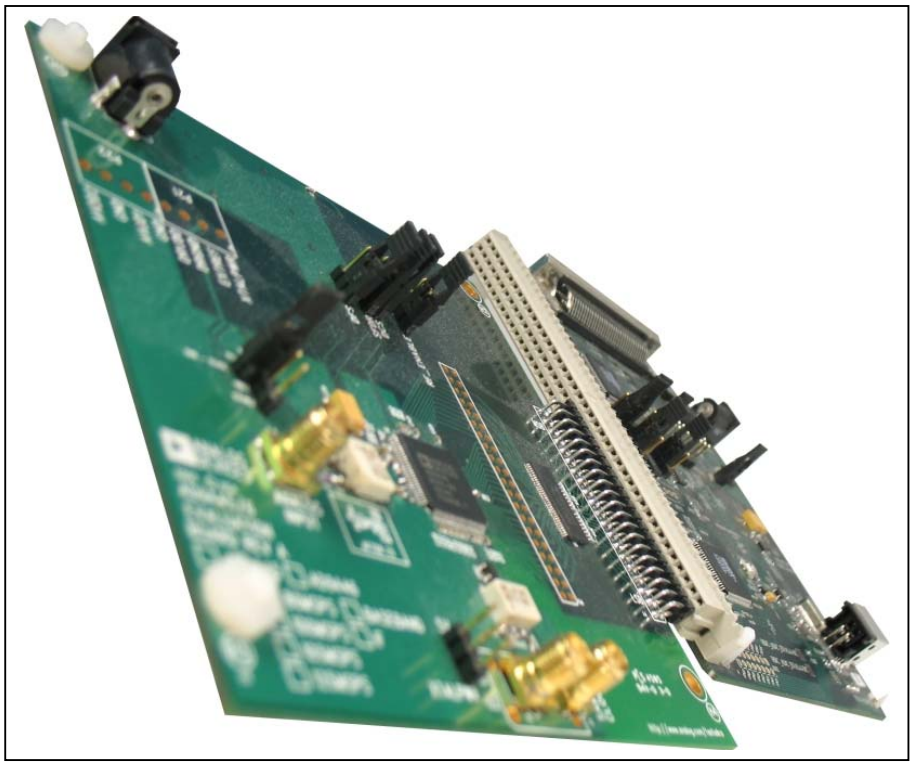


How to Interface 40 Pin ADC 's e.g.AD9446

Some of our ADC boards are mapped to a 40pin output that can be ***either fully left, or fully right justified*** into the bottom two rows on the EVALB. The photo of the AD9446 Evaluation PCB photo demonstrates the concept. Just remember that you have to justify the ADC evaluation board to mate with the desired channel of the FIFO board. You can use either side on the Dual Channel (HSC-ADC-EVALB-DC) FIFO board.

If your customer has the single channel FIFO board (HSC-ADC-EVALB-SC) remember that you have to justify the ADC evaluation board to mate with the populated side of the single-channel (SC) FIFO board. So, for a HSC-ADC-EVALB-SC, the evaluation card is right justified as shown in the photo.

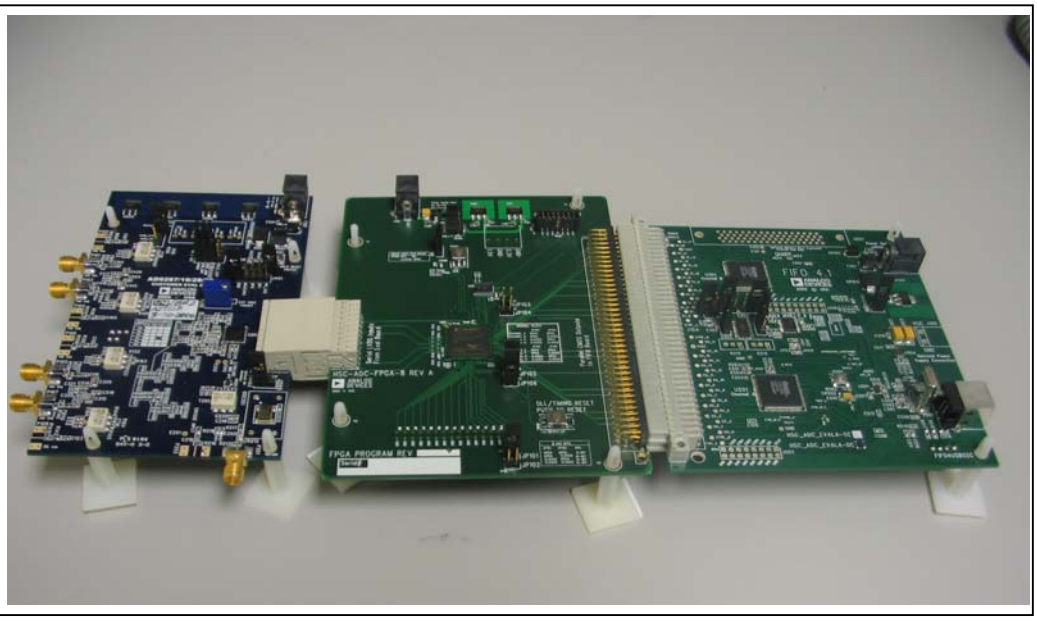
"….can be ***either fully left, or fully right justified*** into the bottom two rows**.** …."



How to Interface with Serial LVDS Devices, e.g Quad and Octal Family ADCs

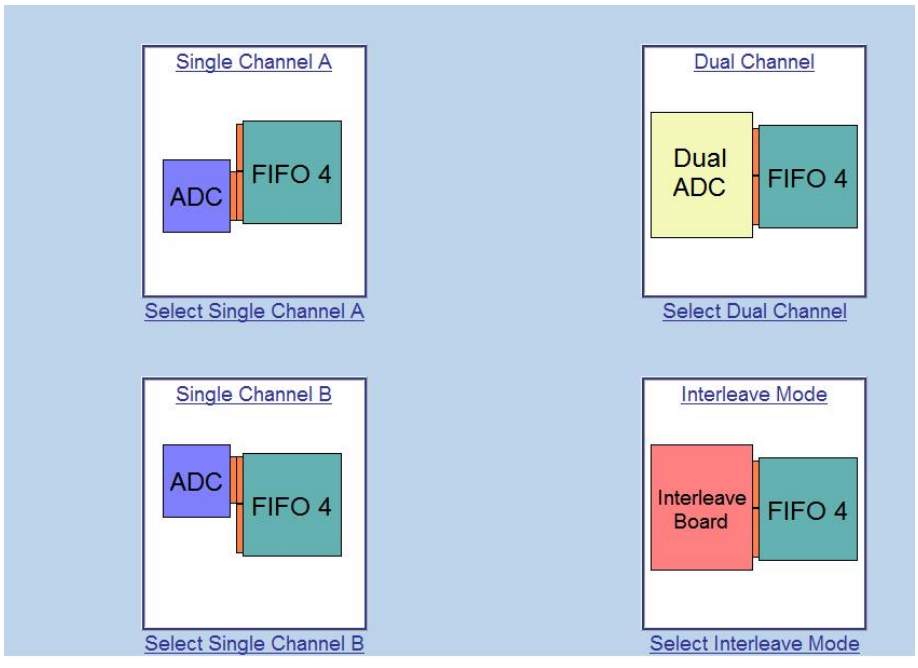
Devices like the AD9228 Quad ADC with serial LVDS outputs require an extra intermediary board between the ADC evaluation board and the data capture board. These devices require a serial LVDS to CMOS converter board called the HSC-ADC-FPGA-8 or deserializer board. These are connected as shown below.

Information on these connectors can be found in the respective datasheets of the evaluations boards.



Setting ADC Analyzer Configuration for FIFO4 & FIFO4.1

Depending on your configuration, that you have selected, you will also need to configure the ADC Analyzer software program to match that of your hardware set-up. See options below that can be used. This is found in ADC Analyzer under the Help menu About HSC-ADC-EVALX-DC.



HSC-ADC-EVALC (FIFO5)

The new generation of control boards are the HSC-ADC-EVALC devices. These are FPGA based data capture boards as opposed to FIFO based devices, like the HSC-ADC-EVALA/B-XX data capture boards. See photo below of the new type boards.

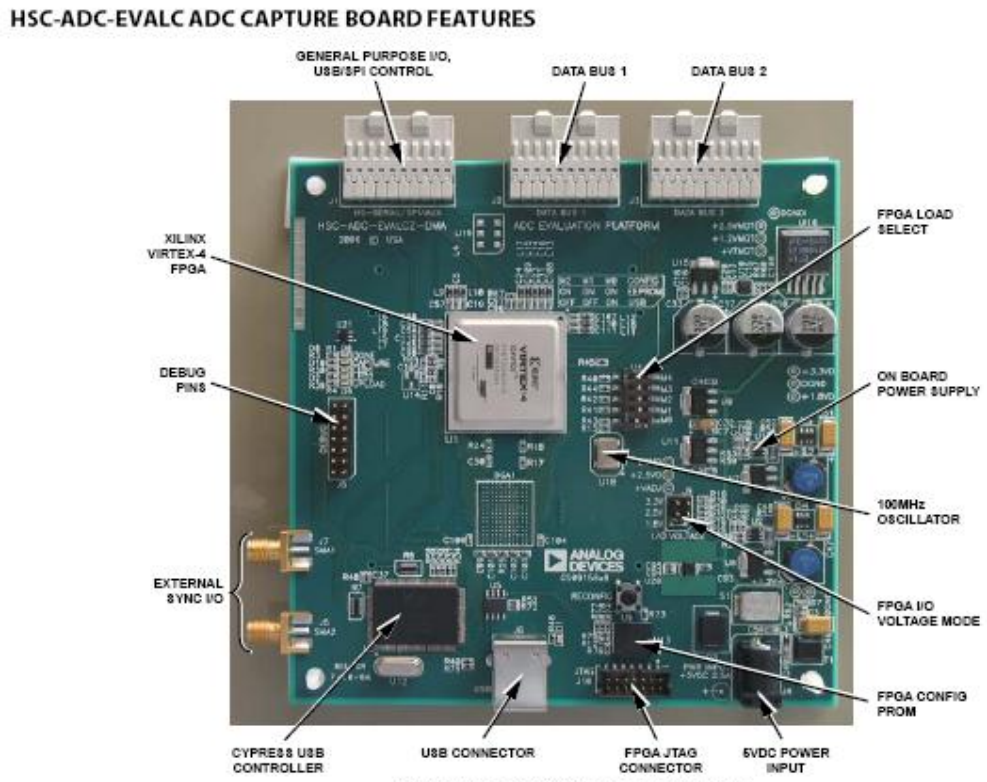


Figure 3. HSC-ADC-EVALC Components (Top View)

If using a the new FIFO5 data capture board then also a new interface software is VisualAnalog® is required.

These new control Boards are due out in May 2007 approximately.

Further information for both VisualAnalog and the new control board can be got from our website at:
http://www.analog.com/VisualAnalog
http://www.analog.com/FIFO